



US005774402A

# United States Patent [19] Lee

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[45] **Date of Patent:** Jun. 30, 1998

[54] **INITIALIZATION CIRCUIT FOR A SEMICONDUCTOR MEMORY DEVICE**

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[57] **ABSTRACT**

[21] Appl. No.: 697,356

An initialization circuit for a semiconductor memory device includes an initialization signal generator that generates an initialization signal in response to a specific sequence of reset control signals. A transfer unit activates a reset signal for resetting various circuits in the device in response to either the initialization signal or a conventional power-up initialization signal. Thus, the initialization signal generator provides reliable initialization even if the power-up detection circuit fails. External row and column address strobe signals serve as two reset control signals, while a mode selection signal serves as another reset control signal. The initialization signal is activated when the three reset control signals are activated in the proper sequence, then deactivated when one of the control signals is deactivated.

[22] Filed: **Aug. 23, 1996**

[30] **Foreign Application Priority Data**

Aug. 23, 1995 [KR] Rep. of Korea ..... 26181/1995

[51] **Int. Cl.<sup>6</sup>** ..... **G11C 7/00**

[52] **U.S. Cl.** ..... **365/191; 365/193**

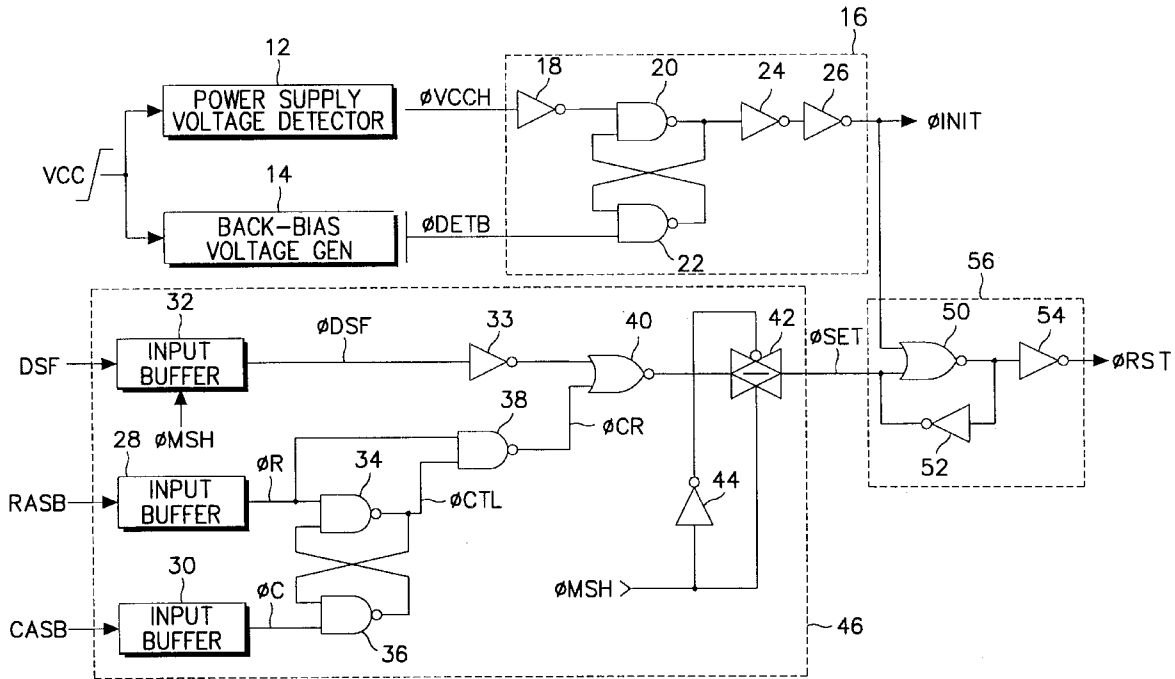
[58] **Field of Search** ..... 365/191, 193;  
327/143, 198, 217

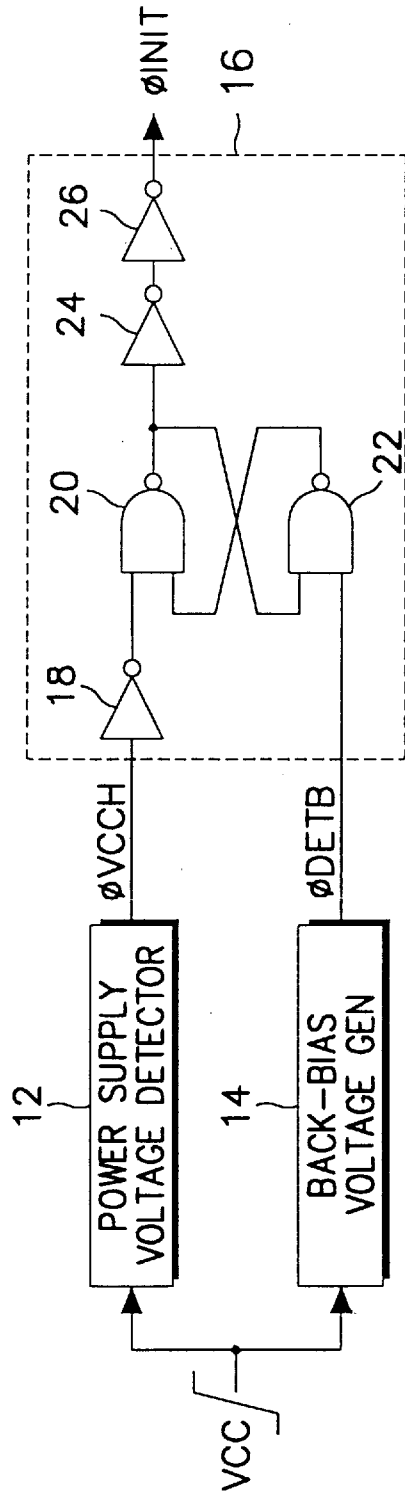
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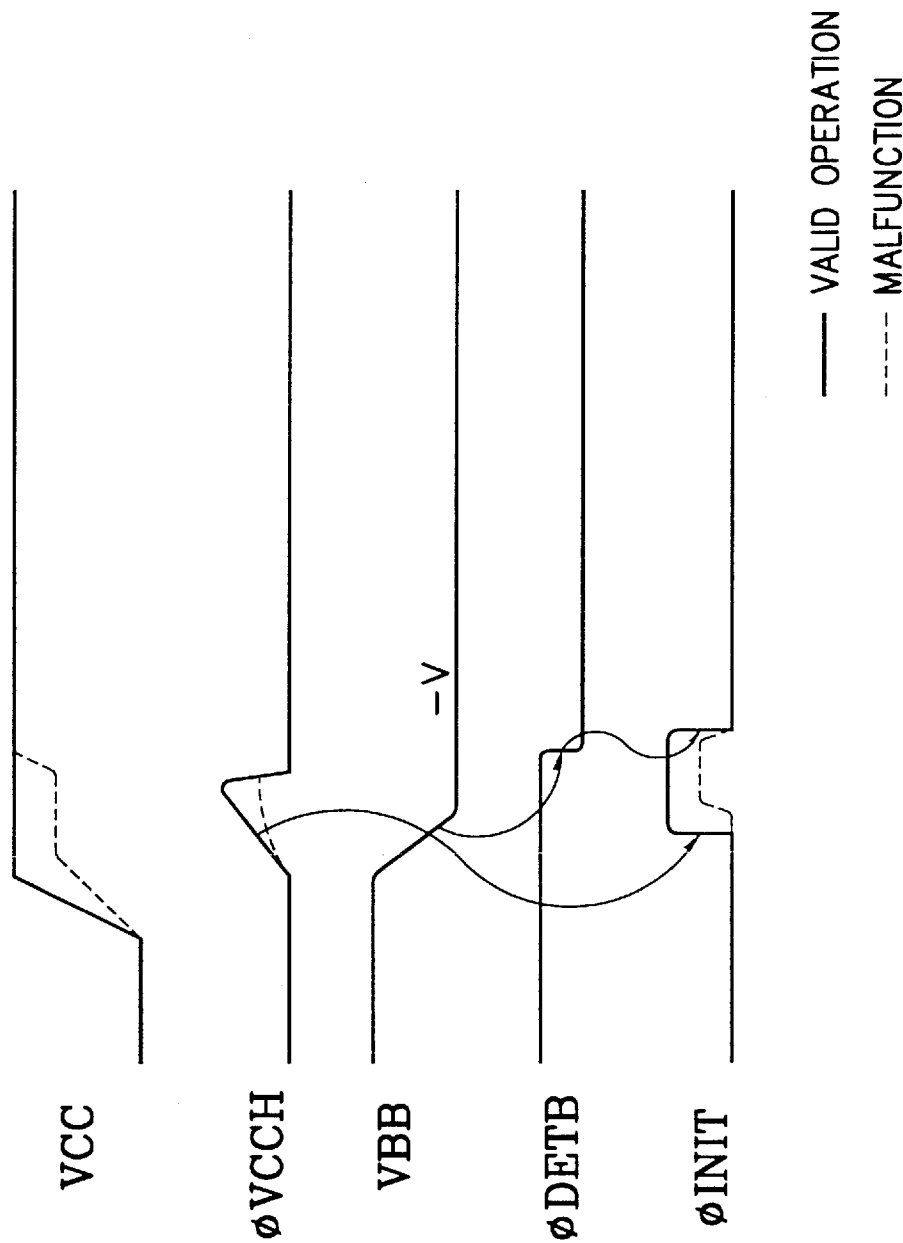
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**19 Claims, 4 Drawing Sheets**





(PRIOR ART)  
Fig. 1



(PRIOR ART)  
Fig. 2

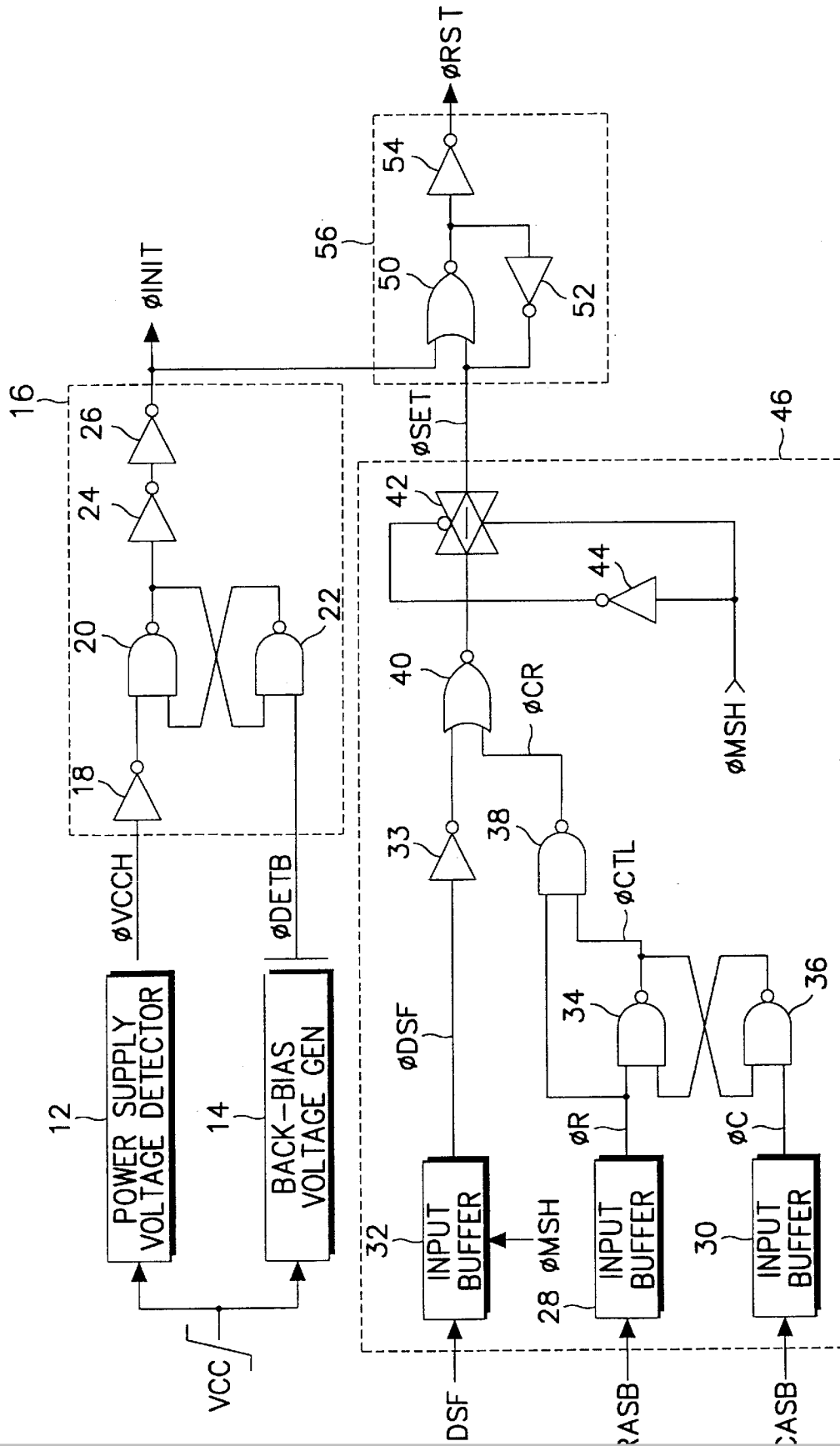


Fig. 3

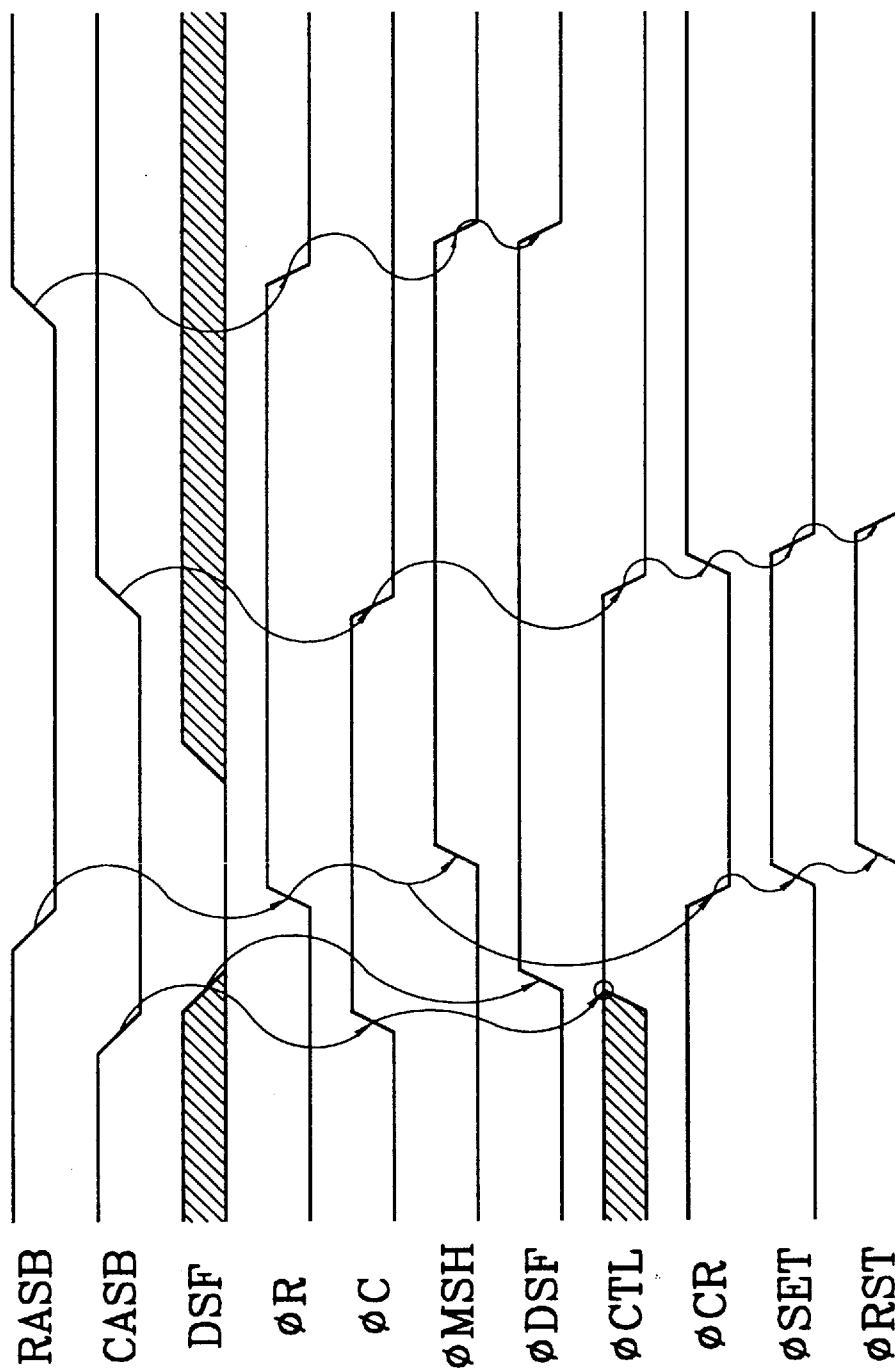


Fig. 4

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