

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

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**DECLARATION OF STEPHEN W. MELVIN**

Case No. IPR2023-00516

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Mail Stop Patent Board  
Patent Trial and Appeal Board  
U.S. Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

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Exhibit No.	Description
1001	U.S. Patent No. 6,157,589 (the “’589 Patent”)
1002	U.S. Prosecution History of the ’589 Patent
1003	Declaration of Stephen W. Melvin
1004	U.S. Patent No. 5,559,753 to Kocis entitled “Apparatus and Method for Preventing Bus Contention During Power-Up in a Computer System With Two or More DRAM Banks” (“Kocis”)
1005	U.S. Patent No. 5,774,402 to Lee entitled “Initialization Circuit for a Semiconductor Memory Device” (“Lee”)
1006	JEDEC Standard No. 21-C, entitled “Configurations for Solid State Memories,” Compilation of Releases 1 through 7, dated January 1997 (“JESD 21-C”)
1007	U.S. Patent No. 5,703,510 to Iketani et al. entitled “Power On Reset Circuit For Generating Reset Signal at Power On” (“Iketani”)
1008	Prosecution History of EPO Patent Application No. 99 113 048.5 (Original)
1009	Excerpt of Prosecution History of EPO Patent Application No. 99 113 048.5 (Original)
1010	Excerpt of Prosecution History of EPO Patent Application No. 99 113 048.5 (English Translation)
1011	Japanese Patent Publication No. JP 09 106668 A to Samsung Electronics Co. Ltd. dated April 22, 1997 (“Tetsuka”)
1012	Declaration of Julie Carson
1013	JEDEC Standard No. 21-C, entitled “Configurations for Solid State Memories,” Release 7, dated January 1997
1014	Scheduling Order, <i>Polaris Innovations Limited v. Xilinx, Inc.</i> , 1:22-cv-00174-RGA, Docket No. 20 (May 31, 2022)
1015	United States District Courts — Federal Court Management Statistics, National Judicial Caseload Profile (June 30, 2022), available at <a href="https://www.uscourts.gov/sites/default/files/fcms_na_distprofile0630.2022_0.pdf">https://www.uscourts.gov/sites/default/files/fcms_na_distprofile0630.2022_0.pdf</a>
1016	Motion Success for Stay Pending IPR before Judge Richard G. Andrews in the District of Delaware (Docket Navigator data from 2020 to 1/20/2023)
1017	Excerpt of Micron Technology, Inc., “DRAM Data Book” (1992)

Exhibit No.	Description
1018	Excerpt of Samsung Electronics Co., Ltd., "Data Book: DRAM" (Dec. 1995)
1019	Samsung Electronics, "4M x 8Bit x 4 Banks Synchronous DRAM" Doc. No. KM48S16030, Rev. 2 (March 1998)

## **I. Introduction**

1. I have prepared this Declaration in connection with Xilinx, Inc.'s Petition for *Inter Partes* Review of U.S. Patent No. 6,157,589 (the "'589 Patent") (Ex. 1001), which is to be filed concurrently with this Declaration.

2. In the course of preparing this Declaration, I reviewed the '589 Patent, its prosecution file history, as well as the other documents discussed in this Declaration.

3. I have been retained by Xilinx, Inc. ("Xilinx" or "Petitioner") as an expert in the fields of computer engineering, computer memory systems and related technologies. My employer is being compensated at my normal consulting rate for my time. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration. I have no financial interest in Xilinx, the '589 Patent or the owner of the '589 Patent.

## **II. Background and Qualifications**

4. I received a Ph.D. in Computer Science from the University of California at Berkeley in 1991 and a B.S. in Electrical Engineering and Computer Science from the University of California at Berkeley in 1982. I have more than 40 years of experience in computer science and computer engineering. I am an inventor on over 45 patents, and I am a registered patent agent before the USPTO.

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