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APPLICATION NUMBER: *09/343,431*
FILING DATE: *June 30, 1999*
PATENT NUMBER: *6,157,589*
ISSUE DATE: *December 5, 2000*

By Authority of the
Under Secretary of Commerce for Intellectual Property
and Director of the United States Patent and Trademark Office

Trudie Wallace
Certifying Officer

JC825 U.S. PTO 09/343431 06/30/99

ISSUE CLASSIFICATION	Class	Subclass
	365	226

PATENT NUMBER
6157589
6157589

U.S. UTILITY PATENT APPLICATION

O.I.P.E.	PATENT DATE
SCANNED A.G.B. O.A.	DEC 05 2000

SECTOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
	365	226	2824 ~~2759~~	Vu Le

FILED WITH: ☐ DISK (CRF) ☐ FICHE
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ORIGINAL		CROSS REFERENCE(S)	
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365	226	365	228

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10-20-00 Formal Drawings(3 shts)set 1 6-30-99

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	3	4	2	13	1

☐ a) The term of this patent subsequent to _____ (date) has been disclaimed.

(Assistant Examiner) (Date)

NOTICE OF ALLOWANCE MAILED
7/17/00

☐ b) The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____.

Group 2800
AU 2824
Vu A. Le
(Primary Examiner) (Date)

ISSUE FEE (W)

Amount Due	Date Paid
$1,210.00	10-3-00

☐ c) The terminal ____months of this patent have been disclaimed.

(Legal Instruments Examiner) 7/18/00 (Date)

ISSUE BATCH NUMBER
P31

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Form PTO-436A
(Rev. 6/98)

ISSUE FEE IN FILE

(LABEL AREA)

Formal Drawings(___shts)set___

(FACE)

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/343,431	06/30/99	365	2818	GR98P1989

APPLICANT

GUNNAR KRAUSE, MUENCHEN, FED REP GERMANY.

CONTINUING DOMESTIC DATA********
VERIFIED

OG NONE

371 (NAT'L STAGE) DATA********
VERIFIED

OG NONE

FOREIGN APPLICATIONS********
VERIFIED FED REP GERMANY 198 29 287.2 06/30/98

OG

IF REQUIRED, FOREIGN FILING LICENSE GRANTED 07/26/99

Foreign Priority claimed 35 USC 119 (a-d) conditions met	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☒yes ☐no ☒yes ☐no ☐Met after Allowance Verified and Acknowledged OG (Examiner's Initials) _____ (Initials)	DEX	3	13	2

ADDRESS

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PO BOX 2480
HOLLYWOOD FL 33022-2480

TITLE

DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INTIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit
$890		

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SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/343,431	06/30/99	365	2818	GR98P1989

APPLICANT

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CONTINUING DOMESTIC DATA********
VERIFIED

371 (NAT'L STAGE) DATA********
VERIFIED

FOREIGN APPLICATIONS********
VERIFIED FED REP GERMANY 198 29 287.2 06/30/98

IF REQUIRED, FOREIGN FILING LICENSE GRANTED 07/26/99

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LERNER AND GREENBERG, P.A.

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"Express Mail" mailing label number EL080659885US
Date of Deposit June 30, 1999

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XIOMARA D. JUNCO

Docket No.: GR 98 P 1989

Date: June 30, 1999

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Enclosed herewith are the necessary papers for filing the following application for Letters Patent:

Applicant : GUNNAR KRAUSE

Title : DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

3 sheets of formal drawings in triplicate.
A check in the amount of $760.00 covering the filing fee.
Information Disclosure Statement and 1 Reference.

This application is being filed without a signed oath or declaration under the provisions of 37 CFR 1.53(d). Applicants await notification of the date by which the oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted,

For Applicant

LAURENCE A. GREENBERG
REG. NO. 29,308

LAG:tg

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

07/13/1999 KHARLING 00000038 09343431
01 FC:101 760.00 OP

PTO-1556
(5/87)

*U.S. GPO: 1998-433-214/80404

Abstract of the Disclosure:

09/343431

A dynamic semiconductor memory device of a random access type has an initialization circuit that controls the switching-on operation of the semiconductor memory device and of its circuit components. The initialization circuit supplies a supply voltage stable signal once the supply voltage has been stabilized after the switching-on of the semiconductor memory device. The initialization circuit has an enable circuit that receives the supply voltage stable signal and further command signals externally applied to the semiconductor memory device. The enable circuit supplies an enable signal after a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is identified. The enable signal effects the unlatching of a control circuit provided for the proper operation of the semiconductor memory device.

REL/cgm

GR 98 P 1989

DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

Background of the Invention:

Field of the Invention:

The invention relates to a dynamic semiconductor memory device of the random access type (DRAM/SDRAM) having an initialization circuit which controls a switching-on operation of the semiconductor memory device and of its circuit components. The initialization circuit supplies a supply voltage stable signal (POWERON) once a supply voltage has been stabilized after the switching-on of the semiconductor memory device. The invention also relates to a method for initializing such a dynamic semiconductor memory device, and also to the use of an enable circuit, that supplies an enable signal, for controlling the switching-on operation of the dynamic semiconductor memory device.

In the case of SDRAM semiconductor memories according to the JEDEC standard, it is necessary to ensure during the switch-on operation ("POWERUP") that the internal control circuits provided for the proper operation of the semiconductor memory device are reliably held in a defined desired state, in order to prevent undesirable activation of output transistors that would cause, on the data lines, a short circuit (so-called "bus contention" or "data

contention") or uncontrolled activation of internal current loads. The solution to the problem turns out to be difficult on account of a fundamental unpredictability of the time characteristic of the supply voltage and of the voltage level or levels at the external control inputs during the switch-on operation of the semiconductor memory. According to the specifications of the manufacturer an SDRAM component should ignore all commands which are present chronologically before a defined initialization sequence. The sequence consists of predetermined commands that must be applied in a defined chronological order. However, a series of functions and commands which are allowed during proper operation of the component are desired or allowed chronologically only after the initialization sequence. According to the JEDEC standard for SDRAM semiconductor memories, a recommended initialization sequence (so-called "POWERON-SEQUENCE") is provided as follows:

a. the application of a supply voltage and a start pulse in order to maintain an NOP condition at the inputs of the component;

b. the maintenance of a stable supply voltage of a stable clock signal, and of stable NOP input conditions for a minimum time period of 200 us;

c. the preparation command for word line activation (PRECHARGE) for all the memory banks of the device;

4. the activation of eight or more refresh commands (AUTOREFRESH); and

5. the activation of a loading configuration register command (MODE-REGISTER-SET) for initializing the mode register.

After the identification of such a defined initialization sequence, the memory module is normally in a so-called IDLE state, that is to say it is precharged and prepared for proper operation. In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.

Summary of the Invention:

It is accordingly an object of the invention to provide a dynamic semiconductor memory device and a method for initializing a dynamic semiconductor memory device which overcome the above-mentioned disadvantages of the prior art methods and devices of this general type, which is as simple as possible in structural terms and which effectively prevents the risk of a short circuit

of the data lines and/or of uncontrolled activation of internal current loads.

With the foregoing and other objects in view there is provided, in accordance with the invention, a dynamic semiconductor memory device of a random access type, containing an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. The initialization circuit has a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals. The enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals are identified and the enable signal effecting an unlatching of the control circuit.

The invention provides for the initialization circuit to have an enable circuit, which receives the supply voltage stable signal and the externally applied further command signals. The enable circuit generates the enable signal after the identification of the predetermined proper initialization sequence of the command signals is achieved. The enable signal effects the unlatching of the control circuit provided for the proper operation of the semiconductor memory device.

Following the principle of the invention, the enable signal (CHIPREADY) is generated and becomes active in dependence on further internal signals and the initialization sequence and then unlatches predetermined circuits. The predetermined circuits remain latched until the end of the predetermined initialization sequence. By way of example, commands are decoded but not executed and the output drivers are held at high impedance.

According to the preferred application in SDRAM memory devices according to the JEDEC standard, it is provided that the command signals, externally applied to the semiconductor memory device, of the initialization sequence are to be identified by the enable circuit. The command signals include a preparation command signal for word line activation (PRECHARGE), and/or a refresh command signal (AUTOREFRESH), and/or a loading configuration register command signal (MODE-REGISTER-SET).

According to an advantageous structural refinement of the initialization circuit according to the invention, it is provided that the enable circuit has at least one bistable multivibrator stage with a set input which receives the command signal (PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET). The bistable multivibrator also has a reset input to which the supply voltage stable signal (POWERON), a signal derived therefrom, or a linked signal is applied. The bistable multivibrator further has an output at which the enable signal (CHIPREADY) is outputted.

In particular, the enable circuit has a plurality of bistable multivibrator stages respectively receiving the command signals.

In an expedient refinement of the invention, it is provided that the output of at least one of the bistable multivibrator stages is passed to a reset input of a further multivibrator stage. In this case, it may furthermore be provided that, in one of the bistable multivibrator stages, the supply voltage stable signal (POWERON) and the signal output from the output of the further multivibrator stage are passed, after having been logically combined by a gate, to the reset input of the multivibrator stage.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a dynamic semiconductor memory device and a method for initializing a dynamic semiconductor memory device, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof

will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 is a diagrammatic, block diagram of components of an initialization circuit which controls a switching-on operation of a semiconductor memory and its circuit components according to the invention;

Fig. 2 is circuit diagram of an enable circuit that supplies an enable signal (CHIPREADY);

Fig. 3 is a time sequence diagram for elucidating a method of operation of the circuit according to Fig. 2; and

Fig. 4 is a circuit diagram of the enable circuit according to an exemplary embodiment of the invention.

Description of the Preferred Embodiments:

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there are shown circuit components, important for understanding the invention, of an SDRAM memory device operating according to the JEDEC standard.

The circuit components include an initialization circuit controlling a switching-on operation of the SDRAM memory device and its circuit components. The initialization circuit has an input circuit 1, to whose input 2 command and clock signals that are externally applied in reference to the semiconductor memory are provided. The command and clock signals are amplified and conditioned before being received by a command decoder 3 connected downstream of the input circuit 1 and at whose output 4, inter alia, the command signals PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command) and MRS or MODE-REGISTER-SET (loading configuration register command) are output. The initialization circuit further has a circuit 5 for internal voltage regulation and/or detection, at whose input 6 the external supply voltages that are externally applied to the semiconductor memory externally are fed in. The circuit 5 has a first output 7 outputting a POWERON signal and a second output 8 supplying stabilized internal supply voltages. The method of operation and the structure of the circuits 1, 3 and 5 are sufficiently known to the person skilled in the art and therefore do not need to be explained in any more detail. What is important for understanding the invention is the fact that the circuit 5 supplies an active POWERON signal if, after the POWERUP phase of the SDRAM memory, the internal supply voltages present at the output 8 have reached the values necessary for proper operation of the component.

According to the invention, the initialization circuit furthermore has an enable circuit 9 connected downstream of the circuits 3 and 5. The command signals PRE, ARF and MRS are applied to an input 10 of the enable circuit 9 and the POWERON signal is applied to an input 11 of the enable circuit 9. An enable signal CHIPREADY is supplied at an output 12 of the enable circuit 9 after the identification of a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is achieved. The enable signal effects unlatching of control circuits 13 provided for proper operation of the semiconductor memory device. The internal control circuits 13 serve inter alia for sequence control for one or more of the memory blocks of the SDRAM memory and are known as such.

Fig. 2 shows a preferred exemplary embodiment of the enable circuit 9 according to the invention. The enable circuit 9 contains three bistable multivibrator stages 14, 15 and 16 each having a set input S, a reset input R, and also an output Q. An AND gate 17 connected upstream of the reset input R of the multivibrator stage 15 and an AND gate 18 connected downstream of all the outputs Q of the multivibrator stages 14, 15, 16 are further provided. The enable circuit further has an inverter 19 connected downstream of the AND gate 18. The enable signal CHIPREADY being output at the output 12 of the inverter 19 and the enable signal CHIPREADY is active HIGH, that is to say activated when its voltage level is at logic HIGH. The command signals PRE,

ARF, MRS applied to the respective set inputs S of the bistable multivibrator stages 14, 15, 16 are each active LOW, that is to say these signals are active when their voltage level is at logic LOW, while the POWERON signal is again active HIGH. The POWERON signal is applied directly to the reset inputs R in the case of the multivibrator stages 14 and 16 and is firstly applied to one input of the AND gate 17 in the case of the multivibrator stage 15, the signal output from the output Q of the multivibrator stage 14 is applied to the other input of the AND gate 17, the output of the AND gate 17 is connected to the reset input of the multivibrator stage 15.

The method of operation of the enable circuit 9 illustrated in Fig. 2 is such that activation of the enable signal CHIPREADY at the output 12 to logic HIGH is generated only when a predetermined chronological initialization sequence of the command signals PRE, ARF and MRS and activation of the POWERON signal to the logic level HIGH are detected. Only then are the control circuits 13 unlatched on account of the activation of the enable signal CHIPREADY; the control circuits 13 remaining latched prior to this.

In the schematic time sequence diagram according to Fig. 3, exemplary command sequences during the switching-on operation of the semiconductor memory device are illustrated in order to elucidate the method of operation of the enable circuit 9.

In the case situation A, the signal PRECHARGE is activated to active LOW too early relative to the activation of the POWERON signal, with the result that, the enable signal CHIPREADY is not yet activated to logic HIGH since the proper initialization sequence requires a waiting time before the first command. The signal swing of the command PRECHARGE according to case situation A is thus correctly ignored. In case situation B, the chronological order of the activation of the signal AUTOREFRESH to logic LOW is incorrect since the proper initialization sequence prescribes a previous PRECHARGE command before the AUTOREFRESH command. The signal swing of the AUTOREFRESH signal to logic LOW according to case situation B is therefore likewise ignored, and the enable signal does not go to logic HIGH. In case situation C, a correct chronological order of the commands PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET is present conforming to the JEDEC standard, in a logically consistent manner, since the POWERON signal is also at logic HIGH, an enable signal CHIPREADY at logic HIGH is now supplied. Illustrated using dashed lines, another further conceivable initialization sequence that is allowed and therefore triggers an enable signal is represented by the symbol D; activation of the command MODE-REGISTER-SET to logic LOW is allowed at any time after the activation of the POWERON signal.

Fig. 4 shows further details of a preferred exemplary embodiment of the enable circuit 9 according to the invention. In this

exemplary embodiment, each of the bistable multivibrators 14, 15, 16 is constructed from in each case two NAND gates 14A, 14B, 15A, 17, 16A, 16B and also an inverter 14C, 15C and 16C, which are connected to one another in the manner illustrated. The NAND gate 17 is provided with three inputs in the bistable multivibrator 15.

I Claim:

1. A dynamic semiconductor memory device of a random access type, comprising:

an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation, said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals, said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

2. The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal.

3. The semiconductor memory device according to claim 1, wherein said enable circuit has at least one bistable multivibrator stage having a set input receiving the externally applied further command signals, a reset input receiving one of the supply voltage

stable signal, a signal derived from the supply voltage stable signal and a linked signal, and an output outputting said enable signal.

4. The semiconductor memory device according to claim 3, wherein said at least one bistable multivibrator stage is a plurality of bistable multivibrator stages respectively receiving one of the externally applied further command signals.

5. The semiconductor memory device according to claim 4, wherein said output of one of said plurality of bistable multivibrator stages is passed to said reset input of another of said plurality of bistable multivibrator stages.

6. The semiconductor memory device according to claim 4, including an AND gate receiving the supply voltage stable signal and a signal output from said output of one of said plurality of bistable multivibrator stages, said AND gate outputting an output signal received at said reset input of another of said plurality of bistable multivibrator stages.

7. The semiconductor memory device according to claim 4, wherein said plurality of bistable multivibrator stages are each formed of an RS flip-flop constructed from one of at least two NOR and at least two NAND gates.

8. The semiconductor memory device according to claim 1, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.

9. The semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.

10. The semiconductor memory device according to claim 1, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences:

a) firstly PRE, secondly ARF, thirdly MRS;

b) firstly PRE, secondly MRS, thirdly ARF; and

c) firstly MRS, secondly PRE, or thirdly ARF;

where,

PRE = the preparation command signal for word line activation,

ARF = the refresh command signal, and

MRS = the loading configuration register command signal.

11. An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components, the improvement which comprises:

supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device; and

supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

12. The method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals.

13. The method according to claim 11, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit.

Docket No.: GR 98 P 1989

COMBINED DECLARATION AND POWER OF ATTORNEY
IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

German Application No. 198 29 287.2, filed June 30, 1998, the International Priority of which is claimed under 35 U.S.C. §119.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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LAURENCE A. GREENBERG (Reg.No.29,308)
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I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE INVENTOR: GUNNAR KRAUSE

INVENTOR'S SIGNATURE: ______________________________

DATE: ______________________

Residence: MUENCHEN, GERMANY

Country of Citizenship: GERMANY

Post Office Address: SCHLIERSEESTRASSE 8
D-81541 MUENCHEN
GERMANY

PRINT OF DRAWINGS
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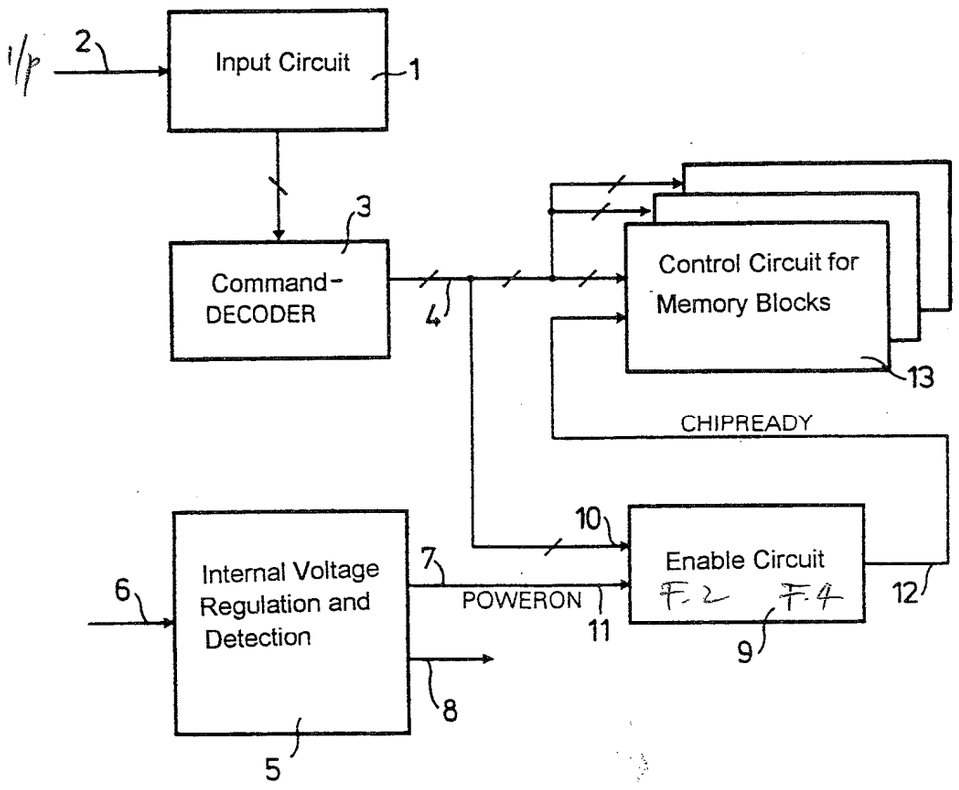
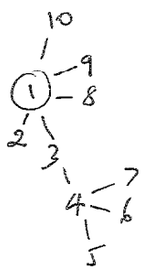
365/226

Fig 1





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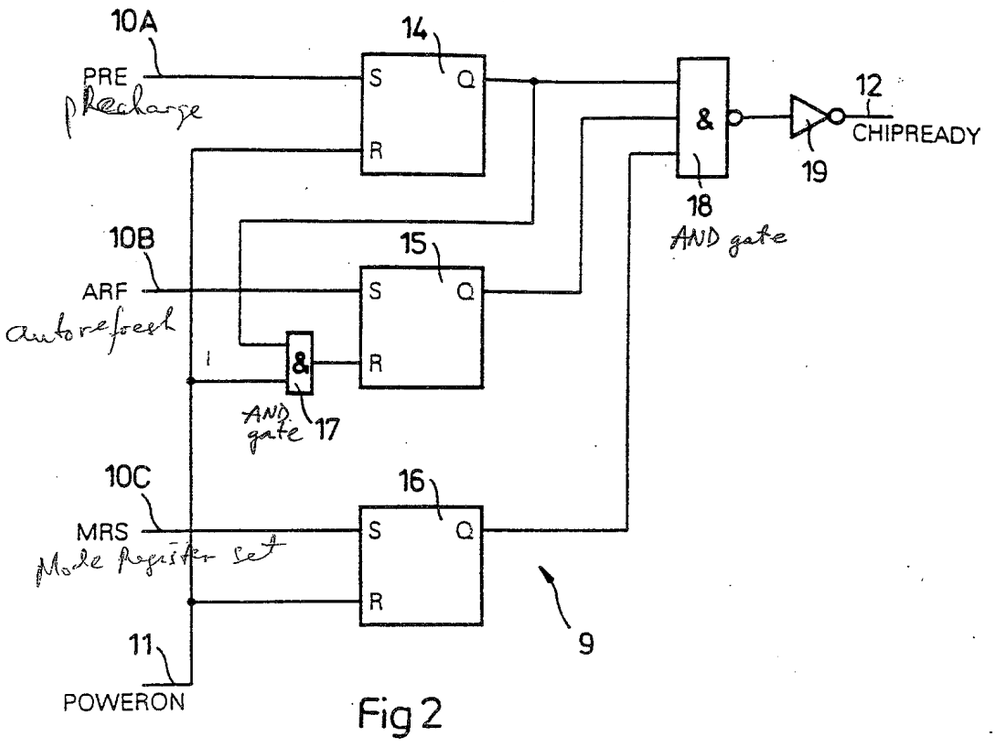

Fig 2

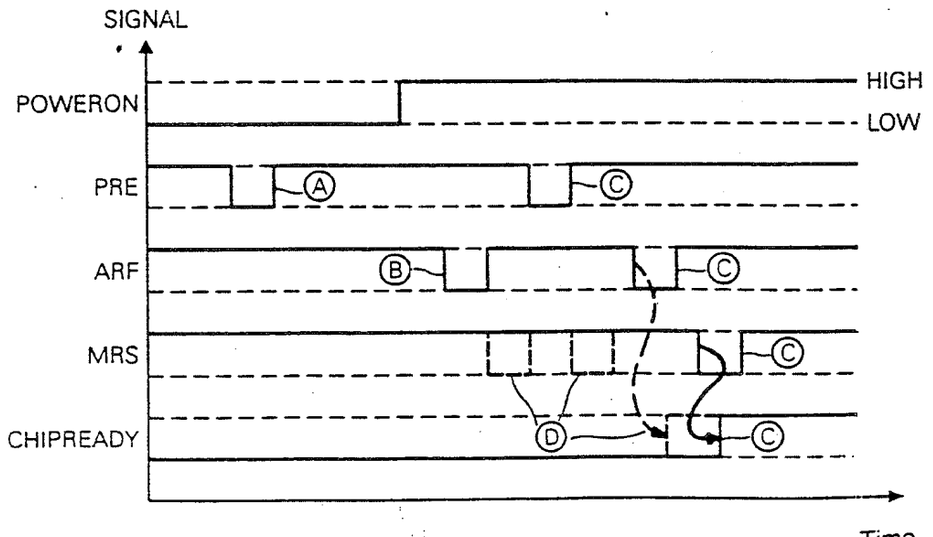

Fig 3

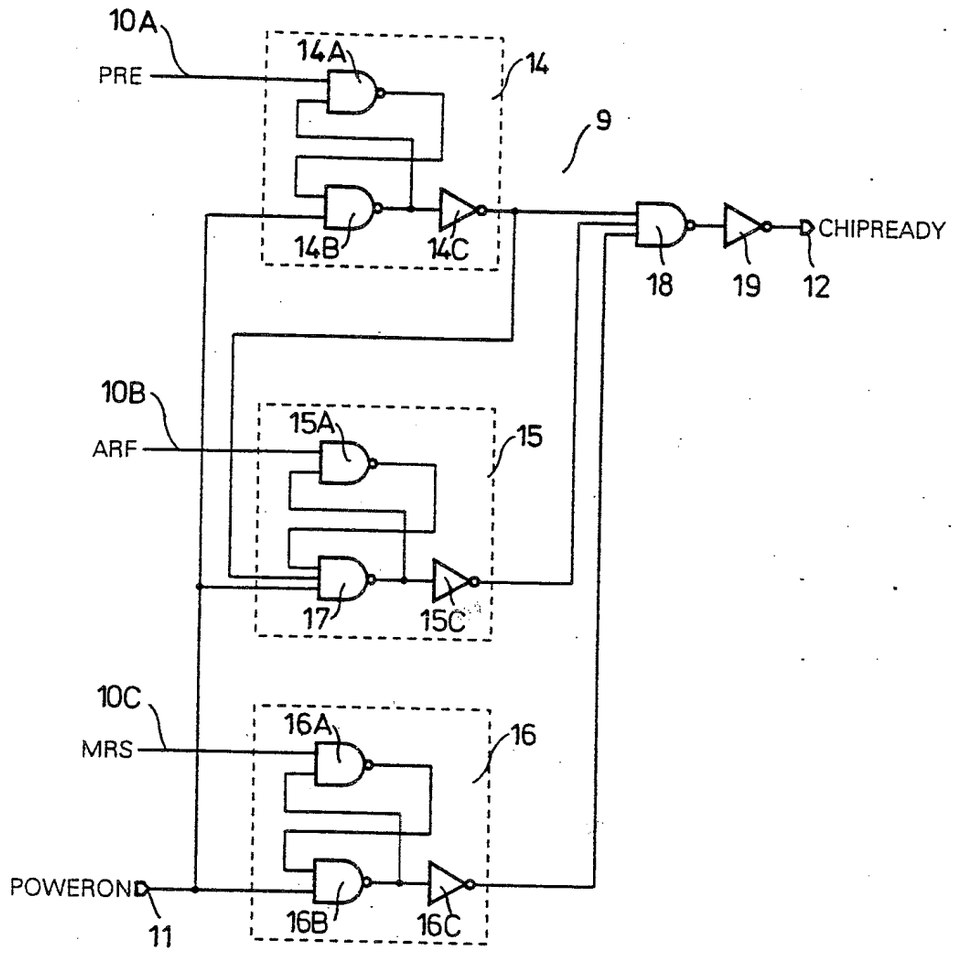

Fig 4

#2

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
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Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO./TITLE
09/343,431	06/30/99	KRAUSE	GR98P1989

0212/0727

LERNER AND GREENBERG PA
PO BOX 2480
HOLLYWOOD FL 33022-2480

NOT ASSIGNED

2818

DATE MAILED: 07/27/99

NOTICE TO FILE MISSING PARTS OF APPLICATION
Filing Date Granted

An Application Number and Filing Date have been assigned to this application. The items indicated below, however, are missing. Applicant is given TWO MONTHS FROM THE DATE OF THIS NOTICE within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a). **If any of items 1 or 3 through 5 are indicated as missing, the SURCHARGE set forth in 37 CFR 1.16(e) of ☐ $65.00 for a small entity in compliance with 37 CFR 1.27, or ☒ $130.00 for a non-small entity, must also be timely submitted in reply to this NOTICE to avoid abandonment.**

If all required items on this form are filed within the period set above, the total amount owed by applicant as a ☐ small entity (statement filed) ☐ non-small entity is $_____.

☐ 1. The statutory basic filing fee is:
- ☐ missing.
- ☐ insufficient.

Applicant must submit $_____ to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).

☐ 2. The following additional claims fees are due:

$_____for_____total claims over 20.

$_____for_____independent claims over 3.

$_____for multiple dependent claim surcharge.

Applicant must either submit the additional claim fees or cancel additional claims for which fees are due.

☒ 3. The oath or declaration:
- ☒ is missing or unsigned.
- ☐ does not cover the newly submitted items.

An oath or declaration in compliance with 37 CFR 1. 63, including residence information and identifying the application by the above Application Number and Filing Date is required.

☐ 4. The signature(s) to the oath or declaration is/are by a person other than inventor or person qualified under 37 CFR 1.42, 1.43 or 1.47.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

☐ 5. The signature of the following joint inventor(s) is missing from the oath or declaration:

_____

An oath or declaration in compliance with 37 CFR 1.63 listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

☐ 6. **A $50.00 processing fee is required since your check was returned without payment (37 CFR 1.21(m)).**

☐ 7. Your filing receipt was mailed in error because your check was returned without payment.

☐ 8. The application was filed in a language other than English.
Applicant must file a verified English translation of the application, the $130.00 set forth in 37 CFR 1.17(k), unless previously submitted, and a statement that the translation is accurate (37 CFR 1.52(d)).

☐ 9. OTHER:_____

Direct the reply and any questions about this notice to "Attention: Box Missing Parts."

A copy of this notice MUST be returned with the reply.

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FORM **PTO-1533** (REV. 9/98) U.S. GPO: 1998–446-824

PART 1 - ATTORNEY/APPLICANT COPY

Docket No.: GR 98 P 1989

COMBINED DECLARATION AND POWER OF ATTORNEY
IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

German Application No. 198 29 287.2, filed June 30, 1998, the International Priority of which is claimed under 35 U.S.C. §119.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

HERBERT L. LERNER (Reg.No.20,435)
LAURENCE A. GREENBERG (Reg.No.29,308)
WERNER H. STEMER (Reg.No.34,956)
RALPH E. LOCHER (Reg.No.41,947)

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POST OFFICE BOX 2480
HOLLYWOOD, FLORIDA 33022-2480
TEL: (954) 925-1100
FAX: (954) 925-1101

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE INVENTOR: GUNNAR KRAUSE

INVENTOR'S SIGNATURE: Gunnar H. Krause

DATE: July 5, 1999

Residence: MUENCHEN, GERMANY

Country of Citizenship: GERMANY

Post Office Address: SCHLIERSEESTRASSE 8
D-81541 MUENCHEN
GERMANY

Docket # GR98P1989
Applic. # 09/343,431
Applicant: Krause

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100 Fax: (954) 925-1101

Docket No.: GR 98 P 1

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

By: _____ Date: September 27, 1999

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Gunnar Krause
Appl. No.	:	09/343,431
Filed	:	June 30, 1999
Title	:	Dynamic Semiconductor Memory Device And Method For Initializing A Dynamic Semiconductor Memory Device
Art Unit	:	2818

LETTER

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

The above-mentioned new patent application was filed on June 30, 1999 without a signed oath or declaration, under the provision of 37 C.F.R. 1.53(f).

In accordance with the above-mentioned rule, enclosed herewith is the original signed declaration as required by the Notice To File Missing Parts Of Application dated July 27, 1999.

The undersigned hereby states that the application filed in the Patent and Trademark Office is the application which the inventor(s) executed by signing the declaration. MPEP 601.01(a)(6)

The fee required for the late filing of an oath or declaration in the amount of $130.00 is also enclosed.

Respectfully submitted,

GREGORY I. MAYBACK
REG NO. 40,719

xdj

Date: September 27, 1999

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Hollywood, FL 33022-2480
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Fax: (954) 925-1101

#4

Docket No.: GR 98 P 1989

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : GUNNAR KRAUSE

Filed : Concurrently herewith

Title : DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U.S. Patent No. 5,307,319 (Kohketzu et al.), dated April 26, 1994.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308

For Applicant

Date: June 30, 1999

Lerner and Greenberg, P.A.
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Hollywood, FL 33022-2480
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Fax: (954) 925-1101

/tg

FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: GR 98 P 1989 Appl. No. 09/343,431 Applicant GUNNAR KRAUSE Filing Date JUNE 30, 1999 Group Art Unit

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
VL	A	5,307,319	04/94	Kohketsu et al.	—	—	
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J							
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED
Vu Le	7/11/00

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

98P1989

B1

US005307319A

United States Patent [19]

Kohketsu et al.

[11] Patent Number: 5,307,319

[45] Date of Patent: Apr. 26, 1994

[54] **INITIALIZATION SETTING CIRCUIT AND SEMICONDUCTOR MEMORY DEVICE USING THE SAME**

[75] Inventors: **Takashi Kohketsu; Teruo Seki**, both of Kasugai, Japan

[73] Assignee: **Fujitsu Limited**, Japan

[21] Appl. No.: **844,659**

[22] PCT Filed: **Aug. 28, 1991**

[86] PCT No.: **PCT/JP91/01143**

§ 371 Date: **Apr. 2, 1992**

§ 102(e) Date: **Apr. 2, 1992**

[87] PCT Pub. No.: **WO92/03825**

PCT Pub. Date: **Mar. 5, 1992**

[30] **Foreign Application Priority Data**

Aug. 28, 1990 [JP] Japan 2-227215

[51] **Int. Cl.**[5] **G11C 13/00**

[52] **U.S. Cl.** **365/230.08**; 365/189.01; 365/189.05

[58] **Field of Search** 365/189.01, 230.01, 365/203, 189.05, 230.08

[56] **References Cited**

U.S. PATENT DOCUMENTS

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5,124,951 6/1992 Slemmer 365/230.08

FOREIGN PATENT DOCUMENTS

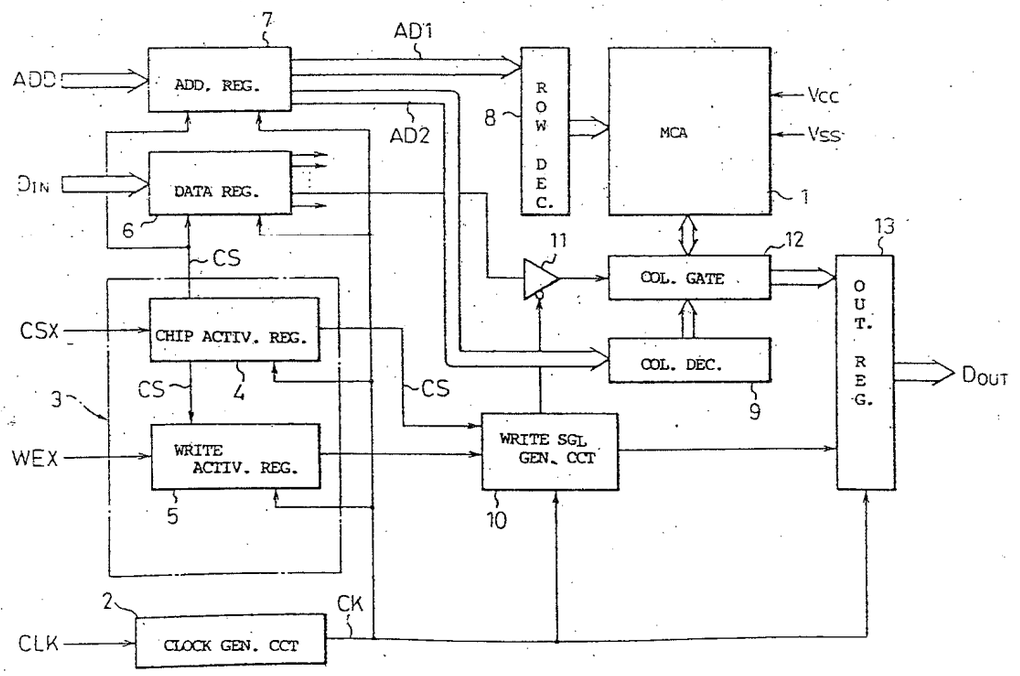
0155113 9/1985 European Pat. Off. .
63-314914 12/1988 Japan .

Primary Examiner—Terrell W. Fears
Attorney, Agent, or Firm—Welsh & Katz, Ltd.

[57] **ABSTRACT**

An initialization setting circuit (**20**) is adapted to set an initial condition of a latch circuit in a semiconductor device upon ON-set of the power supply, comprises a detecting circuit (**TR1, TR2, R, 21**) responsive to ON-set of power supply to detect the power source voltage (Vcc) reaching a given voltage, and an output level control circuit (**22**) responsive to the detecting signal output from the detecting circuit, for elevating up the level of an output signal of the initialization setting circuit to a high potential level or lowering the level of the output signal of the initialization setting circuit to a low potential level. By supplying the output signal controlled by said output level control circuit of the latch circuit as the power source voltage; the operation of the latch circuit is synchronized when the power source voltage is shut down, and a malfunction can be successfully prevented upon resetting of the power supply.

11 Claims, 8 Drawing Sheets



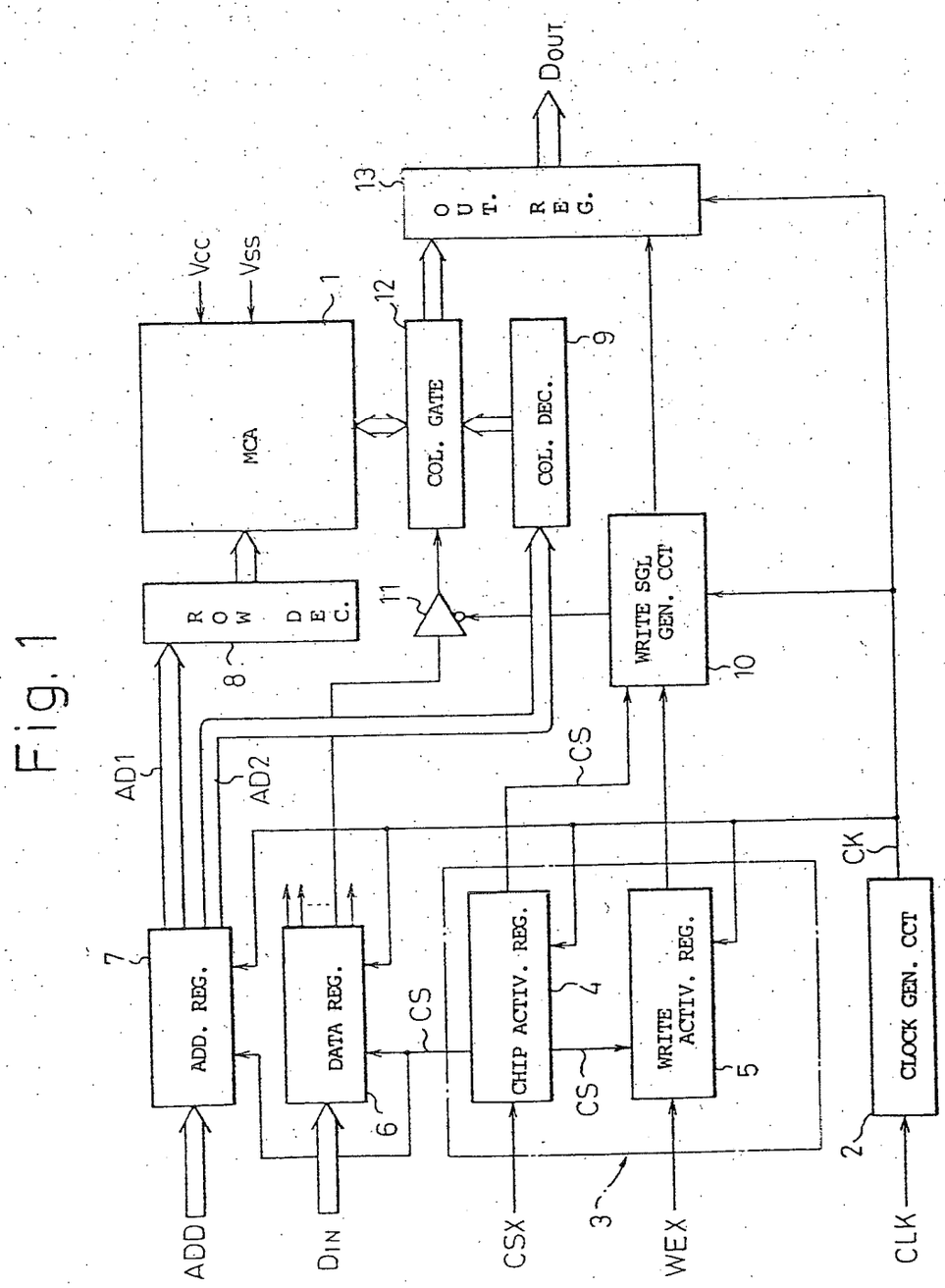

DOUT
OUT. REG.
13
VCC
VSS
MCA
1
COL. GATE
12
COL. DEC.
9
ROW DEC.
8
11
WRITE SGL GEN. CCT
10
AD1
AD2
CS
CK
ADD. REG.
7
DATA REG.
6
CHIP ACTIV. REG.
4
WRITE ACTIV. REG.
5
CLOCK GEN. CCT
2
ADD
DIN
CSX
3
WEX
CLK

Fig. 1

Fig. 2

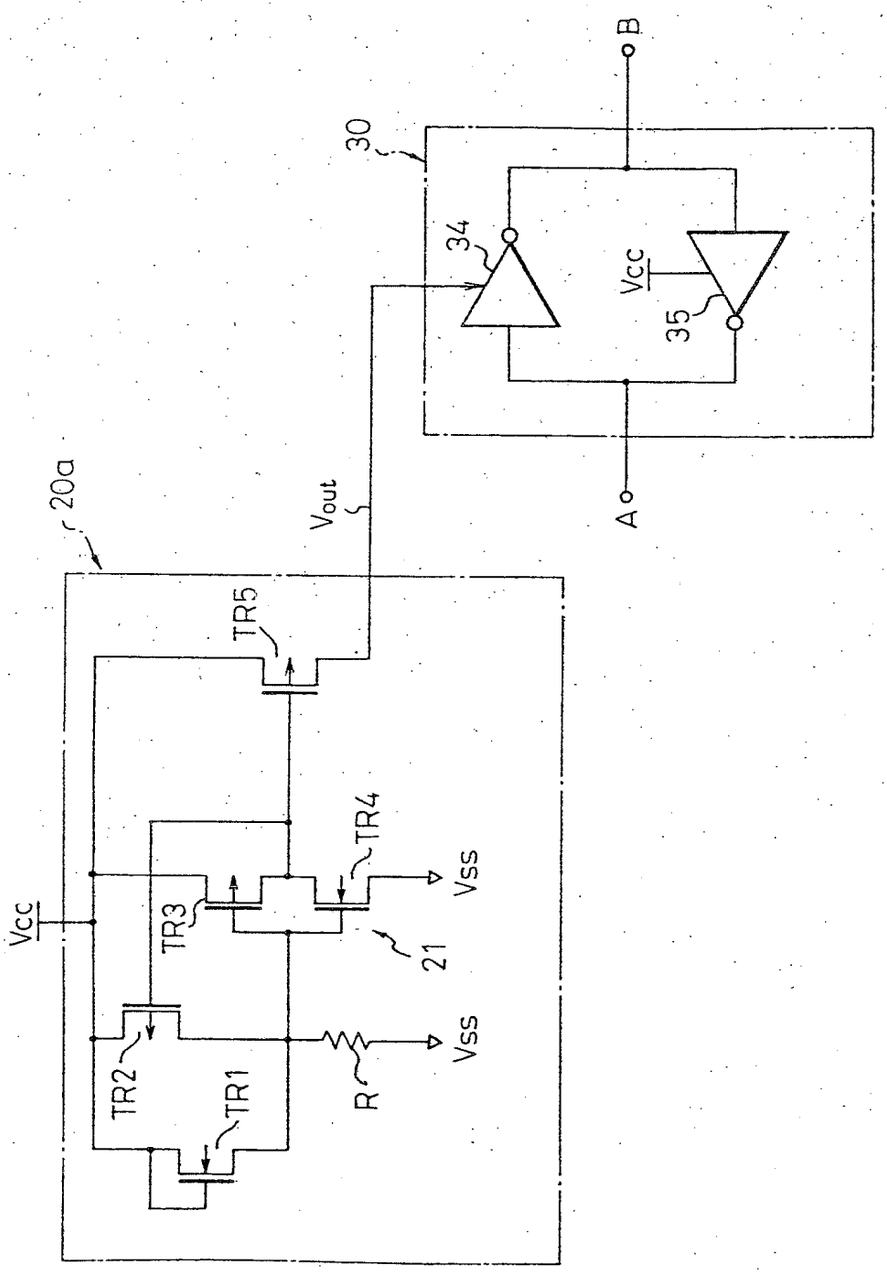


Fig. 3

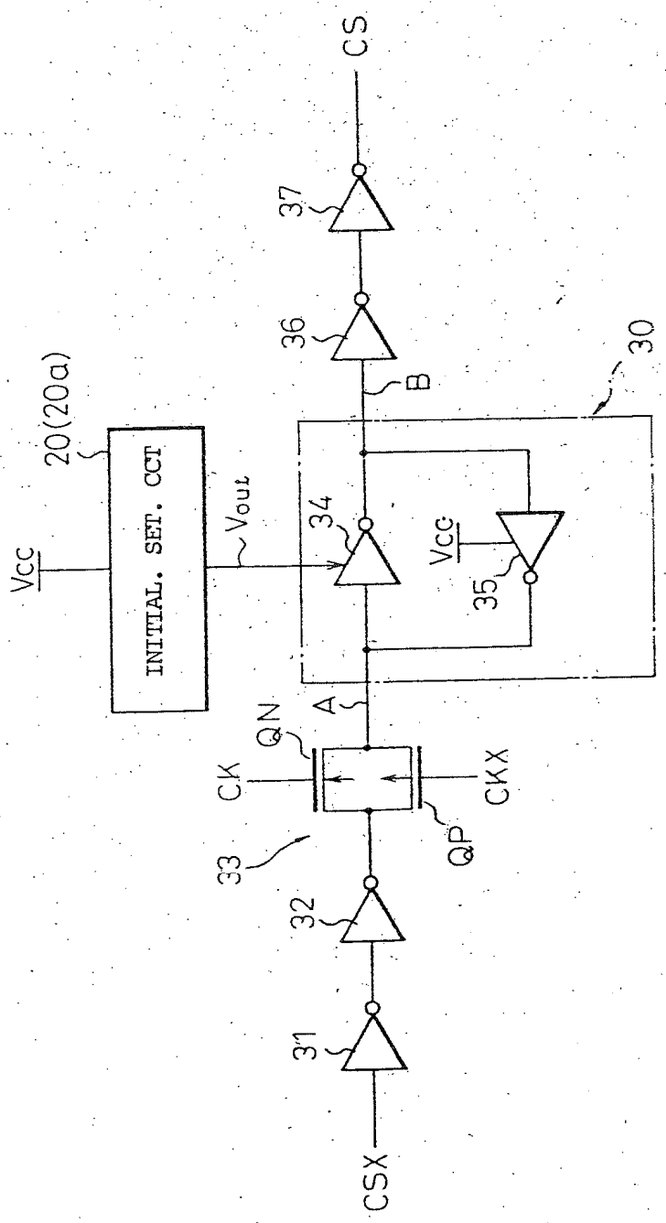

CS
37
36
B
30
20(20a)
INITIAL. SET. CCT
Vout
Vcc
34
Vcc
35
A
QN
CK
CKX
QP
33
32
31
CSX

Fig.5

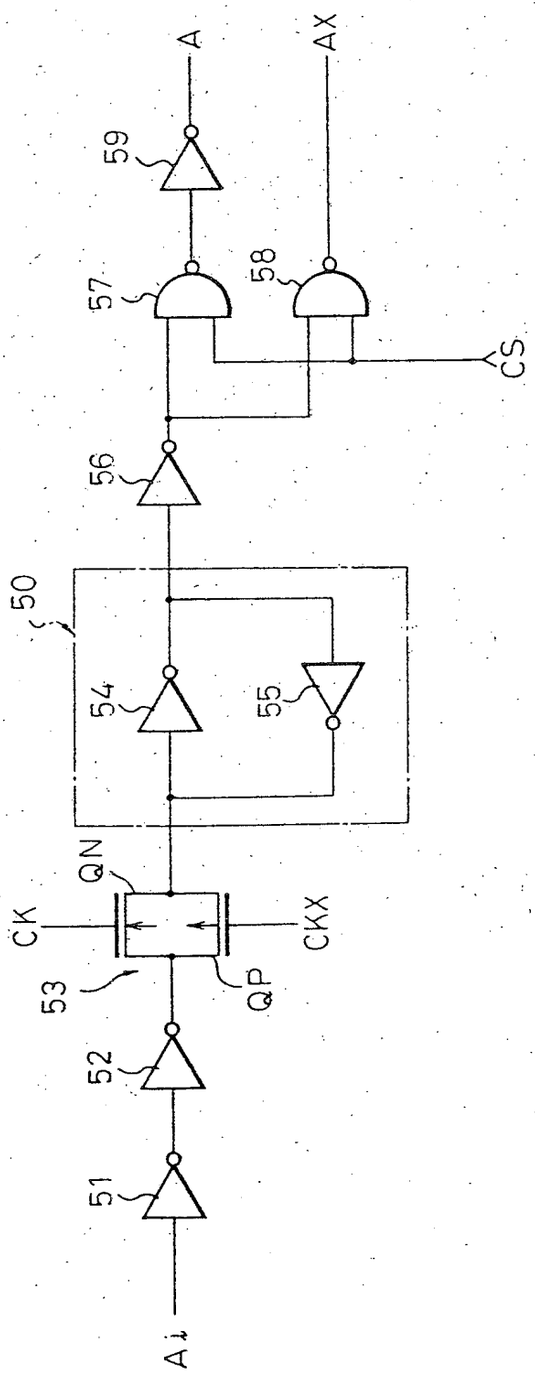


Fig. 6

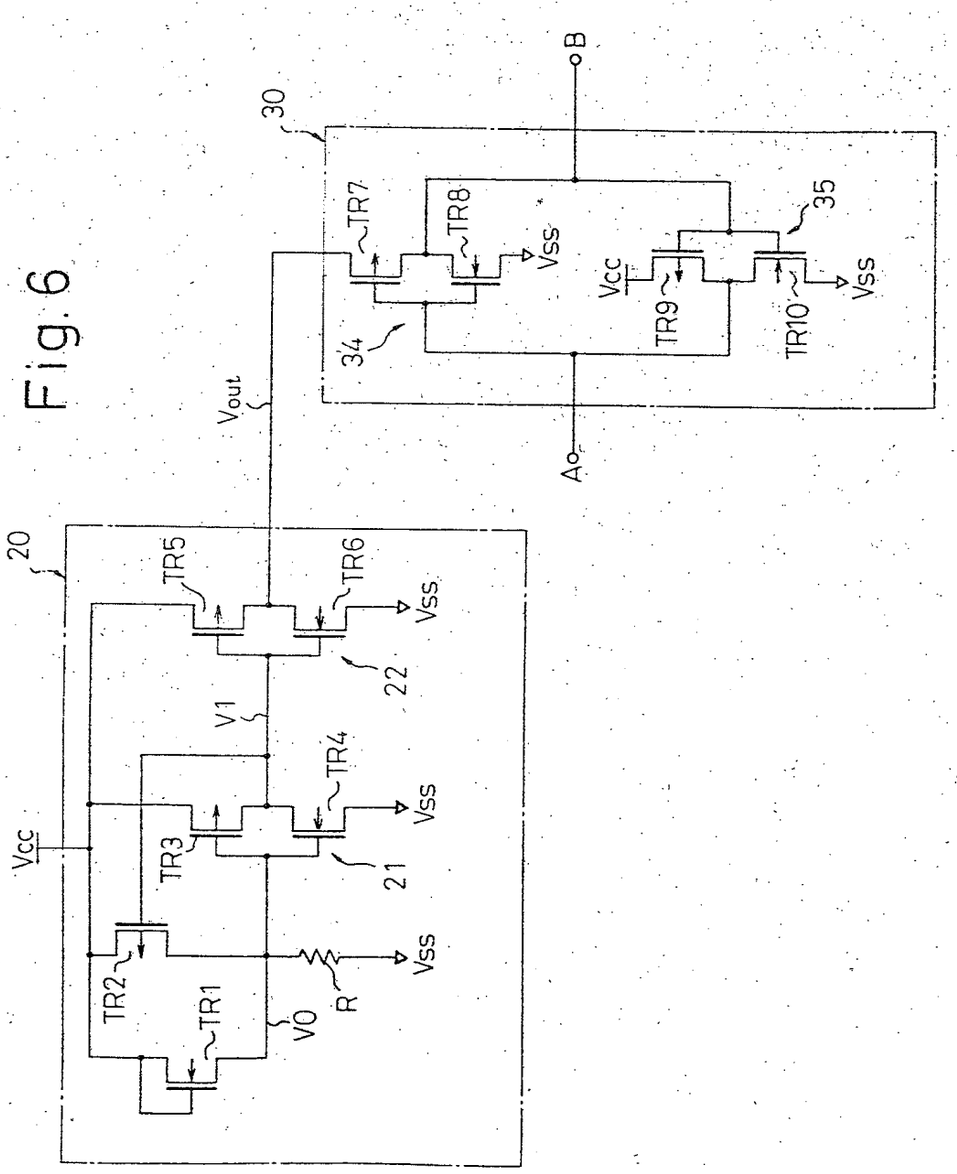

B
30
TR7
TR8
Vss
Vcc
TR9
35
TR10
Vss
34
Vout
A
20
TR5
TR6
Vss
22
V1
TR4
Vss
Vcc
TR3
21
TR2
TR1
V0
R
Vss

Fig. 7

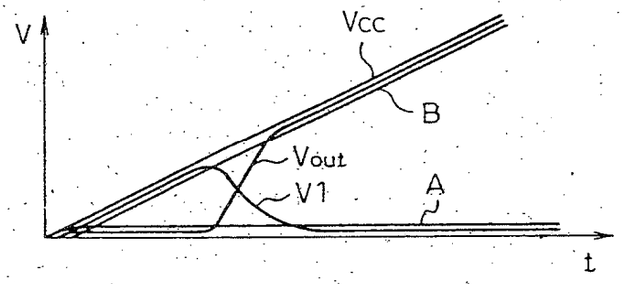


Fig. 8

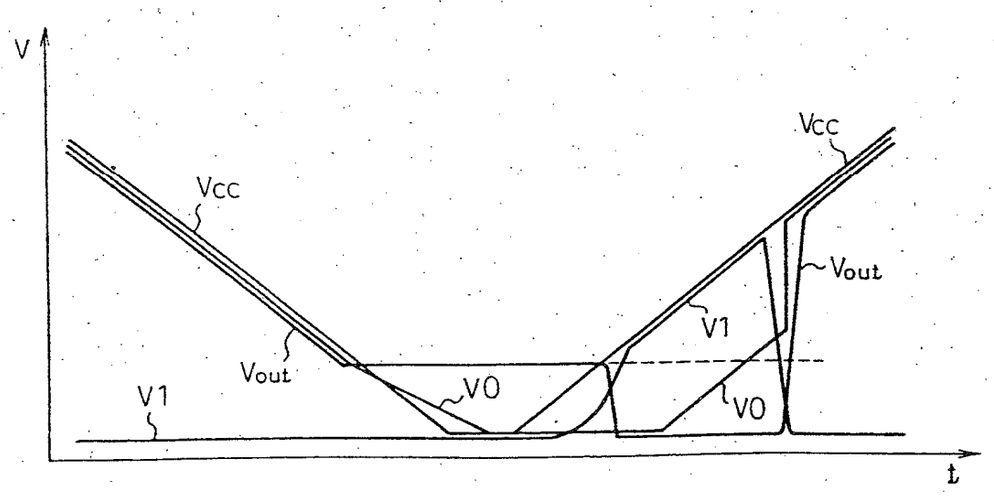
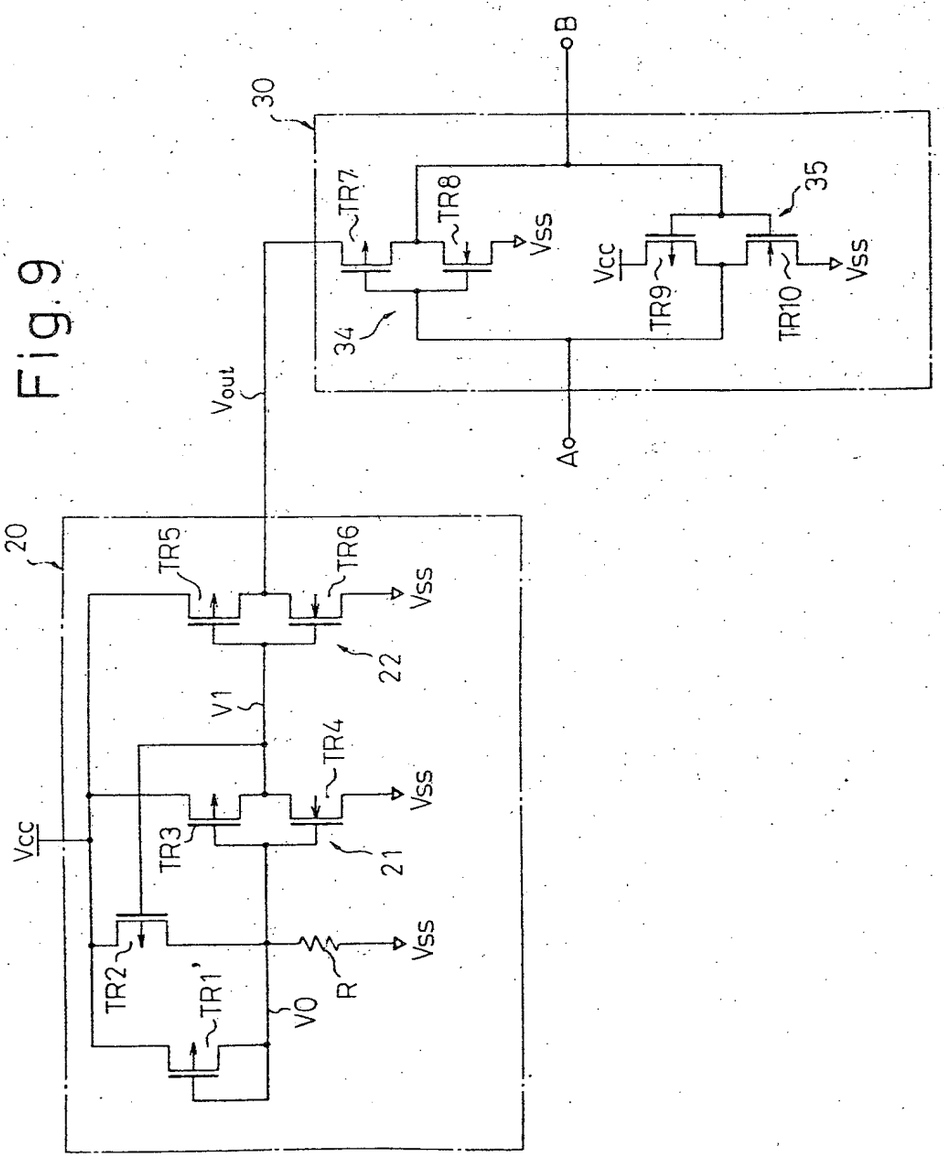


Fig. 9


B
30
TR7
TR8
Vss
Vcc
TR9
35
TR10
Vss
34
A
Vout
20
TR5
TR6
Vss
22
V1
TR4
Vss
Vcc
TR3
21
Vss
TR2
TR1'
V0
R

INITIALIZATION SETTING CIRCUIT AND SEMICONDUCTOR MEMORY DEVICE USING THE SAME

FIELD OF THE INVENTION

The present invention relates to a circuit for setting an initial condition of a latch circuit for holding operational conditions of respective circuits in a semiconductor device upon ON-set of power supply, and more particularly, to an improvement for an initialization setting circuit for setting initial conditions of a latch circuit that holds information, such as addresses, control signals, data and so forth in a semiconductor memory device, upon ON-set of power supply.

A latch circuit is provided in a semiconductor memory device, for example, for latching operational conditions of respective circuit. An initialization setting circuit is typically connected to the latch circuit for setting initial condition upon ON-set of the power supply.

BACKGROUND ART

In the conventional semiconductor memory device, as in the construction shown in FIG. **1**, for example, an external address signal Add is input to a row decoder **8** and a column decoder **9** as respective row address signal AD1 and column address signal AD2, through an address register **7**. Respective decoders produce decode signals based on respective address signals to select a memory cell of the corresponding address in a memory cell array **1**, and writing and reading of data is performed.

In this case, the address register **7** receives an activation signal CS from a chip activation register **4** to control the transmission of the address signal ADD for the internal circuit. The activation signal CS is generated, when reference is made to the construction in FIG. **3**, by a chip activation register on the basis of a chip selection signal CSX of an active row, the chip selection signal of which is supplied externally. In this case, the chip selection signal CSX is input to a latch circuit **30** formed by two inverters **34** and **35** connected in a reverse parallel relationship, through two stage inverters **31** and **32** and a transfer gate **33**, and is further output as the activation signal CS through two stage inverters **36** and **37**. In this construction, when the chip selection signal CSX is "H" level, an "H" level signal is input to the latch circuit **30** and a "L" level signal is output from the latch circuit **30**. Therefore, the activation circuit CS becomes "L" level to maintain the address register **7** in an inactive state. Conversely, when the chip selection signal CSX is "L" level, since a "H" level signal is output from the latch circuit **30**, the activation signal CS becomes "H" level to activate the address register **7**.

On the other hand, for one of the inverter **34** of the latch circuit, a power source voltage Vout is supplied from an initialization setting circuit **20***a* which will be discussed later (see FIG. **3**). For the other inverter **35**, power source voltage Vcc is directly supplied from a high potential power source line (not shown) similarly to other circuits. Upon ON set of power (Vcc) supply for such semiconductor memory device, by an operation of the initialization setting circuit **20***a*, the power source voltage Vout is supplied to the inverter **34** with a delay from the supply of the power source voltage Vcc for the inverter **35**. Therefore, upon ON-set of the power supply, because of the operation of the inverter **35** in advance of initiation of the operation of the inverter **34** in the latch circuit **30**, the potential at the input terminal A of the latch circuit **30** becomes "H" level, and by this operation of the inverter **35**, the output signal of the latch circuit **30** is latched at "H" level after the power supply for the inverter **34**.

FIG. **2** shows one example of construction of the above-mentioned initialization setting circuit **20***a*.

In this figure, for the input terminal of a CMOS inventer **21** (p channel transistor TR3 and n channel transistor TR4), the source of an n channel transistor TR1 is connected. The drain and the gate of the n channel transistor TR1 are connected to a high potential power source line Vcc. On the other hand, to the input terminal of the inverter **21**, the drain of a p channel transistor TR2 is connected, which has the source connected to the power source line Vcc, and the gate connected to the output terminal of the inverter **21**. Further, a resistor R is disposed between the input terminal of the inverter **21** and a low potential power source line Vss. On the other hand, the output terminal of the inverter **21** is output to the gas of a p channel transistor TR5, the transistor of which has the source connected to the power source line Vcc, and the drain connected to the output terminal (output voltage Vout) of the initialization setting circuit **20***a*.

When the power source Vcc is allied to the initialization circuit **20***a* constructed as set forth above, a voltage lower than the power source voltage Vcc by a magnitude corresponding to the threshold level (VthN) of the transistor TR1, is applied to the input terminal of the inverter **21**. Subsequently, after a given period from the rise of the power source voltage Vcc, the inverter **21** makes a decision for "H" level for the level of (Vcc−VthN) to output a "L" level output signal to the transistor TR5. By this, the transistor TR5 is turned ON to output the output signal Vout equal to the power source voltage Vcc at the output terminal. On the other hand, at the same time, the transistor TR2 is turned ON to maintain the level at the input terminal of the inverter **21** at "H" level.

Accordingly, the initialization setting circuit **20***a* is responsive to ON-set of the power supply voltage Vcc and outputs the output signal Vout more rapidly than the power source voltage Vcc at the output terminal with a given period of delay from ON-set. Through the operation set forth above, the power supply for the inverter **34** of the latch circuit **30** is slightly delayed.

However, in the initialization setting circuit **20***a* as set forth above, a problem will be arise when power source voltage Vcc is shut down at the condition in which the voltage Vout is supplied to the inverter **34** of the latch circuit **30** from the output terminal by ON-set of the power supply (namely, the condition that the signal line connected to the drain of the transistor TR5 is charged at a level substantially corresponding to the power source voltage Vcc).

Namely, the charge accumulated at the output terminal cannot be discharged, and as a result, the voltage level (level of the output signal Vout) at the output terminal is floating at an intermediate level. Accordingly, if power source voltage Vcc is again applied to respective circuits, due the level of the output signal Vout (intermediate level) of the initialization setting circuit **20***a*, the inverters **34** and **35** of the latch circuit **30** start operation simultaneously. As a result, it becomes possible that the potential at the output terminal B of the latch circuit **30** becomes "H" level. Therefore, the prob-

lem of malfunction can arise upon writing in and reading out data.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an initialization setting circuit that assures initialization of the operation again upon setting the power supply ON when the power source voltage is shut down, and thus can prevent malfunction.

In order to accomplish the above-mentioned object, there is provided an initialization setting circuit according to the present invention that is adapted to set an initial condition of a latch circuit in a semiconductor device upon ON-set of the power supply, comprising a detecting circuit responsive to ON-set of the power supply to detect the power source voltage reaching a given voltage, and an output level control circuit responsive to the detecting signal output from the detecting circuit, for elevating the level of an output signal of the initialization setting circuit to a high potential level or pulling down the level of the output signal of the initialization setting circuit to a low potential level, the output signal controlled by said output level control circuit being supplied to the latch circuit as the power source voltage.

With the construction set forth above, the output level control circuit can pull-up the output signal level of the initialization setting circuit rapidly to a high potential level with a delay from a rising of the power source voltage, upon ON-set of the power source voltage. Also, upon shutting of the power source voltage, the output signal level of the initialization setting circuit can be rapidly pulled down to the low potential level. Accordingly, when the power source voltage is shut down, the operation of the latch circuit can be certainly initialized and thus make it possible to prevent malfunction of the ON setting power supply.

It should be noted that other features and functions of the present invention will be discussed herebelow in detail with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram showing construction of a semiconductor memory device according to the present invention;

FIG. **2** is a circuit diagram showing one example of the conventional initialization setting circuit;

FIG. **3** is a circuit diagram showing construction of a chip activation register in FIG. **1**;

FIG. **4** is a circuit diagram showing the construction of a writing activation register or data register in FIG. **1**, which illustrates a part for one bit;

FIG. **5** is a circuit diagram showing the construction of an address register of FIG. **1**, which illustrates a part for one bit;

FIG. **6** is a circuit diagram showing the construction of one embodiment of the initialization setting circuit according to the present invention;

FIG. **7** is a chart showing a signal waveform illustrating operation of the circuit of FIG. **6** upon ON-set of the power supply;

FIG. **8** is a chart showing signal waveform illustrating the operation of the circuit of FIG. **6** upon setting the On power supply after shutting down the power supply; and

FIG. **9** is a circuit diagram of another embodiment of the initialization setting circuit according to the present invention.

BEST MODE FOR IMPLEMENTING THE INVENTION

Hereafter, the practical embodiments of the present invention will be discussed with reference to FIGS. **1** and **3** to **8**.

FIG. **1** shows the construction of one embodiment of a semiconductor memory device according to the present invention.

The shown device is a so-called self-timed random-access-memory (self-timed RAM) adapted to perform a necessary memory operation with internal synchronization by clock with respect to externally entered asynchronous data, address signal and various control signals.

In this figure, the reference numeral **1** denotes a memory cell array, **2** denotes a clock generator circuit for generating synchronization clock signal CK for internal use on the basis of an external clock signal CLK, **3** denotes a control register. The control register includes a chip activation register **4** that receives an externally entered chip selection signal CSX of the active row in response to the clock signal to generate an activation signal CS and a write activation register **5** that receives an externally entered write enabling signal WEX of active row in response to the clock signal and is controlled by the activation signal CS. The reference numeral **6** denotes a data register that receives externally entered data DIN in response to the clock signal and is controlled by the activation signal CS, **7** denotes an address register that receives an externally entered address signal ADD in response to the clock signal and is controlled by the activation signal CS.

On the other hand, the reference numeral **8** denotes a row decoder that decodes row address signal AD1 output from the address register and selects one of word lines (not shown) in a memory cell array **1**, **9** denotes a column decoder that decodes column address signal AD2 output from the address register **7** and selects one of bit lines in the memory cell array **1**, **10** denotes a write-in signal generating circuit for generating a write-in signal based on the activation signal CS from the register **4** and the write enabling signal from the register, in response to the clock signal CK, **11** denotes a try state buffer for controlling passing and blocking output of the data register **6** depending upon the logical level of the write-in signal, **12** denotes a column gate connecting the selected column line to a data line (output line of the try state buffer and input line of an output register **13**), **13** denotes the output register for externally outputting the data output through the column gate **12** as an output (D00T) in response to the write-in signal and the clock signal CK.

FIG. **3** shows a circuit construction of the check activation register **4**.

The shown circuit includes an inverter **31** responsive to the externally entered chip selection signal CSX, an inverter **32** responsive to the output of the inverter, a transfer gate **33** that comprises an n channel transistor QN and a p channel transistor QP and controls transmission and blocking of the output of the inverter **32** in response to the clock signal CK or an inverted signal thereof, a latch circuit **30** composed of two inverters **34** and **35** arranged in reverse parallel connection, an initialization setting circuit **20** for supplying a power source voltage Vout for the inventer **34** in the latch circuit, an inverter **36** responsive to the output of the latch circuit **30**, and an inverter **37** generating the acti-

vation signal CS in response to the output of the inventer.

FIG. 4 shows the circuit construction of the write-in activation register 5 (or data register 6 in a part for one bit).

The shown circuit includes an inverter 41 responsive to an external write enabling signal WEX (or data D), an inverter 42 responsive to the output of the inverter, a transfer gate comprising an n channel transistor QN and a p channel transistor QP in parallel connection to each other and controlling the transmission and blocking of output of the inverter 42 in response to the clock signal CK or the inverted signal CKX thereof, a latch circuit 40 comprising two inverters 44 and 45 in reverse parallel connection, an inverter 46 responsive to the output of the latch circuit, a NAND gate 47 responsive to the output of the inverter and the activation signal CS, and an inverter 48 outputting the write enabling signal WEX (or data D) in response to the output of the NAND gate.

FIG. 5 shows a circuit construction of an address register 7 for one bit.

The shown circuit includes an inverter 51, an inverter 52 responsive to the output of the inverter, a transfer gate comprising an n channel transistor QN and a p channel transistor QP in parallel connection to each other and controlling transmission and blocking of output of the inverter 52 in response to the clock signal CK or the inverted signal CKX thereof, a latch circuit 40 comprising two inverters 4 and 55 of reverse parallel connection, an inverter 6 responsive to the output of the latch circuit, a NAND gate responsive to the output of the inverter and the activation signal CS, a NAND gate responsive to the output of the inverter 56 and the activation signal CS to output an inverted address bit AX, an inverter 59 responsive to the output of the NAND gate 7 for outputting an address bit A.

FIG. 6 shows the circuit construction of the initialization setting circuit (see FIG. 3), which is a particular feature of the present invention.

As shown in this figure, the shown embodiment of the initialization setting circuit 20 is constructed by connecting an n channel transistor TR6 that is connected between the drain of the transistor TR5 and a power source line Vss and responsive to the output signal V1 of the inverter 21, to the p channel transistor TR5 of the conventional initialization setting circuit 20*a* (see FIG. 2) so as to form CMOS inventer 22, and supplies the output Vout of this inverter 22 to one of the inverters 34 of the latch circuit 30 as the power source voltage.

With this construction, by utilizing the n channel transistor TR1 as an enhancement type, the bias effect of the substrate is utilized. In the shown embodiment, the threshold level (approximately 1.5 to 2V) of the transistor is set to be higher than the threshold level (approximately 1V or more or less) of the p channel transistor TR3. On the other hand, for the resistor R, a substantially higher resistance value of several MΩ is provided.

In FIG. 7, there is illustrated signal waveforms at various portions in the initialization setting circuit 20 of FIG. 6, upon ON-set of the power supply.

Consideration is given to the fact that the output terminal of the shown embodiment of the initialization setting circuit (output signal Vout) is connected to one of the inverters 34 of the latch circuit 30 similarly to the prior art, and the power source voltage Vcc is applied to the initialization setting circuit 20 and the latch circuit 30.

When the power source voltage Vcc exceeds a predetermined level, the gate potential (voltage V0) of the n channel transistor TR4 of the inverter 21 via the transistor TR1 becomes higher than or equal to the threshold level to turn the transistor TR4 ON and thus turns the output signal V1 of the inventer into a "L" level signal. Subsequently, by this output signal V1, the p channel transistor TR5 of the inverter 22 is turned ON so that the output signal Vout of the inverter 22 is rapidly elevated to the level of the power source voltage Vcc. The output signal Vout is supplied to the inverter 34 of the latch circuit 30 as the power source voltage.

On the other hand, at the latch circuit, associated with ON-set of the power source voltage Vcc, the inverter 35 initiates an operation to elevate the level at the input terminal A of the latch circuit 30 to "H" level, i.e. the power source voltage Vcc, and latched at this condition. Accordingly, upon ON-set of the power supply, it operates in the same manner as the prior art.

FIG. 8 shows the signal waveform at various portions of the initialization setting circuit of FIG. 1, upon shutting down of the power source and subsequent ON-set again.

When the power source voltage Vcc for the initialization setting circuit 20 and the latch circuit 30 is shut down, the source potential (voltage V0) of the transistor TR1 and the potential of the output signal Vout lowers gradually according to the lowering of the power source voltage Vcc. When the power source voltage Vcc is lowered to a given level (the threshold level of the p channel transistor TR5 of the inventer 22), the output signal Vout maintains the instantaneous level thereafter. On the other hand, with respect to the input voltage (voltage V0) of the inverter 21, according to a voltage drop at the resistor, the potential is lowered gradually.

When the power supply is resumed after lowering the power source voltage Vcc across the above-mentioned given level, since the threshold level of the transistor TR3 is lower than the threshold level of the transistor TR1, the transistor TR3 is turned ON earlier. By this, the output signal V1 of the inverter 21 rises to the level of the power source voltage Vcc. By this, the n channel transistor TR6 of the inverter 22 is turned ON to lower the output signal Vout to "L" level.

At this time, as shown by a broken line in this figure, the output signal Vout in the prior art is floating at the intermediate level instead of being lowered to the "L" level. However, with the construction of this embodiment, the charge accumulated at the output terminal (output signal Vout) is drawn to the power source line Vss by turning ON the n-channel transistor TR6 of the inverter 22, and therefore, the output signal Vout attains "L" level.

As set forth, in the construction of the shown embodiment of the initialization setting circuit 20, by a power supply for the inverter 34 of the latch circuit, the ON-set of the power supply is delayed, the initial output signal of the latch circuit becomes a "L" level signal, and upon shutting down of the power supply, the output signal Vout is lowered to the "L" level by the operation of the inverter 22 (n channel transistor TR6) to prevent outputting of erroneous signals from the latch circuit 30 and so forth, upon re-setting of the power supply.

It should be noted that in the shown embodiment, upon ON-set of the power source voltage Vcc after once shutting down, the level of the output signal Vout is lowered to "L" level. This is for the following reason.

Namely, the timing to lower the output signal level to "L" level by turning ON the n channel transistor TR6 of the inventer appears to be able to shut down the power supply. However, in view of the capacity of the output signal (Vout) line, it is necessary to add an element, such as a resistor for drawing the charge on the line, and the value of the additional element has to be varied according to the condition of the circuit. The adjustment should become cumbersome.

However, according to the shown embodiment, the desired task can be achieved solely by adding the n channel transistor TR6.

On the other hand, although the initialization setting circuit 20 is provided only for the latch circuit 30 in the chip activation register 4 in the foregoing embodiment, such initialization setting circuit can also be applied for the write-in activation register 5, the data register 6 or the address register 7.

Furthermore, although the foregoing embodiment employs the n channel transistor TR1 as the element for outputting voltage Vo that is lower than the power source voltage Vcc by a given magnitude, it can be replaced with p channel transistor TR1" as shown in FIG. 9. It is clear that the substantially equivalent effect can be expected. In addition, although the foregoing discussion is given for the application of the shown embodiment of the initialization setting circuit for the self-timed ransom-access-memory, the initialization setting circuit according to the present invention is not limited to the specific application. For example, it is equally applicable for semiconductor devices which have latch circuits at the input stages.

We claim:

1. An initialization setting circuit for setting an initial state of a latch circuit in a semiconductor device upon ON-set of power supply, comprising:

a detecting circuit active in response to ON-set of power supply for detecting power source voltage reaching a predetermined level; and

an output level controlling circuit responsive to a detecting signal output from said detecting circuit for elevating an output signal of the initialization setting circuit to a high potential level, or to pull down the output signal to a low potential level,

the output signal controlled by said output level controlling circuit being supplied to said latch circuit as the power source voltage.

2. An initialization setting circuit as set forth in claim 1, wherein said detecting circuit is active in response to ON-set of the power supply and includes a semiconductor element that outputs a voltage that has a level lower than said power source voltage by a predetermined threshold level, an inverter receiving said power source voltage and responsive to an output voltage of said semiconductor element, and a voltage holding circuit for maintaining a level relationship of the output voltage of said semiconductor element relative to the threshold level of said inverter after ON-set of the power supply.

3. An initialization circuit as set forth in claim 2, wherein said output level controlling circuit comprises a first CMOS inverter including a p channel transistor and a n channel transistor connected between a power source line of high potential and a power source line of low potential.

4. An initialization setting circuit as set forth in claim 3, wherein the inverter responsive to the output voltage of said semiconductor element comprises a second CMOS inverter including a p channel transistor and a n channel transistor connected between the high potential power source line (Vcc) and the low potential power source line.

5. An initialization setting circuit as set forth in claim 4, wherein said semiconductor element is an enhancement type n channel transistor and the gate of the transistor is connected to the drain thereof.

6. An initialization setting circuit as set forth in claim 4, wherein said semiconductor device is a p channel transistor, and the gate of the transistor is connected to the drain thereof.

7. An initialization setting circuit as set forth in claim 5, wherein the threshold level of said enhancement type n channel transistor is set higher than the threshold level of the p channel transistor of said second CMOS inventer.

8. An initialization setting circuit as set forth in claim 7, wherein said voltage holding circuit comprises a p channel transistor connected between said high potential power source line and the input terminal of said second CMOS inverter and a resistor connected between said input terminal of said second CMOS inverter and said low potential power source line; said p channel transistor being responsive to the output voltage level of said second CMOS inverter to be turned ON and OFF to maintain the input voltage level of said second CMOS inverter.

9. A semiconductor memory device comprising:

a memory cell array;

a circuit for generating a clock signal for synchronization of operations of respective internal circuits;

register means receiving an external address signal, data and control signal in response to said clock signal, and including latch means for maintaining the received state and an initialization setting means for setting the initial state of said latch means upon ON-set of power supply;

peripheral circuit for controlling access of memory and reading and writing of data out and in said memory cell array on the basis of said address signal, data and control signal input through said register;

said initialization setting means comprising:

a detecting circuit active in response to ON-set of power supply for detecting a power source voltage reaching a predetermined level; and

an output level controlling circuit responsive to a detecting signal output from said detecting circuit for elevating an output signal of the initialization setting circuit to a high potential level, or to lowering the output signal to a low potential level,

the output signal controlled by said output level controlling circuit being supplied to said latch circuit as the power source voltage.

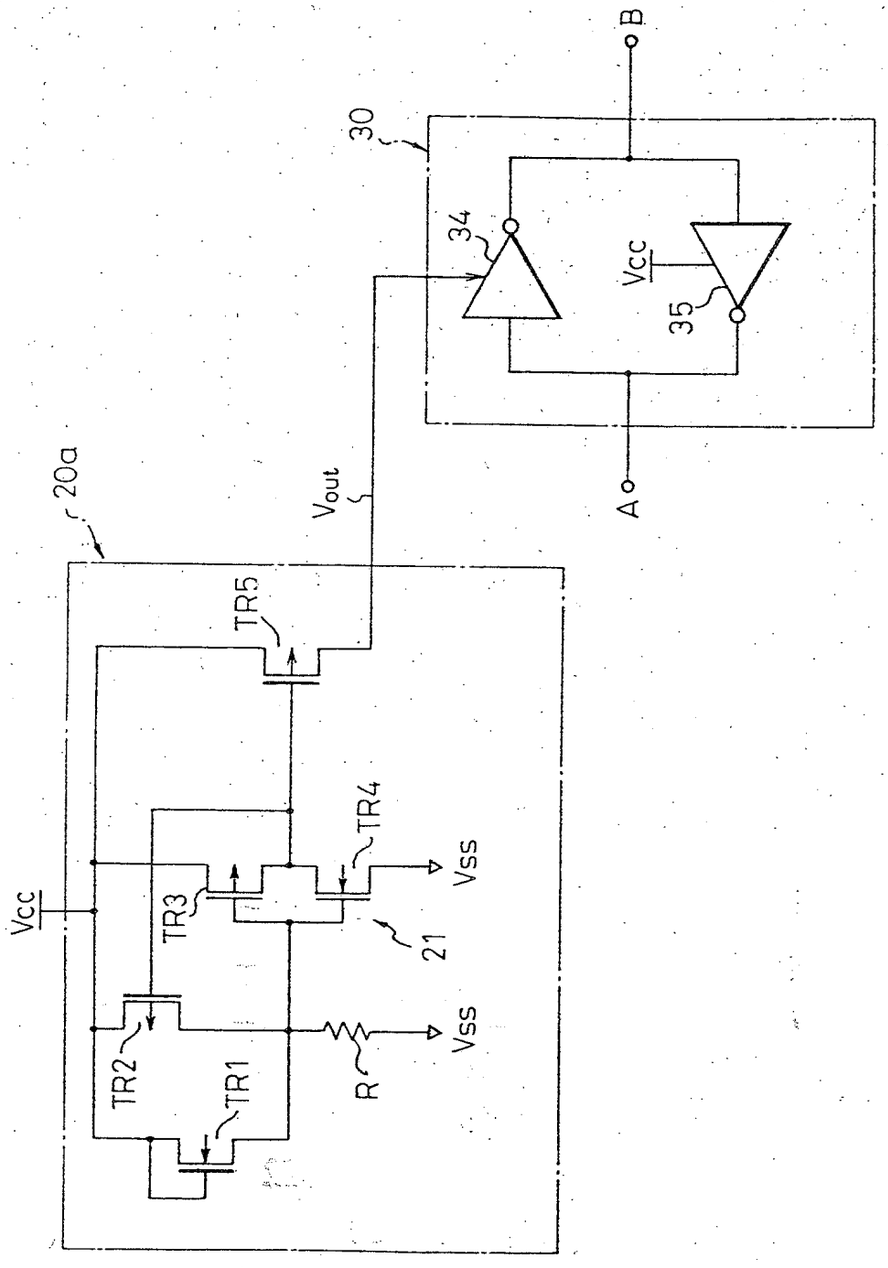
10. A semiconductor memory device as set forth in claim 9, wherein said detecting circuit is active in response to ON-set of power supply and includes a semiconductor element that outputs a voltage that has a level lower than said power source voltage by a predetermined threshold level, an inverter receiving said power source voltage and responsive to an output voltage of said semiconductor element, and a voltage hold-

ing circuit for maintaining a level relationship of the output voltage of said semiconductor element relative to the threshold level of said inverter after ON-set of the power supply.

11. A semiconductor memory device as set forth in claim **10**, wherein said register means includes a plurality of registers respectively provided corresponding to said external address signal, data and control signal, each of a plurality of said registers has said latch means, and at least one of a plurality of said registers includes said initialization setting circuit.

* * * * *

Fig. 2



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By:_____ Date: September 27, 1999

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Gunnar Krause
Appl. No.	:	09/343,431
Filed	:	June 30, 1999
Title	:	Dynamic Semiconductor Memory Device And Method For Initializing A Dynamic Semiconductor Memory Device

CLAIM FOR PRIORITY

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

Claim is hereby made for a right of priority under Title 35, U.S. Code, Section 119, based upon the German Patent Application 198 29 287.2 filed June 30, 1998.

A certified copy of the above-mentioned foreign patent application is being submitted herewith.

Respectfully submitted,

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BUNDESREPUBLIK DEUTSCHLAND

Bescheinigung

Die Siemens Aktiengesellschaft in München/Deutschland hat eine Patentanmeldung unter der Bezeichnung

"Dynamische Halbleiter-Speichervorrichtung und Verfahren zur Initialisierung einer dynamischen Halbleiter-Speichervorrichtung"

am 30. Juni 1998 beim Deutschen Patent- und Markenamt eingereicht.

Die angehefteten Stücke sind eine richtige und genaue Wiedergabe der ursprünglichen Unterlagen dieser Patentanmeldung.

Die Anmeldung hat im Deutschen Patent- und Markenamt vorläufig die Symbole G 11 C und G 06 F der Internationalen Patentklassifikation erhalten.

München, den 22. Juni 1999
Deutsches Patent- und Markenamt
Der Präsident
Im Auftrag

Aktenzeichen: 198 29 287.2

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Beschreibung

Bezeichnung der Erfindung: Dynamische Halbleiter-Speichervorrichtung und Verfahren zur Initialisierung einer dynamischen Halbleiter-Speichervorrichtung

Die Erfindung betrifft eine dynamische Halbleiter-Speichervorrichtung vom wahlweisen Zugriffstyp (DRAM/SDRAM) mit einer den Einschaltvorgang der Halbleiter-Speichervorrichtung und ihrer Schaltungsbestandteile steuernden Initialisierungsschaltung, welche nach einer nach dem Einschalten der Halbleiter-Speichervorrichtung erfolgten Stabilisierung der Versorgungsspannung ein Versorgungsspannungsstabilsignal (POWERON) liefert, ein Verfahren zur Initialisierung einer solchen dynamischen Halbleiter-Speichervorrichtung, sowie die Verwendung einer ein Freigabesignal liefernden Freigabeschaltung zur Steuerung des Einschaltvorganges einer dynamische Halbleiter-Speichervorrichtung.

Bei SDRAM-Halbleiterspeichern nach dem JEDEC-Standard ist während des Einschaltvorganges ("POWERUP") dafür zu sorgen, dass die internen, für den ordnungsgemäßen Betrieb der Halbleiter-Speichervorrichtung vorgesehenen Steuerschaltungen sicher in einem definierten Sollzustand gehalten werden, um eine unerwünschte Aktivierung von Ausgangstransistoren zu verhindern, die auf den Datenleitungen einen Kurzschluss (sogenannte "Bus Contention" bzw. "Data Contention") oder eine unkontrollierte Aktivierung von internen Stromverbrauchern hervorrufen würde. Aufgrund einer prinzipiellen Unvorhersehbarkeit des zeitlichen Verlaufes der Versorgungsspannung und des bzw. der Spannungspegel an den externen Steuereingängen während des Einschaltvorganges des Halbleiter-Speichers gestaltet sich die Lösung dieses Problems schwierig. Nach den Herstellerspezifikationen sollte ein SDRAM-Bauelement sämtliche Befehle, die zeitlich vor einer definierten Initialisierungs-

abfolge anliegen, ignorieren. Diese Abfolge besteht aus vorbestimmten Kommandos, die in einer definierten zeitlichen Reihenfolge angelegt werden müssen. Eine Reihe von Funktionen und Kommandos, die im ordnungsgemäßen Betrieb des Bauelementes erlaubt sind, sind jedoch zeitlich erst nach der Initialisierungsabfolge erwünscht bzw. erlaubt. Nach dem JEDEC-Standard für SDRAM-Halbleiter-Speicher ist eine empfohlene Initialisierungsabfolge (sogenannte "POWERON-SEQUENCE") wie folgt vorgesehen:

1. Anlegen eines Versorgungsspannungs- und Startimpulses, um die Aufrechterhaltung einer NOP-Bedingung bei den Eingängen des Bauelementes zu erzielen.

2. Aufrechterhaltung einer stabilen Versorgungsspannung, eines stabilen Taktes, und von stabilen NOP-Eingangsbedingungen für eine Mindestzeitdauer von 200 µs.

3. Vorbereitungskommando für die Wortleitungsaktivierung (PRECHARGE) für sämtliche Speicherbänke der Vorrichtung.

4. Aktivierung von acht oder mehreren Auffrischungskommandos (AUTOREFRESH).

5. Aktivierung des Lade-Konfigurations-Register-Kommandos (MODE-REGISTER-SET) zur Initialisierung des Modusregisters.

Nach dem Erkennen einer solchen definierten Initialisierungsabfolge befindet sich der Speicherbaustein normalerweise in einem sogenannten IDLE-Zustand, d.h. er ist vorgeladen und für den ordnungsgemäßen Betrieb vorbereitet. Bei den bisher bekannt gewordenen SDRAM-Halbleiter-Speicherbausteinen wurden sämtliche Steuerschaltungen des Bauelementes lediglich mit dem POWERON-Signal entriegelt. Dieses Signal POWERON ist aktiv, wenn die internen Versorgungsspannungen die erforderli-

chen Werte erreicht haben, die zum ordnungsgemäßen Betrieb des Bauelementes erforderlich sind. Danach ist der Baustein in der Lage, Befehle anzuerkennen und auszuführen.

Der Erfindung liegt die Aufgabe zugrunde, eine konstruktiv möglichst einfache Verbesserung der Steuerung des Einschaltvorganges bei dynamischen Halbleiter-Speichervorrichtungen vom wahlweisen Zugriffstyp (DRAM oder SDRAM) anzugeben, mit welcher die Gefahr eines Kurzschlusses der Datenleitungen und/oder einer unkontrollierten Aktivierung von internen Stromverbrauchern wirksam verhindert wird.

Diese Aufgabe wird durch eine dynamische Halbleiter-Speichervorrichtung vom wahlweisen Zugriffstyp nach Anspruch 1, ein Verfahren zur Initialisierung einer solchen Halbleiter-Speichervorrichtung nach Anspruch 11, sowie durch die Verwendung einer ein Freigabesignal (CHIPREADY) liefernden Freigabeschaltung zur Steuerung des Einschaltvorganges einer derartigen Halbleiter-Speichervorrichtung nach Anspruch 14 gelöst.

Erfindungsgemäß ist vorgesehen, dass die Initialisierungsschaltung eine dem Versorgungsspannungsstabilsignal und weiteren, von außen an die Halbleiter-Speichervorrichtung angelegten Kommandosignalen zugeordnete Freigabeschaltung aufweist, welche nach dem Erkennen einer vorbestimmten ordnungsgemäßen Initialisierungsabfolge der an die Halbleiter-Speichervorrichtung angelegten Kommandosignale ein Freigabesignal liefert, welches die Entriegelung der zum ordnungsgemäßen Betrieb der Halbleiter-Speichervorrichtung vorgesehenen Steuerschaltung bewirkt.

Dem Prinzip der Erfindung folgend wird ein Freigabesignal (CHIPREADY) generiert, welches in Abhängigkeit weiterer interner Signale und der Initialisierungsabfolge aktiv wird und danach vorbestimmte Schaltungen entriegelt. Bis zur Beeendi-

gung der vorgegebenen Initialisierungsabfolge bleiben die vorbestimmten Schaltungen verriegelt. Beispielsweise werden Kommandos decodiert, jedoch nicht ausgeführt, und die Ausgangstreiber hochohmig gehalten.

Nach der bevorzugten Anwendung bei SDRAM-Speichervorrichtungen nach dem JEDEC-Standard ist vorgesehen, dass die von außen an die Halbleiter-Speichervorrichtung angelegten Kommandosignale der von der Freigabeschaltung erkennenden Initialisierungsabfolge das Vorbereitungskommando für die Wortleitungsaktivierung (PRECHARGE), und/oder das Auffrischungskommando (AUTCREFRESH), und/oder das Lade-Konfigurations-Register-Kommando (MODE-REGISTER-SET) aufweist.

Nach einer vorteilhaften konstruktiven Ausgestaltung der erfindungsgemäßen Initialisierungsschaltung ist vorgesehen, dass die Freigabeschaltung wenigstens eine bistabile Kippschaltungsstufe mit einem Setzeingang, an dem ein Kommandosignal (PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET) anliegt, einem Rücksetzeingang, an dem das Versorgungsspannungsstabilsignal (POWERON) oder ein davon abgeleitetes bzw. verknüpftes Signal anliegt, und mit einem Ausgang, an dem das Freigabesignal (CHIPREADY) abgeleitet ist, aufweist.

Insbesondere besitzt die Freigabeschaltung mehrere, jeweils einem Kommandosignal zugeordnete bistabile Kippschaltungsstufen.

In zweckmäßiger Ausgestaltung der Erfindung ist vorgesehen, dass der Ausgang wenigstens einer der bistabilen Kippschaltungsstufen an einen Rücksetzeingang einer weiteren Kippschaltungsstufe geführt ist. Hierbei kann des Weiteren vorgesehen sein, dass bei einer der bistabilen Kippschaltungsstufe das Versorgungsspannungsstabilsignal (POWERON) und das von dem Ausgang einer weiteren Kippschaltungsstufe ausgegebene

Signal über ein Gatter logisch verknüpft an den Rücksetzeingang der Kippschaltungsstufe geführt sind.

Weitere vorteilhafte Ausgestaltungen der Erfindung ergeben sich aus den Unteransprüchen.

Nachfolgend wird die Erfindung anhand mehrerer in der Zeichnung dargestellter Ausführungsbeispiele weiter erläutert. Es zeigt:

Figur 1 eine schematische Blockdarstellung einer den Einschaltvorgang des Halbleiterspeichers und ihrer Schaltungsbestandteile steuernden Initialisierungsschaltung;

Figur 2 ein schematisches Schaltbild einer das Freigabesignal (CHIPREADY) liefernden Freigabeschaltung;

Figur 3 ein Zeitablaufdiagramm zur Erläuterung der Funktionsweise der Schaltung nach Figur 2;

Figur 4 ein Schaltbild einer Freigabeschaltung nach einem Ausführungsbeispiel der Erfindung.

Figur 1 zeigt die für das Verständnis der Erfindung wichtigen Schaltungsbestandteile einer nach dem JEDEC-Standard arbeitenden SDRAM-Speichervorrichtung mit einer den Einschaltvorgang der Halbleiterspeichervorrichtung und ihrer Schaltungsbestandteile steuernden Initialisierungsschaltung mit einer Eingangsschaltung 1, an deren Eingang 2 die von außen an den Halbleiterspeicher einzugebenden Kommando- und Taktsignale anliegen, verstärkt und aufbereitet werden, einem der Eingangsschaltung 1 nachgeschalteten Kommandodecoder 3, an dessen Ausgang 4 unter anderem die Kommandosignale PRE bzw. PRECHARGE (Vorbereitungskommando für die Wortleitungsaktivie-

rung), ARF bzw. AUTOREFRESH (Auffrischungskommando) und MRS bzw. MODE-REGISTER-SET (Lade-Konfiguration-Register-Kommando) ausgegeben werden, sowie einer Schaltung 5 für die interne Spannungsregulierung bzw. -detektierung, an deren Eingang 6 die von außen an den Halbleiter-Speicher anliegenden externen Versorgungsspannungen zugeführt sind, und an deren Ausgang 7 das POWERON-Signal und an deren Ausgang 8 die stabilisierten internen Versorgungsspannungen geliefert werden. Die Funktionsweise und der Aufbau der Schaltungen 1, 3 und 5 ist dem Fachmann hinreichend bekannt und braucht daher nicht näher erläutert werden. Wichtig für das Verständnis der Erfindung ist, dass die Schaltung 5 ein aktives POWERON-Signal liefert, wenn nach der POWERUP-Phase des SDRAM-Speichers die am Ausgang 8 anliegenden internen Versorgungsspannungen die für den ordnungsgemäßen Betrieb des Bauelementes erforderlichen Werte erreicht haben.

Nach der Erfindung besitzt die Initialisierungsschaltung darüber hinaus eine den Schaltungen 3 und 5 nachgeschaltete Freigabeschaltung 9, an deren Eingang 10 unter anderem die Kommandosignale PRE, ARF und MRS, an deren Eingang 11 das POWERON-Signal anliegt, und an deren Ausgang 12 das nach dem Erkennen einer vorbestimmten ordnungsgemäßen Initialisierungsabfolge der an die Halbleiter-Speichervorrichtung angelegten Kommandosignale ein Freigabesignal CHIPREADY geliefert wird, welches die Entriegelung der zum ordnungsgemäßen Betrieb der Halbleiter-Speichervorrichtung vorgesehenen Steuerschaltungen 13 bewirkt. Diese internen Steuerschaltungen 13 dienen unter anderem der Ablaufsteuerung für einen oder mehrere der (nicht näher dargestellten) Speicherblöcke des SDRAM-Speichers und sind als solche bekannt.

Figur 2 zeigt ein bevorzugtes Ausführungsbeispiel der Freigabeschaltung 9 nach der Erfindung. Diese umfasst drei bistabile Kippschaltungsstufen 14, 15 und 16 mit jeweils einem Setz-

eingang S, einem Rücksetzeingang R, sowie einem Ausgang Q, ein dem Rücksetzeingang R der Kippschaltungsstufe 15 vorgeschaltetes UND-Gatter 17, ein sämtlichen Ausgängen Q der Kippschaltungsstufen 14, 15, 16 nachgeschaltetes UND-Gatter 18, sowie einem dem UND-Gatter 18 nachgeschalteten Inverter 19, an dessen Ausgang 12 das Freigabesignal CHIPREADY ausgegeben wird, wobei das Freigabesignal HIGH-aktiv ist, d.h. aktiviert ist, wenn sein Spannungspegel auf logisch HIGH ist. Die an den jeweiligen Setzeingängen S der bistabilen Kippschaltungsstufen 14, 15, 16 anliegenden Kommandosignale PRE, ARF, MRS sind jeweils LOW-aktiv, d.h. diese Signale sind aktiv, wenn ihr Spannungspegel auf logisch LOW liegt, während das POWERON-Signal wiederum HIHG-aktiv ist. Das POWERON-Signal liegt bei den Kippschaltungsstufen 14 und 16 unmittelbar an den Rücksetzeingängen R an und liegt bei der Kippschaltungsstufe 15 zunächst an dem einen Eingang des UND-Gatters 17 an, an dessen anderem Eingang das von dem Ausgang Q der Kippschaltungsstufe 14 ausgegebenen Signal anliegt, wobei der Ausgang des UND-Gatters 17 mit dem Rücksetzeingang der Kippschaltungsstufe 15 verbunden ist.

Die Funktionsweise der in Figur 2 dargestellten Freigabeschaltung 9 ist dergestalt, dass eine Aktivierung des Freigabesignales CHIPREADY am Ausgang 12 auf logisch HIGH erst dann generiert wird, wenn eine vorbestimmte zeitliche Initialisierungsabfolge der Kommandosignale PRE, ARF und MRS und eine Aktivierung des POWERON-Signales auf den logischen Pegel HIGH detektiert wird. Erst danach werden aufgrund der Aktivierung des Freigabesignales CHIPREADY die Steuerschaltungen entriegelt; vorher bleiben diese Schaltungen verriegelt.

In dem schematischen Zeitablaufdiagramm nach Figur 3 sind beispielhafte Kommandoabfolgen während des Einschaltvorganges der Halbleiter-Speichervorrichtung zur Erläuterung der Funktionsweise der Freigabeschaltung 9 dargestellt.

Bei der Fallkonstellation A erfolgt eine gegenüber der Aktivierung des POWERON-Signales zu frühe Aktivierung des Signales PRECHARGE auf LOW-aktiv, so dass konsequenterweise noch keine Aktivierung des Freigabesignales CHIPREADY auf logisch LOW erfolgt, da die ordnungsgemäße Initialisierungsabfolge eine Wartezeit vor dem ersten Kommando erfordert. Richtigerweise wird damit der Signalhub des Kommandos PRECHARGE nach der Fallkonstellation A ignoriert. Bei der Fallkonstellation B ist die zeitliche Reihenfolge der Aktivierung des Signales AUTOFRESH auf logisch LOW falsch, da die ordnungsgemäße Initialisierungsabfolge einen vorherigen PRECHARGE-Befehl vor dem AUTOREFRESH-Befehl vorschreibt. Der Signalhub des AUTOREFRESH-Signales auf logisch LOW nach der Fallkonstellation B wird daher ebenfalls ignoriert, das Freigabesignal geht nicht auf logisch HIGH. Bei der Fallkonstellation C liegt - konform mit dem JEDEC-Standard - eine richtige zeitliche Reihenfolge der Befehle PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET vor; folgerichtig wird nun, nachdem auch das POWERON-Signal auf logisch HIGH ist, ein Freigabesignal CHIPREADY auf logisch HIGH geliefert. Mit dem Symbol D ist strichliert dargestellt noch eine weitere denkbare, erlaubte und daher ein Freigabesignal auslösende Initialisierungsabfolge dargestellt: Eine Aktivierung des Kommandos MODE-REGISTER-SET auf logisch LOW ist nach der Aktivierung des POWERON-Signales jederzeit erlaubt.

Figur 4 zeigt in näheren Einzelheiten ein bevorzugtes Ausführungsbeispiel einer erfindungsgemäßen Freigabeschaltung 9. Bei diesem Ausführungsbeispiel ist jede bistabile Kippstufe 14, 15, 16 aus jeweils zwei NAND-Gattern 14A, 14B, 15A, 17, 16A, 16B, sowie einem Inverter 14C, 15C und 16C aufgebaut, die in der dargestellten Art und Weise miteinander verbunden sind. Bei der bistabilen Kippstufe 15 ist das NAND-Gatter 17 mit drei Eingängen versehen.

Patentansprüche

1. Dynamische Halbleiter-Speichervorrichtung vom wahlweisen Zugriffstyp (DRAM/SDRAM) mit einer den Einschaltvorgang der Halbleiter-Speichervorrichtung und ihrer Schaltungsbestandteile steuernden Initialisierungsschaltung, welche nach einer nach dem Einschalten der Halbleiter-Speichervorrichtung erfolgten Stabilisierung der Versorgungsspannung ein Versorgungsspannungsstabilsignal (POWERON) liefert,
dadurch g e k e n n z e i c h n e t,
dass die Initialisierungsschaltung eine dem Versorgungsspannungsstabilsignal (POWERON) und weiteren, von außen an die Halbleiter-Speichervorrichtung angelegten Kommandosignalen (PRE, ARF, MRS) zugeordnete Freigabeschaltung (9) aufweist, welche nach dem Erkennen einer vorbestimmten ordnungsgemäßen Initialisierungsabfolge der an die Halbleiter-Speichervorrichtung angelegten Kommandosignale Kommandosignalen (PRE, ARF, MRS) ein Freigabesignal (CHIPREADY) liefert, welches die Entriegelung der zum ordnungsgemäßen Betrieb der Halbleiter-Speichervorrichtung vorgesehenen Steuerschaltung (13) bewirkt.

2. Halbleiter-Speichervorrichtung nach Anspruch 1,
dadurch g e k e n n z e i c h n e t,
dass die von außen an die Halbleiter-Speichervorrichtung angelegten Kommandosignale (PRE, ARF, MRS) der von der Freigabeschaltung (9) erkennenden Initialisierungsabfolge das Vorbereitungskommando für die Wortleitungsaktivierung (PRECHARGE), und/oder das Auffrischungskommando (AUTOREFRESH), und/oder das Lade-Konfigurations-Register-Kommando (MODE-REGISTER-SET) aufweist.

3. Halbleiter-Speichervorrichtung nach Anspruch 1 oder 2, dadurch g e k e n n z e i c h n e t, dass die Freigabeschaltung (9) wenigstens eine bistabile Kippschaltungsstufe (14, 15, 16) mit einem Setzeingang (S), an dem ein Kommandosignal (PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET) anliegt, einem Rücksetzeingang (R), an dem das Versorgungsspannungsstabilsignal (POWERON) oder ein davon abgeleitetes bzw. verknüpftes Signal anliegt, und mit einem Ausgang (Q), an dem das Freigabesignal (CHIPREADY) (9) abgeleitet ist, aufweist.

4. Halbleiter-Speichervorrichtung nach Anspruch 3, dadurch g e k e n n z e i c h n e t, dass die Freigabeschaltung (9) mehrere, jeweils einem Kommandosignal (PRE, ARF, MRS) zugeordnete bistabile Kippschaltungsstufen (14, 15, 16) aufweist.

5. Halbleiter-Speichervorrichtung nach Anspruch 3 oder 4, dadurch g e k e n n z e i c h n e t, dass der Ausgang (Q) wenigstens einer der bistabilen Kippschaltungsstufen (14) an einen Rücksetzeingang einer weiteren Kippschaltungsstufe (15) geführt ist.

6. Halbleiter-Speichervorrichtung nach einem der Ansprüche 3 bis 5, dadurch g e k e n n z e i c h n e t, dass bei einer der bistabilen Kippschaltungsstufe (15) das Versorgungsspannungsstabilsignal (POWERON) und das von dem Ausgang (Q) einer weiteren Kippschaltungsstufe (14) ausgegebene Signal über ein Gatter (17) logisch verknüpft an den Rücksetzeingang (R) der Kippschaltungsstufe (15) geführt sind.

7. Halbleiter-Speichervorrichtung nach einem der Ansprüche 3 bis 6,
dadurch g e k e n n z e i c h n e t,
dass die bistabile Kippschaltungsstufe (14, 15, 16) jeweils durch ein aus wenigstens zwei NOR- oder NAND-Gattern (14A, 14B, 15A, 17, 16A, 16B) aufgebautes RS-Flip-Flop ausgebildet ist.

8. Halbleiter-Speichervorrichtung nach einem der Ansprüche 2 bis 7,
dadurch g e k e n n z e i c h n e t,
dass die von der Freigabeschaltung (9) als ordnungsgemäße Initialisierungsabfolge erkannte und das Freigabesignal (CHIPREADY) auslösende Initialisierungsabfolge eine mit dem JEDEC-Standard konforme Kommandofolge darstellt.

9. Halbleiter-Speichervorrichtung nach einem der Ansprüche 1 bis 8,
dadurch g e k e n n z e i c h n e t,
dass die Ausgangstreiber der Halbleiter-Speichervorrichtung beim Einschaltvorgang bis zur Ausgabe des von der Freigabeschaltung (9) gelieferten Freigabesignals (CHIPREADY) verriegelt bleiben.

10. Halbleiter-Speichervorrichtung nach einem der Ansprüche 1 bis 9,
dadurch g e k e n n z e i c h n e t,
dass eine ordnungsgemäße Initialisierungsabfolge, welche die Auslösung eines Freigabesignals (CHIPREADY) bewirkt, folgende zeitlich aufeinanderfolgende Kommandosequenzen umfasst:
a) erstens PRE, zweitens ARF, drittens MRS, oder
b) erstens PRE, zweitens MRS, drittens ARF, oder
c) erstens MRS, zweitens PRE, oder drittens ARF,
wobei die Abkürzungen folgende Kommandos bezeichnen:
PRE = Vorbereitungskommando für die Wortleitungsaktivierung

(PRECHARGE),
ARF = Auffrischungskommando (AUTOREFRESH), und
MRS = Lade-Konfigurations-Register-Kommando (MODE-REGISTER-SET).

11. Verfahren zur Initialisierung einer dynamischen Halbleiter-Speichervorrichtung vom wahlweisen Zugriffstyp (DRAM/SDRAM) vermittels einer den Einschaltvorgang der Halbleiter-Speichervorrichtung und ihrer Schaltungsbestandteile steuernden Initialisierungsschaltung, welche nach einer nach dem Einschalten der Halbleiter-Speichervorrichtung erfolgten Stabilisierung der Versorgungsspannung ein Versorgungsspannungsstabilsignal (POWERON) liefert,
dadurch g e k e n n z e i c h n e t,
dass die Initialisierungsschaltung vermittels einer dem Versorgungsspannungsstabilsignal (POWERON) und weiteren, von außen an die Halbleiter-Speichervorrichtung angelegten Kommandosignalen (PRE, ARF, MRS) zugeordneten Freigabeschaltung (9) nach dem Erkennen einer vorbestimmten ordnungsgemäßen Initialisierungsabfolge der an die Halbleiter-Speichervor-richtung angelegten Kommandosignale ein Freigabesignal (CHIP-READY) liefert, welches die Entriegelung der zum ordnungsgemäßen Betrieb der Halbleiter-Speichervorrichtung vorgesehenen Steuerschaltung (13) bewirkt.

12. Verfahren nach Anspruch 11,
dadurch g e k e n n z e i c h n e t,
dass die von außen an die Halbleiter-Speichervorrichtung angelegten Kommandosignale (PRE, ARF, MRS) der von der Freigabeschaltung (9) erkennenden Initialisierungsabfolge das Vorbereitungskommando für die Wortleitungsaktivierung (PRECHARGE), und/oder das Auffrischungskommando (AUTOREFRESH), und/oder das Lade-Konfigurations-Register-Kommando (MODE-REGISTER-SET) aufweist.

13. Verfahren nach Anspruch 11 oder 12,
dadurch g e k e n n z e i c h n e t,
dass die Ausgangstreiber der Halbleiter-Speichervorrichtung beim Einschaltvorgang bis zur Ausgabe des von der Freigabeschaltung (9) gelieferten Freigabesignals (CHIPREADY) verriegelt bleiben.

14. Verwendung einer ein Freigabesignal (CHIPREADY) liefernden Freigabeschaltung (9) zur Steuerung des Einschaltvorganges einer dynamischen Halbleiter-Speichervorrichtung vom wahlweisen Zugrifftyp (DRAM/SDRAM) nach einem der Ansprüche 1 bis 10.

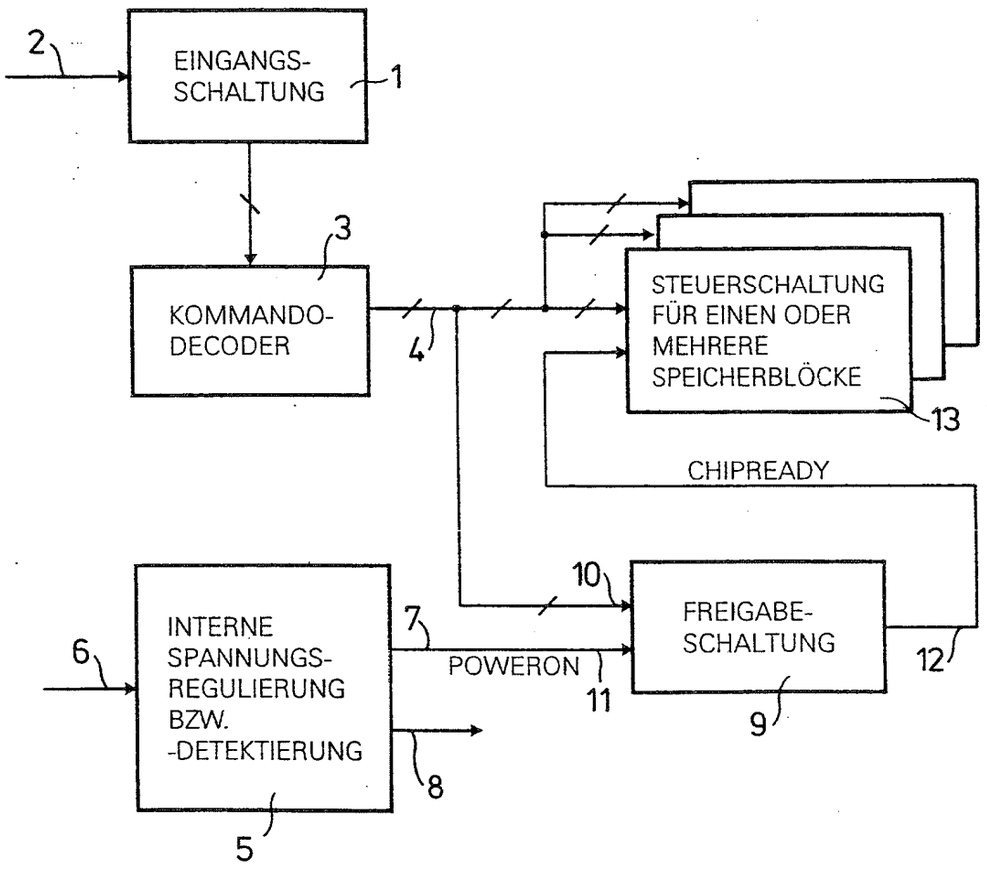
Zusammenfassung

Bezeichnung der Erfindung: Dynamische Halbleiterspeichervorrichtung und Verfahren zur Initialisierung einer dynamischen Halbleiterspeichervorrichtung

Die Erfindung betrifft eine dynamische Halbleiter-Speichervorrichtung vom wahlweisen Zugriffstyp (DRAM/SDRAM) mit einer den Einschaltvorgang der Halbleiter-Speichervorrichtung und ihrer Schaltungsbestandteile steuernden Initialisierungsschaltung, welche nach einer nach dem Einschalten der Halbleiter-Speichervorrichtung erfolgten Stabilisierung der Versorgungsspannung ein Versorgungsspannungsstabilsignal (POWERON) liefert. Die Initialisierungsschaltung weist eine dem Versorgungsspannungsstabilsignal (POWERON) und weiteren, von außen an die Halbleiter-Speichervorrichtung angelegten Kommandosignalen zugeordnete Freigabeschaltung (9) auf, welche nach dem Erkennen einer vorbestimmten ordnungsgemäßen Initialisierungsabfolge der an die Halbleiter-Speichervorrichtung angelegten Kommandosignale ein Freigabesignal (CHIP-READY) liefert, welches die Entriegelung der zum ordnungsgemäßen Betrieb der Halbleiter-Speichervorrichtung vorgesehenen Steuerschaltung (13) bewirkt.

(Figur 1)

Fig 1


2
EINGANGS-
SCHALTUNG
1
3
KOMMANDO-
DECODER
4
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FÜR EINEN ODER
MEHRERE
SPEICHERBLÖCKE
13
CHIPREADY
10
FREIGABE-
SCHALTUNG
12
9
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POWERON
11
6
INTERNE
SPANNUNGS-
REGULIERUNG
BZW.
-DETEKTIERUNG
8
5

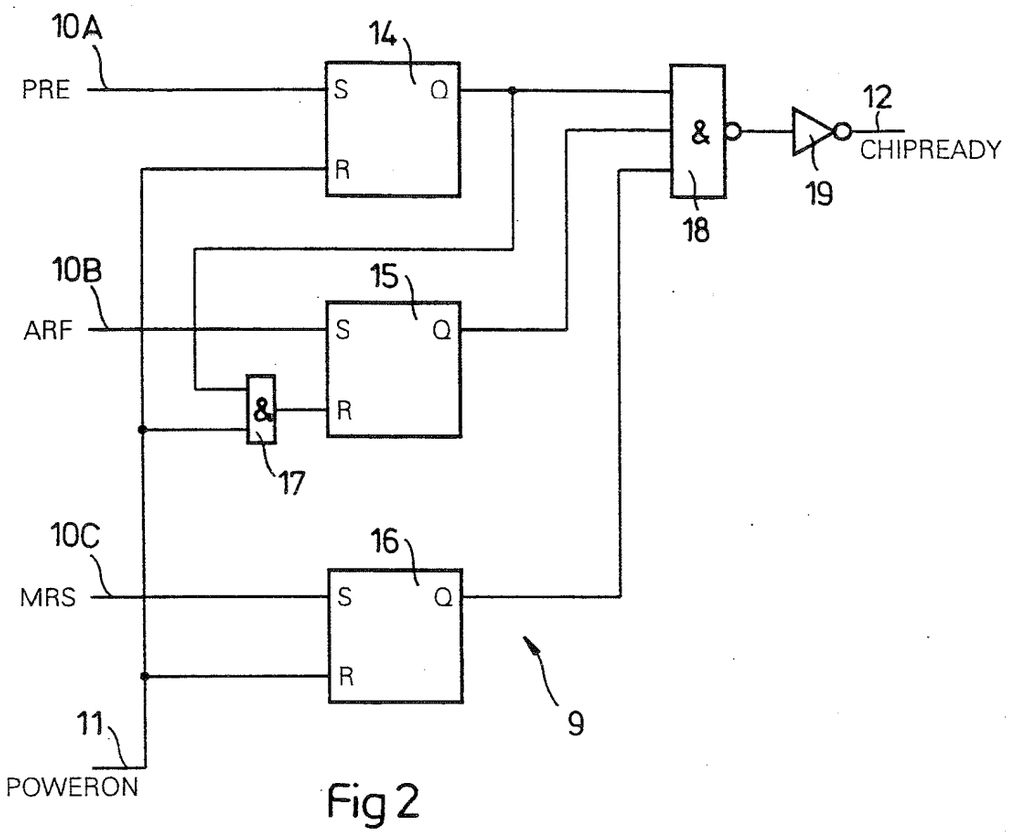

10A
PRE
14
S
Q
R
&
12
CHIPREADY
19
18
10B
ARF
15
S
Q
R
&
17
10C
MRS
16
S
Q
R
9
11
POWERON

Fig 2

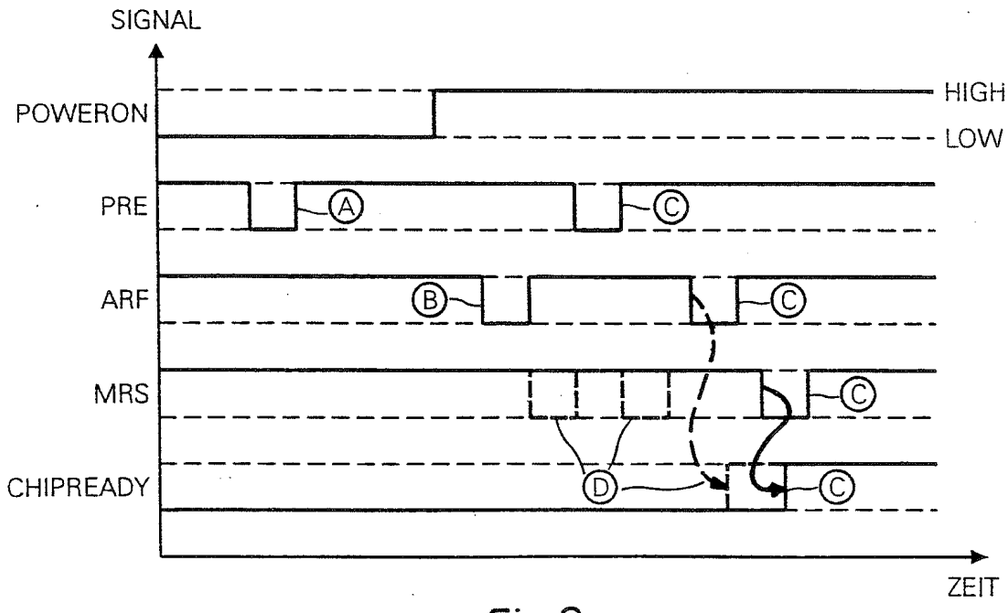
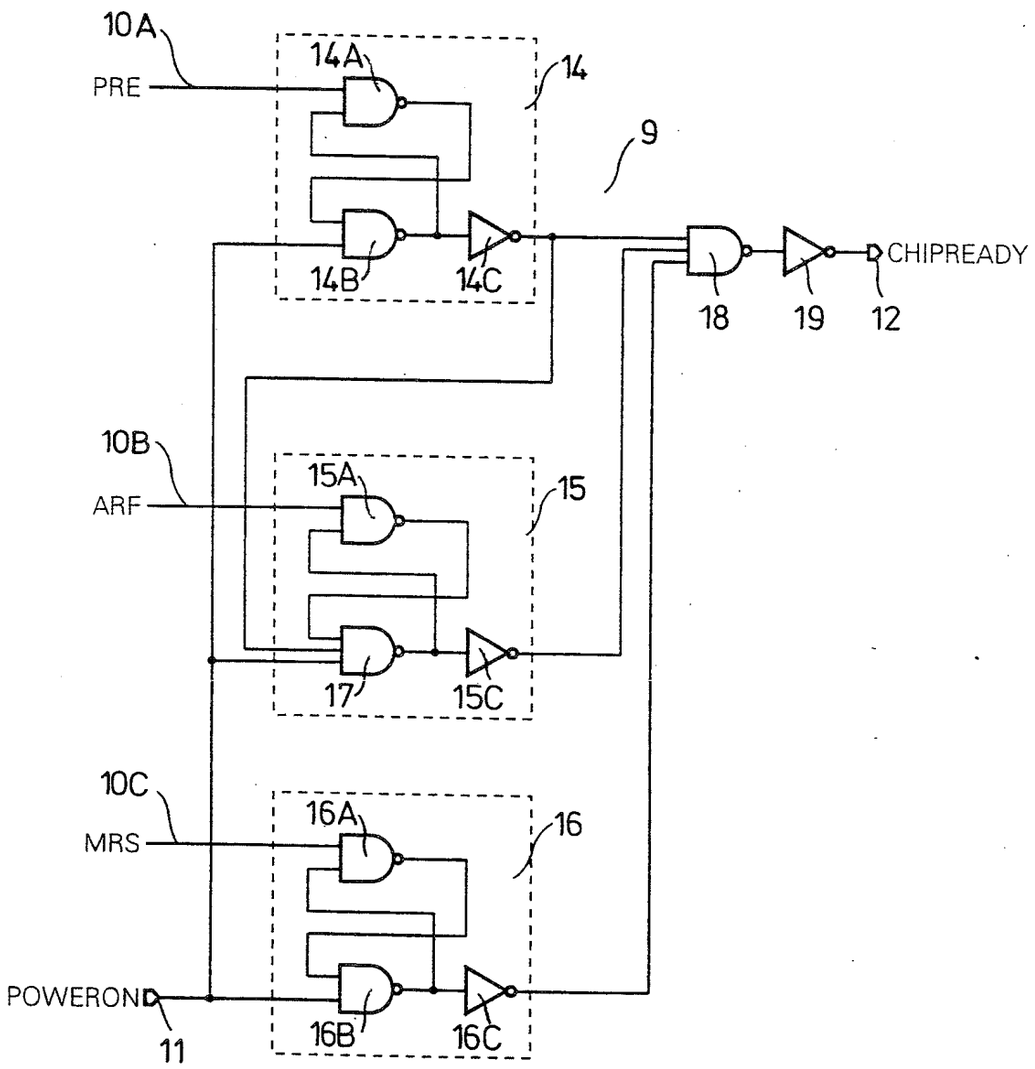

SIGNAL
POWERON
HIGH
LOW
PRE
A
C
ARF
B
C
MRS
C
CHIPREADY
D
C
ZEIT

Fig 3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PRE
14A
14
9
14B
14C
18
19
CHIPREADY
12
10B
ARF
15A
15
17
15C
10C
MRS
16A
16
POWERON
11
16B
16C

Fig 4

Docket # CR98P1989

Applic. # 09/343,431

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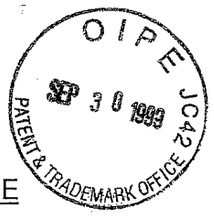
#6



Docket No.: GR 98 P 1989

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Gunnar Krause
Appl. No.	:	09/343,431
Filed	:	June 30, 1999
Title	:	Dynamic Semiconductor Memory Device And Method For Initializing A Dynamic Semiconductor Memory Device
Art Unit	:	2818

ASSOCIATE POWER OF ATTORNEY

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

S i r :

Please recognize GREGORY L. MAYBACK (Reg. No. 40,719) as my associate in the matter in the above-identified application, with full powers. Please continue addressing all communications to the following address:

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Respectfully submitted,

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GAU 2818

Docket No.: GR 98 P 1989

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Applicant	:	Gunnar Krause
Application No.	:	09/343,431
Filed	:	June 30, 1999
Title	:	Dynamic Semiconductor Memory Device And Method For Initializing A Dynamic Semiconductor Memory Device
Art Unit	:	2818

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

European Patent Application EP 0 797 207 A2 (Shinozaki et al.), dated September 24, 1997;

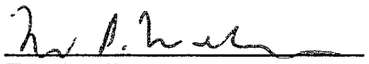
Japanese Patent Application No. 9-106668, dated April 22, 1997.

In accordance with 37 C.F.R. 1.97(e) the undersigned herewith states that each item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications,

patents and or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,



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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
(37 CFR 1.98(b)

Attorney Docket No.:	Serial No.
GR 98 P 1989	09/343,431

Applicant: Gunnar Krause

Filing Date	Group Art Unit
June 30, 1999	2818

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
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	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
VL	J	0 797 207 A2	09/24/97	Europe	—	—	X	
VL	K	9-106668	4/22/97	Japan	—	—		X
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

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EXAMINER	DATE CONSIDERED
Vu Le	7/11/00

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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

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(12) EUROPEAN PATENT APPLICATION

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(51) Int. Cl.[6]: **G11C 7/00**

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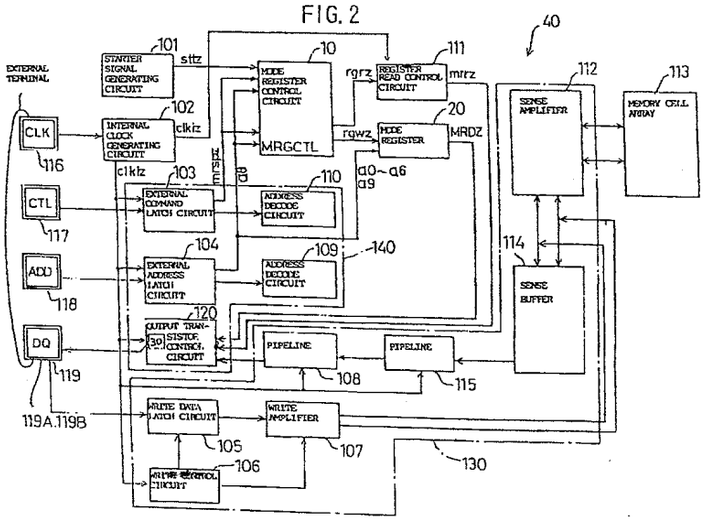
(54) Mode register control circuit and semiconductor device having the same

(57) A mode register control circuit (10) for a semiconductor device (40) includes a first control unit (202) for preventing the content of a mode register (20) from being read, using an initializing signal for instructing latching circuits (103, 104) to be initialized, the initialization being done in a transient occurring after the semiconductor device (40) is turned on; a second control unit (104) for instructing the mode register (20) to execute a mode register read command even if a mode register set command has not been executed, on the condition that an external command other than the mode register read command is detected when the semiconductor device (40) is turned on; or a third control unit (206) for instructing the mode register (20) to execute the mode register read command on the condition that the mode register set command is executed after the semiconductor device (40) is turned on.

FIG. 2



EP 0 797 207 A2

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2.14.14/3.4

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Description

BACKGROUND OF THE INVENTION

1. Field of the invention

The present invention relates to mode register control circuit for controlling a semiconductor memory, and more particularly to a mode register control circuit for controlling a synchronous dynamic RAM (SDRAM), a type of high-band dynamic RAM (high-band DRAM) capable of achieving a data transfer speed of, for example, 100 Mbyte/sec.

2. Description of the related art

Fig. 1A is a circuit diagram showing a conventional mode register control circuit 9 and a mode register 2 controlled by the mode register control circuit 9.

A conventional mode register control circuit 9 may be built into an integrated SDRAM chip capable of high-speed outputting of data in response to an externally supplied high-speed clock.

The mode register control circuit 9 (indicated as MRGCTL in Fig. 1A) is provided in an SDRAM 1 so as to control operation of reading from the mode register 2 within the SDRAM 1, in synchronism with an external command (mrspz) and external address data (a0 - a6, a8 and a9) fed via a terminal of the SDRAM 1.

The mode register 2 latches an operating mode of the SDRAM 1 in response to a mode register set command and a mode register read command, which are external commands.

The mode register read command causes an operating mode of the SDRAM 1 chip to be output via an output terminal DQ provided on the SDRAM 1 chip.

More specifically, the mode register read command causes a mode selection signal (indicated as MRDZ in Fig. 1A) to be output via an output transistor 3 (indicated as outTr in Fig. 1A) connected to the output terminal DQ.

A description will now be given, with reference to Fig. 1A, of an operation effected by external commands in the mode register control circuit 9.

The mode register control circuit 9 is constructed to be capable of executing the mode register read command whether the mode register control circuit 9 is in an idle state or an active state. Since a normal reading operation is conducted after the chip becomes active, data is not output in an idle state.

The mode register set command initiates an operating mode which controls the SDRAM 1 to be set to a desired operating mode by setting a CAS latency (CL) operating mode, a burst length (BL) operating mode and a burst type in the mode register 2.

Setting of an operating mode (an operating mode initiated by the mode register set command, or an operating mode initiated by the mode register set command) in the mode register control signal 9 is effected by raising an operating mode signal (more specifically, CL1 - CL3 signals) selected when the mode register set command is executed. More specifically, as shown in Fig. 1A, address data a0 - a6, a8 and a9 input to the mode register 2 via an address input terminal ADD on the chip and specifying mode addresses are used to set the operating mode signal.

In the conventional mode register control circuit 9 as shown in Fig. 1A, the output transistor 3 (indicated as outTr in Fig. 1A) of the SDRAM 1 may be put in a low-impedance state when the mode register read command is input to the SDRAM 1 when the SDRAM 1 is turned on, or when it is determined that the mode register read command is latched in internal latching means in the SDRAM 1 (more specifically, an external command latching part or an external address latching part). The low-impedance state presents problems described later.

In the conventional control circuit, the mode register read command allows data to be output when the SDRAM 1 is idle. Hence, if it is determined that the data is output via the output terminal DQ according to the mode register read command, mode data inside the mode register can be read from the output transistor of the SDRAM 1.

A description will now be given, with reference to Fig. 1B, of how the mode register set command and the mode register read command are executed in the mode register control circuit 9.

As shown in the timing chart of Fig. 1B, predetermined data (a0 - a6, a8 and a9 shown in (b-2) of Fig. 1B) for selecting between the mode register set command and the mode register read command is input to the mode register 2 in synchronism with an internal clock of the SDRAM 1. The internal clock is a signal indicated as clkiz in (b-1) of Fig. 1B externally supplied via an external clock terminal CLK and an internal clock generating unit. A difference between the data setting for the mode register set command and that for the mode register read command is found only in a mode setting signal, that is, an a08 pin signal a8 supplied via the address input terminal ADD on the chip as address data specifying the mode address. When the a8 signal is L, the mode register set command is specified; when H, the mode register read command is specified.

Subsequently, the mode register control circuit 9 generates a register read signal (rgrz) (see (b-4) of Fig. 1B) which is a composite signal composed of the mode setting signal a8 and a mrspz signal (see (b-3) of Fig. 1B) which is generated in the external command latching part in the SDRAM 1 when the mode register set command or the mode register read command is latched, in synchronism with the external clock signal clkiz.

Subsequently, the mode register control circuit 9 generates a driving signal mrrz (see (b-5) of Fig. 1B) which is the register read signal latched. The driving signal mrrz is latched until the next external clock clkiz is generated. In response to the driving signal mrrz, the

mode selection signal MRDZ stored in the mode register 2 is output (see (b-6) of Fig. 1B).

However, in the conventional mode register control circuit 9, if it is determined that data is output, when the SDRAM 1 is turned on, via the external output terminal DQ of the SDRAM 1 according to the mode register read command, or if it is determined that data is output in an idle state before the SDRAM 1 is turned on via the external output terminal DQ of the SDRAM 1 according to the mode register read command, the mode data inside the mode register is read from the output transistor of the SDRAM 1, causing the output transistor of the SDRAM 1 to be put in a low-impedance state. Therefore, the conventional mode register control circuit has a problem in that an abnormal current may flow when the SDRAM 1 is turned on or in an idle state occurring after the SDRAM 1 is turned on.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide a mode register control and a semiconductor integrated circuit having the same, in which the aforementioned problems are eliminated.

Another and more specific object of the present invention is to provide a mode register control circuit capable of preventing an abnormal current from flowing in the SDRAM when the SDRAM is turned on or in an idle state occurring after the SDRAM is turned on, by providing a control unit in the SDRAM (more specifically, in the mode register control circuit MRGCTL) for preventing the output transistor of the SDRAM from being in a low-impedance state even if it is determined that data is output, when the SDRAM is turned on, via an external output terminal of an SDRAM according to the mode register read command, or if it is determined that data is output in an idle state before the SDRAM is turned on via the external output terminal DQ of the SDRAM according to the mode register read command.

In order to achieve the aforementioned objects, the present invention provides a mode register control circuit provided in a semiconductor device and controlling operation of reading from a mode register of the semiconductor device in synchronism with an external command signal and an external clock signal,

the mode register control circuit comprising a first control unit which uses internal means to disable, when the semiconductor device is turned on, execution a mode register read command, an external command, for specifying reading from the mode register so as to prevent reading from the mode register.

The first control unit may use internal means to disable, when the semiconductor device is turned on, execution of the mode register read command, using an initializing signal for specifying initialization of a latch part for latching an external command and/or an external address externally fed to the semiconductor device, the initialization being done during a transient state occurring after the semiconductor device is turned on.

By providing the first control unit, an abnormal current is prevented from flowing in an output transistor of the semiconductor device by preventing the mode register read command from being executed when the semiconductor device is turned on.

The aforementioned objects can also be achieved by a mode register control circuit provided in a semiconductor device and controlling operation of reading from a mode register of the semiconductor device in synchronism with an external command signal and an external clock signal, the mode register control circuit comprising a second control unit which instructs, upon determining that an external command detected when the semiconductor device is turned on is other than a mode register read command, an external command, specifying reading from the mode register, the mode register to execute the mode register read command even if a mode register set command, an external command, has not been executed after a power supply voltage becomes stable.

By providing the second control unit, the mode register read command is enabled on the condition that the mode register read command is executed after the semiconductor device is turned on, so that an abnormal current is prevented from flowing in the output transistor of the semiconductor device. In an idle state occurring after the semiconductor device is turned on, an abnormal current is prevented from flowing in the output transistor of the semiconductor device.

The aforementioned objects can also be achieved by a mode register control circuit provided in a semiconductor device and controlling operation of reading from a mode register of the semiconductor device in synchronism with an external command signal and an external clock signal, the mode register control circuit comprising a third control unit which instructs, upon detecting that a mode register set command, an external command, has been executed after the semiconductor is turned on, the mode register to execute a mode register read command, an external command, for specifying reading from the mode register.

By providing the second control unit, the mode register read command is enabled on the condition that the mode register set command is executed after the semiconductor device is turned on, so that an abnormal current is prevented from flowing in the output transistor of the semiconductor device. In an idle state occurring after the semiconductor device is turned on, an abnormal current is prevented from flowing in the output transistor of the semiconductor device.

The mode register control circuit may include the second control unit which instructs, upon determining that an external command detected when the semiconductor device is turned on is other than a mode register read command, an external command, specifying reading from the mode register, the mode register to execute the mode register read command even if a mode register set command, an external command, has not been executed after a power supply voltage becomes stable; and the third control unit which instructs, upon detecting

that the mode register set command has been executed after the semiconductor is turned on, the mode register to execute the mode register read command.

The mode register control circuit may include the second control unit which instructs, upon determining that an external command detected when the semiconductor device is turned on is other than the mode register read command, the mode register to execute the mode register read command even if the mode register set command has not been executed after a power supply voltage becomes stable; and the third control unit which instructs, upon detecting that a mode register set command, an external command, has been executed after the semiconductor is turned on, the mode register to execute a mode register read command, an external command, for specifying reading from the mode register.

By providing the second control unit and the third control unit, an abnormal current is prevented from flowing in the output transistor of the semiconductor device, by disabling execution of the mode register read command when the semiconductor device is turned on. In the idle state occurring after the semiconductor device is turned on, an abnormal current is prevented from flowing in the output transistor of the semiconductor device, by ensuring that execution of the mode register read command is enabled on the condition that the mode register set command is executed.

The aforementioned objects of the present invention can also be achieved by a semiconductor device comprising:

a starter signal generating circuit for generating an initializing signal for initializing a latching circuit when the semiconductor device is turned on;
an internal clock generating unit for generating an internal clock signal in correspondence with an external clock signal;
a memory cell array;
a read/write circuit for reading data from and writing data to the memory cell array;
an input/output circuit for inputting and outputting data addresses and commands;
a mode register for latching an operation mode of the input/output circuit;
a mode register control circuit according to the present invention.

By providing the mode register control circuit of the present invention, an abnormal current is prevented from flowing in the output transistor of the semiconductor device, by disabling execution of the mode register read command when the semiconductor device is turned on. In the idle state occurring after the semiconductor device is turned on, an abnormal current is prevented from flowing in the output transistor of the semiconductor device, by ensuring that execution of the mode register read command is enabled on the condition that the mode register read command is executed.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings, in which:

Fig. 1A is a circuit diagram showing a conventional mode register circuit and a mode register controlled by the same;
Fig. 1B is a timing chart which explains an operation of the circuit of Fig. 1A;
Fig. 2 is a circuit diagram showing a mode register control circuit of the present invention;
Fig. 3A is a circuit diagram showing a first embodiment of the present invention;
Fig. 3B is a timing chart which explains an operation of the first embodiment;
Fig. 4A is a circuit diagram showing a second embodiment of the present invention; and
Figs. 4B and 4C are timing charts which explain an operation of the second embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A description will now be given, with reference to the associated drawings, of a first and second embodiment of the present invention.

A mode register control circuit 10 according to the first and second embodiments of the present invention controls a semiconductor device 40 (SDRAM) capable of a data transfer speed higher than 100 Mbyte/sec.

A description will be given of a basic construction of an SDRAM 40.

Fig. 2 is a block diagram showing the mode register control circuit 10.

An external clock signal clkiz is a signal input via an external clock terminal (CLK) 116 on the chip. An initializing signal sttz is a signal generated by a starter signal generating unit 101 on the chip so as to instruct latching circuits (specifically, an external command latching circuit 103 and an external address latching circuit 104) in the chip to be initialized when the SDRAM is turned on. A mrspz signal is generated by the external command latching circuit 103 in synchronization with the external clock signal clkiz, when the mode register set command or the mode register read command is fed via a command input terminal (CTL) 117 and latched in the external command latching circuit 103. A mode setting signal a8 is generated by the external address latching circuit 104 in correspondence with address data specifying mode address and input via the address input terminal (ADD) 118 on the chip.

The external clock terminal (CLK) 116, the command input terminal (CTL) 117, the address input terminal (ADD) 118 and an output terminal (DQ) 119 are external terminals provided on the SDRAM 40 chip.

The starter signal generating circuit 101 generates

an initializing signal sttz for instructing latching circuits (more specifically, the external command latching circuit 103 and the external address latching circuit 104) to be initialized.

The internal clock generating circuit 102 generates a clock signal for internal use in accordance with the external clock signal clkiz supplied via the external clock terminal (CLK) 116.

The external address latching circuit 104 latches an external address signal (signal fed to the address input terminal (ADD) 118) in synchronism with the external clock signal clkiz supplied by the internal clock generating circuit 102. The external address signal is embodied by the address data a0 - a6, a9 and the mode setting signal a8. An external address decoding circuit 109 generates a mode type out of the external address signal.

The external command latching circuit 103 latches an external command signal fed via the command input terminal (CTL) 117, that is, the mode register set command or the mode register read command, in synchronism with the external clock signal clkiz supplied from the internal clock generating circuit 102.

An external command decoding circuit 110 generates internal commands such as a mode register set command out of an external command signal.

The mode register control circuit 10 (indicated as MRGCTL in Fig. 2) executes the mode register set command or the mode register read command in accordance with the external address signal (a0 - a6, a9), the mode setting signal (a8) and the mrspz signal. The mode register control circuit 10 generates a register set signal rgwz for instructing a mode register 20 to be set and also generates the register read signal rgrz for controlling the reading from the mode register.

A register read control circuit 111 generates, in accordance with a register read signal rgrz, a driving signal mrrz for instructing the output transistor control circuit 120 to drive an output transistor (outTr) 30.

The mode register 20 generates the mode selection signal (MRDZ) stored in the mode register 20, in accordance with the register read signal rgrz, the external address signal (a0 - a6, a9).

The output transistor control circuit 120 controls the output transistor (outTr) 30 in accordance with the mode selection signal MRDZ.

A memory cell array 113 is constructed such that memory cells each storing data in units of a bit are formed into layers in a predetermined manner. The memory cell array 113 stores write data from a write amplifier circuit 107.

A sense amplifier 112 reads data stored in a memory cell of the memory cell array 113, temporarily stores the same, and transfers the same to a sense buffer 114. The sense amplifier 112 also temporarily stores the write data supplied by the write amplifier circuit 107 and stored in the sense buffer 114.

The sense buffer 114 temporarily stores data read by the sense amplifier 112 or the write data transferred by the write amplifier circuit 107.

A pipeline structure constructed of a pipeline 115 and a pipeline 108 one on top of the other executes a pipeline process for reading data stored in the sense buffer 114 in a parallel manner, in synchronism with an external clock signal clkiz.

A write data latching circuit 105 temporarily stores data input via an external input terminal (DQ) 119B.

The write amplifier circuit 107 writes the buffer latched in the write data latching circuit 105 in the sense buffer 114 in synchronism with the external clock signal clkiz.

A write control circuit 106 controls the latching action of the write data latching circuit 105 and the write operation of the write amplifier circuit 107, in synchronism with the external clock signal clkiz.

A description will now be given of modes of operation of the SDRAM 40.

The SDRAM 40 is capable of outputting data at a data transfer speed of higher than 100 Mbyte/sec, in synchronism with a high-speed clock supplied via the external clock terminal 116. In the SDRAM 40, two operating modes are available: the mode register set mode and the mode register read mode.

The mode register set command initiating the mode register set mode specifies the operating mode in which the SDRAM 40 is used. The mode register set command may set the CAS latency operating mode (CL), the burst length operating mode (BL) or the burst type in the mode register 2 in order to specify a specific operating mode.

Setting of the operating mode is effected by raising the operating mode signal (specifically, CL1 - CL3 signals) selected when the mode register set command is executed. Specifically, as shown in Figs. 3A and 4A, predetermined data a0 - a6 and a9 is input to the mode register 20 so that the operating mode is set. The mode register read command causes an operating mode of the SDRAM 40 chip to be output via a terminal DQ (an output terminal 119A or the output terminal 119B) provided on the SDRAM 40 chip. More specifically, the mode register read mode is such that the mode selection signal (MRDZ shown in Figs. 3A and 4A) is output via the output transistor (outTr) 30 shown in Figs. 3A and 4A and connected to the terminal DQ (the output terminal 119A or the input terminal 119B).

A description will now be given of the SDRAM 40.

When the SDRAM 40 receives the external clock signal clkiz generated by the internal clock generating circuit 102, or a signal supplied via the external clock terminal (CLK) 116 on the chip and the internal clock generating circuit 102, predetermined data (a0 - a6, a8 and a9) for selection between the mode register set command and the mode register read command is input to the mode register 20 in synchronism with the reception. A difference between the data setting for the mode register set command and that for the mode register read command is found only in a mode setting signal, that is, an a08 pin signal a8 supplied via the address

input terminal (ADD) 118 on the chip as address data specifying the mode address. When the a8 signal is L, the mode register set command is specified; when H, the mode register read command is specified.

Subsequently, the mode register control circuit 10 generates a register read signal rgrz which is a composite signal composed of the mode setting signal a8 and a mrspz signal which is generated in the external command latching circuit 103 in the SDRAM 40 when the mode register set command or the mode register read command is latched, in synchronism with the external clock signal clkiz.

Subsequently, the mode register control circuit 10 generates a driving signal mrrz which is the register read signal rgrz latched. The driving signal mrrz is latched until the next external clock clkiz is generated. In response to the driving signal mrrz, the mode selection signal MRDZ stored in the mode register 20 is output via the output transistor (outTr) 30.

A description will now be given of individual embodiments of the present invention.

Fig. 3A is a circuit diagram showing a first embodiment of the present invention; and Fig. 3B is a timing chart which explains an operation according to the first embodiment.

The mode register control circuit (indicated as MRGCTL in Fig. 3A) 10 according to the first embodiment is semiconductor device provided in the SDRAM 40 so as to control operation of reading from the mode register within the SDRAM 40 in synchronism with the external command signal and the external clock signal. The mode register control circuit comprises a first control unit 202.

The first control unit 202 disables, when the SDRAM 40 is turned on, execution of the mode register read command so as to prevent the content of the mode register from being read. When the SDRAM 40 is turned on, the first control unit 202 uses an initialising signal sttz for instructing a transient state which occurs at power-on in the external command latching circuit 103 and the external address latching circuit 104 to be initialized, so that execution of the mode register read command is internally disabled.

A starter signal sttz is used to set logical elements like flip-flop circuits constituting the external command latching circuit 103 and the external address latching circuit 104 at a predetermined potential level (more specifically, at logical H or logical L) so as to put the elements out of an unstable state occurring after the power is on. A prohibiting signal setz generated by the first control unit 202 is set to logical H so as to prevent the mode register read command from being executed at the power-on. That is, no command for reading from the mode register 20 is output. In this way, the mode register read command is prevented by internal means from being executed when the SDRAM 40 is turned on, and the output transistor 30 is prevented from being in a low-impedance state.

The prohibiting signal setz generated by the first control unit 202 is set to logical L when the mode register read command is executed after the SDRAM 40 is turned on, so as to enable reading from the mode register.

More specifically, a signal similar to the register set signal rgwz output to set the mode register is used to reset the flip-flop circuits of the external command latching circuit 103 and the external address latching circuit 104 maintained at the predetermined potential by the starter signal sttz. In this way, the prohibiting signal setz is maintained at logical L.

Thus, the first control unit 202 enables execution of the mode register set command.

A description will now be given, with reference to Fig. 3B, of a specific operation according to the first embodiment.

In phase (1) shown in Fig. 3B, execution of the mode register read command is attempted. However, since the prohibiting signal setz generated by the first control unit 202 is at logical H, the register read signal rgrz generated by the mode register control circuit 10 is at logical L so that the output transistor 30 is maintained at a high-impedance state.

In phase (2) shown in Fig. 3B, the mode setting signal a8 is set to logical L in order for the mode register set command to be executed. Subsequently, the mode register control circuit 10 outputs the register set signal rgwz so as to set the mode register 20. At the same time, the prohibition signal setz generated by the first control unit 202 is latched at logical L so that the driving signal mrrz is generated. Thus, subsequent execution of the mode register read command is enabled.

In phase (3) shown in Fig. 3B, a bus that carries the register read signal rgrz generated by the mode register control circuit 10 is activated since the prohibition signal setz generated by the first control unit 202 is set at logical L as a result of the operation in phase (2). The mode setting signal a8 is set so that the mode register read command is executed. The mrspz signal in synchronism with the internal clock CLK is generated. The register read signal rgrz generated by the mode register control circuit 10 is output. Thus, the mode selection signal MRDZ which carries a content of the mode register 20 is output from the output transistor 30.

In phase (4) shown in Fig. 3B, the output transistor 30 is reset by the internal clock CLK to a high-impedance state so that the whole operation is completed.

As has been described, according to the mode register control circuit 10 provided with the first control unit 202, execution of the mode register read command is prevented when the SDRAM 40 is turned on. In this way, an abnormal current is prevented from flowing in the output transistor 30 of the SDRAM 40.

A description will now be given of the SDRAM 40 according to the first embodiment.

The SDRAM 40 comprises the mode register control circuit 10, the starter signal generating circuit 101 for generating an initializing signal sttz for instructing latching circuits to be initialised at power-on, the internal

clock generating unit 102 for generating an internal clock clkiz in accordance with the external clock, the memory cell array 113, a read/write circuit 130 responsible for reading data from the memory cell 113 and writing data into the same, an input/output circuit 140 responsible for inputting and outputting data addresses and commands, the mode register 20 storing the operating mode of the input/output circuit, and the register read control circuit 111 for controlling reading from the mode register in synchronism with the external clock.

The read/write circuit 130 comprises the write data latching circuit 105, the write control circuit 106, the write amplifier circuit 107, the pipeline 108, the sense amplifier 112, the sense buffer 114, and the pipeline 115 which are described above.

The input/output circuit 140 comprises the external command latching circuit 103, the external address latching circuit 104, the external address decoding circuit 109, the external command decoding circuit 110, and the output transistor control circuit 120.

According to the SDRAM 40 provided with the mode register control circuit 10, it is possible to prevent an abnormal current from flowing in the output transistor (outTr) 30 by prohibiting execution of the mode register read command when the SDRAM 40 is turned on. In the idle state occurring after the SDRAM 40 is turned on, it is ensured that execution of the mode register read command is enabled on the condition that the mode register set command is executed so that an abnormal current is prevented from flowing in the output transistor (outTr) 30.

A description will now be given of a second embodiment.

Fig. 4A is a circuit diagram showing the second embodiment, and Figs. 4B and 4C are timing charts which explain the operation according to the second embodiment.

The mode register control circuit 10 (indicated as MRGCTL in Fig. 4A) according to the second embodiment comprises a second control unit 204 and a third control circuit 106, as shown in Fig. 4A.

Upon detecting that the external command detected when the SDRAM 40 is turned on is other than the mode register read command, the second control unit 204 instructs the mode register to execute the mode register read command even if the mode register set signal has not been executed after the power supply voltage is stabilized.

The third control circuit 106 instructs the mode register to execute the mode register read command when it is determined that the mode register set command is executed after the SDRAM 40 is turned on.

Since the mode register control circuit 10 according to the second embodiment is provided with the second control unit 204 and the third control circuit 206, its added advantage over the mode register control circuit 10 according to the first embodiment is that the operating mode type of the external command, latched in the mode register 20, other than the mode register set command can be read. Even if the mode register set command is not executed, the mode register read command can be executed on the condition that an external command other than the mode register set command is executed after power-on. In this way, a normal internal operation can be effected.

A description will now be given, with reference to Fig. 4B, of a specific operation according to the second embodiment executed when it is determined that the mode register read command is specified, that is, it is determined that a8 = H.

In phase (1) shown in Fig. 4B, the mrspz signal and the mrsqz signal in synchronism with the internal clock CLK, and the mode setting signal a8 are set to logical H, so that the second control unit 204 sets a set signal setR to logical L. The set signal setR set to logical L by the second control unit 204 is maintained at logical L after power-on.

In phase (2) shown in Fig. 4B, the third control circuit 206 latches the prohibiting signal setz to logical H, in response to the starter signal sttz and the set signal setR set to logical L by the second control unit 204. As a result, the output transistor 30 is prevented from being put in a low-impedance state at power-on and an abnormal current is prevented from flowing.

In phase (3) shown in Fig. 4B, when the mode register set command is executed, the mode register control circuit 10 outputs the register set signal rgwz. At the same time as the mode register 20 is set, the prohibiting signal setz generated by the third control circuit 206 is latched at logical L so that the driving signal mrrz is generated. Subsequently, execution of the mode register read command is enabled.

In phase (4) shown in Fig. 4B, the prohibiting signal setz is set by the third control circuit 206 at logical L as a result of the operation in phase (3). Therefore, the bus carrying the register read signal rgrz generated by the mode register control circuit 10 is activated. Further, the mode setting signal a8 is set to logical H to enable execution of the mode register read command, the mrspz signal in synchronism with the internal clock CLK is generated, and the register read signal rgrz is generated and output by the mode register control circuit 10. As a result, the mode selection signal MRDZ stored in the mode register 20 is output via the output transistor 30.

A description will now be given, with reference to Fig. 4C, of a specific operation according to the second embodiment executed when it is determined that the mode register read command is not specified, that is, a8 = L.

In phase (1) shown in Fig. 4C, the mrsqz signal or the mode setting signal a8 is set to logical L, so that the second control unit 204 sets the set signal setR to logical H. The set signal setR set to logical H by the second control unit 204 is maintained at logical H after power-on.

In phase (2) shown in Fig. 4C, the third control circuit 206 latches the prohibiting signal setz to logical L. As a result, it is determined that the mode register read

command is not specified. Thus, the output transistor 30 is prevented from being put in a low-impedance state.

In phase (3) shown in Fig. 4C, the prohibiting signal setz generated by the third control circuit 206 is latched at logical L so that execution of the mode register read command is enabled and the content of the register can be read at power-on.

As has been described, according to the mode register control circuit 10 provided with the second control unit 204 and the third control unit 206, execution of the mode register read command is disabled when the SDRAM 40 is turned on. By maintaining the output transistor 30 in a high-impedance state, an abnormal current is prevented from flowing into the output transistor 30 of the SDRAM 40.

In an idle state occurring after power-on, execution of the mode register read command is enabled subsequent to at least one execution of the mode register read command. Thus, an abnormal current is prevented from flowing in the output transistor 30 of the SDRAM 40.

A description will now be given of the SDRAM 40 according to the second embodiment.

As shown in Fig. 2, the SDRAM 40 comprises the mode register control circuit 10, the starter signal generating circuit 101 for generating an initializing signal sttz for instructing latching circuits to be initialized at power-on, the internal clock generating unit 102 for generating an internal clock clkiz in accordance with the external clock, the memory cell array 113, the read/write circuit 130 responsible for reading data from the memory cell 113 and writing data into the same, the input/output circuit 140 responsible for inputting and outputting data addresses and commands, the mode register 20 storing the operating mode of the input/output circuit, and the register read control circuit 111 for controlling reading from the mode register in synchronism with the external clock.

The read/write circuit 130 comprises the write data latching circuit 105, the write control circuit 106, the write amplifier circuit 107, the pipeline 108, the sense amplifier 112, the sense buffer 114, and the pipeline 115 which are described above.

The input/output circuit 140 comprises the external command latching circuit 103, the external address latching circuit 104, the external address decoding circuit 109, the external command decoding circuit 110, and the output transistor control circuit 120.

According to the SDRAM 40 provided with the mode register control circuit 10, it is possible to prevent an abnormal current from flowing in the output transistor (outTr) 30 by prohibiting execution of the mode register read command when the SDRAM 40 is turned on. In the idle state occurring after the SDRAM 40 is turned on, it is ensured that execution of the mode register read command is enabled on the condition that the mode register read command is executed so that an abnormal current is prevented from flowing in the output transistor (outTr) 30.

The present invention is not limited to the above described embodiments, and variations and modifications may be made without departing from the scope of the present invention.

Claims

1. A mode register control circuit (10) provided in a semiconductor device (40) and controlling operation of reading from a mode register of the semiconductor device (40) in response to an external command signal,

   said mode register control circuit (10) comprising a first control unit (102) for preventing reading out a content of the mode register from the semiconductor device (40), when the semiconductor device (40) begins to be supplied with power.

2. The mode register control circuit (10) as claimed in claim 1, wherein a content of the mode register is prevented from being read out by using an initializing signal for initializing a latch part for latching an external command and/or an external address externally fed to the semiconductor device (40) when said latch part is supplied with power.

3. A mode register control circuit (10) provided in a semiconductor device (40) and controlling operation of reading from a mode register of the semiconductor device (40) in response to an external command signal, said mode register control circuit (10) comprising a second control unit (104) which instructs, upon determining that a command other than a mode register read command instructing a content of the mode register to be read out is detected when the semiconductor device (40) is supplied with power, the mode register to execute the mode register read command even if a mode register set command has not been executed after a power supply voltage becomes stable.

4. A mode register control circuit (10) provided in a semiconductor device (40) and controlling operation of reading from a mode register of the semiconductor device (40) in response to an external command signal, said mode register control circuit (10) comprising a third control unit (106) which instructs, upon detecting that a mode register set command has been executed after the semiconductor is supplied with power, the mode register to execute a mode register read command instructing a content of the mode register to be read out.

5. The mode register control circuit (10) as claimed in claim 3, comprising a third control unit (106) which instructs, upon detecting that the mode register set command has been executed after the semiconductor is supplied with power, the mode register to execute the mode register read command.

6. The mode register control circuit (10) as claimed in claim 4, comprising a second control unit (104) which instructs, upon determining that a command other than the mode register read command is detected when the semiconductor device (40) is supplied with power, the mode register to execute the mode register read command even if the mode register set command has not been executed after a power supply voltage becomes stable.

7. A semiconductor device (40) comprising:

a starter signal generating circuit (101) for generating an initializing signal for initializing a latching circuit when the semiconductor device (40) is turned on;
an internal clock generating unit (102) for generating an internal clock signal in correspondence with an external clock signal;
a memory cell array (113);
a read/write circuit (130) for reading data from and writing data to the memory cell array (113);
an input/output circuit (140) for inputting and outputting data addresses and commands;
a mode register (20) for latching an operation mode of the input/output circuit (140);
a mode register control circuit (111) for controlling operation of reading from the mode register (20),

wherein
said mode register control circuit (111) is provided in a semiconductor device (40), controls operation of reading from the mode register (20) of the semiconductor device (40) in response to an external command signal, and comprises a first control unit (102) for preventing a content of the mode register from being read out from the semiconductor device (40), when the semiconductor device (40) beings to be supplied with power.

8. The semiconductor device (40) as claimed in claim 7, wherein a content of the mode register (20) is prevented from being read out by using an initializing signal for initializing a latch part for latching an external command and/or an external address externally fed to the semiconductor device (40) when said latch part is supplied with power.

9. A semiconductor device (40) comprising:

a starter signal generating circuit (101) for generating an initializing signal for initializing a latching circuit when the semiconductor device (40) is turned on;
an internal clock generating unit (102) for generating an internal clock signal in correspondence with an external clock signal;
a memory cell array (113);
a read/write circuit (130) for reading data from and writing data to the memory cell array (113);
an input/output circuit (140) for inputting and outputting data addresses and commands;
a mode register (20) for latching an operation mode of the input/output circuit (140);
a mode register control circuit (111) for controlling operation of reading from the mode register (20),

wherein
said mode register control circuit (111) is provided in a semiconductor device (40), controls operation of reading from the mode register (20) of the semiconductor device (40) in response to an external command signal and comprises a second control unit (104) which instructs, upon determining that a command other than a mode register read command instructing a content of the mode register (20) to be read out is detected when the semiconductor device (40) is supplied with power, the mode register (20) to execute the mode register read command even if a mode register set command has not been executed after a power supply voltage becomes stable.

10. A semiconductor device (40) comprising:

a starter signal generating circuit (101) for generating an initializing signal for initializing a latching circuit when the semiconductor device (40) is turned on;
an internal clock generating unit (102) for generating an internal clock signal in correspondence with an external clock signal;
a memory cell array (113);
a read/write circuit (130) for reading data from and writing data to the memory cell array (113);
an input/output circuit (140) for inputting and outputting data addresses and commands;
a mode register (20) for latching an operation mode of the input/output circuit (140);
a mode register control circuit (111) for controlling operation of reading from the mode register (20),

wherein
said mode register control circuit (111) is provided in a semiconductor device (40), controls operation of reading from the mode register (20) of the semiconductor device (40) in response to an external command signal, and comprises a third control unit (106) which instructs, upon detecting that a mode register set command has been executed after the semiconductor is supplied with power, the mode register (20) to execute a mode register read command instructing a content of the mode register (20) to be read out.

11. The semiconductor device (40) as claimed in claim 9, wherein the mode register control unit (111) comprises a third control unit (106) which instructs, upon detecting that the mode register set command has been executed after the semiconductor is supplied with power, the mode register (20) to execute the mode register read command.

12. The semiconductor device (40) as claimed in claim 10, wherein the mode register control circuit (111) comprises a second control unit (104) which instructs, upon determining that a command other than the mode register read command is detected when the semiconductor device (40) is supplied with power, the mode register (20) to execute the mode register read command even if the mode register set command has not been executed after a power supply voltage becomes stable.

FIG. 1A

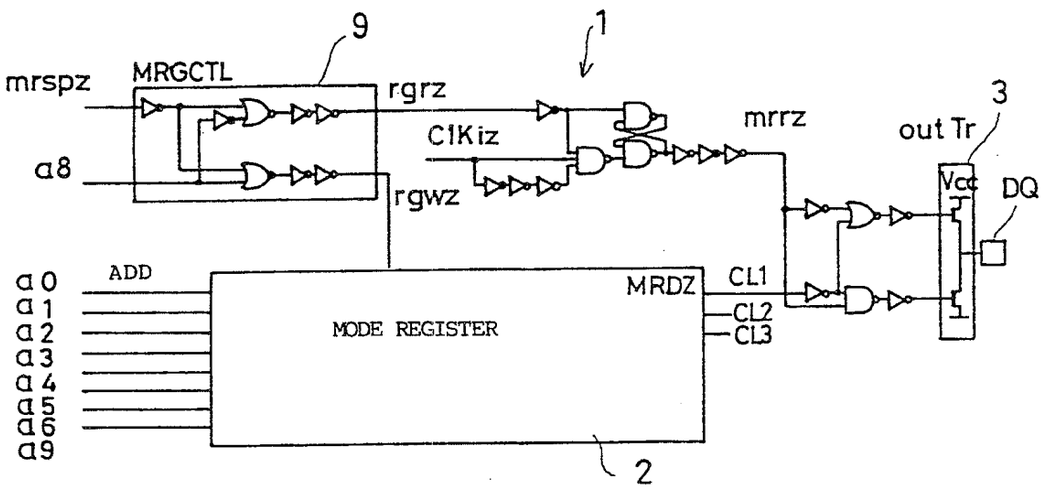


FIG. 1B

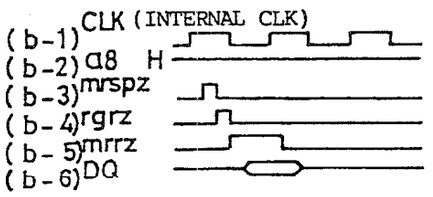


FIG. 2

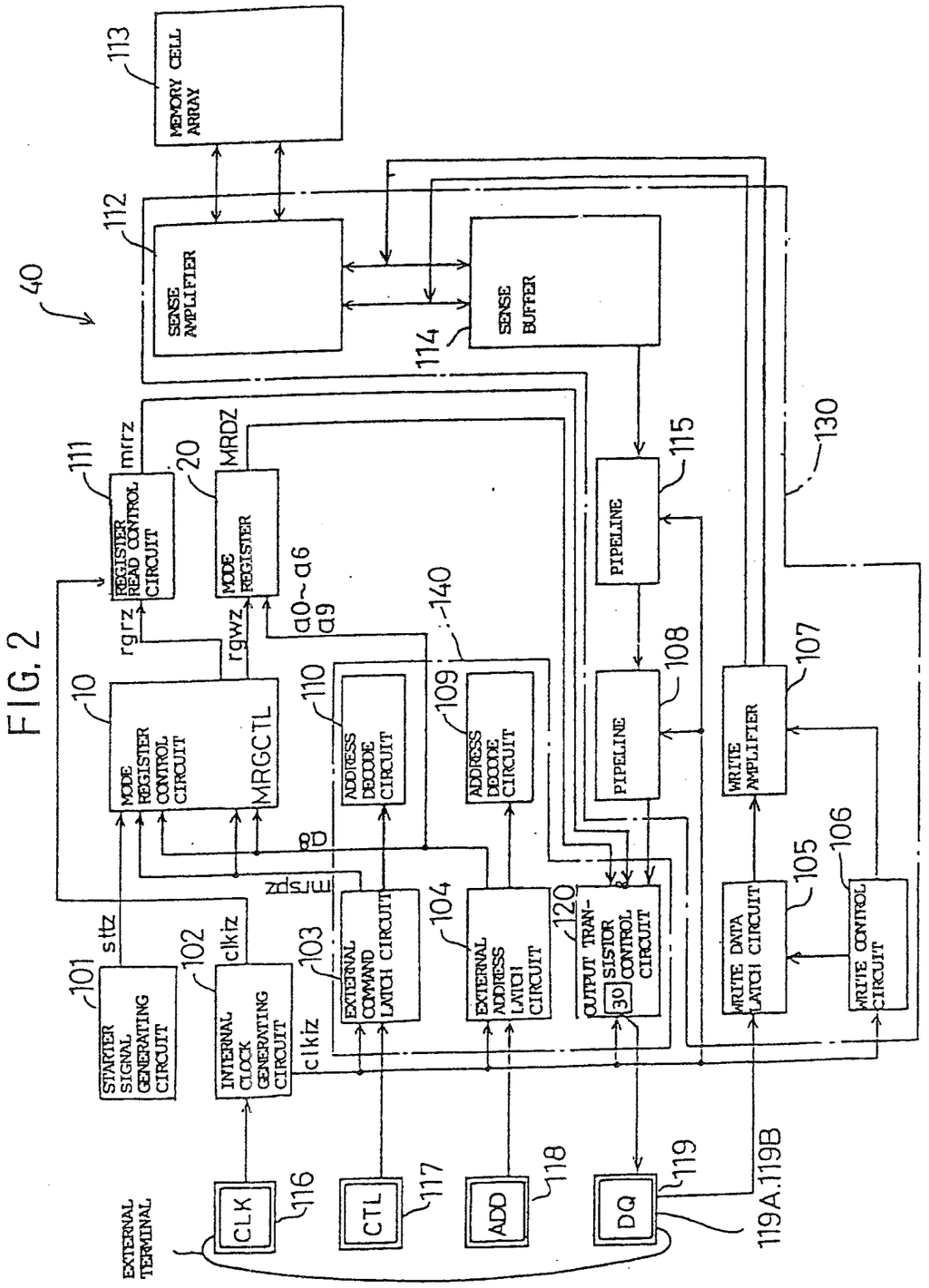


FIG. 3A

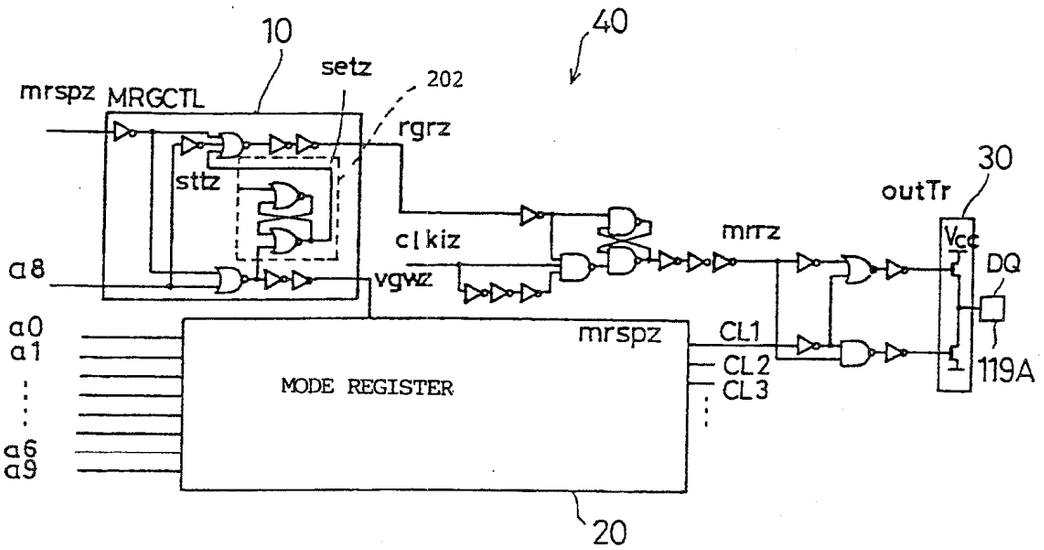


FIG. 3B

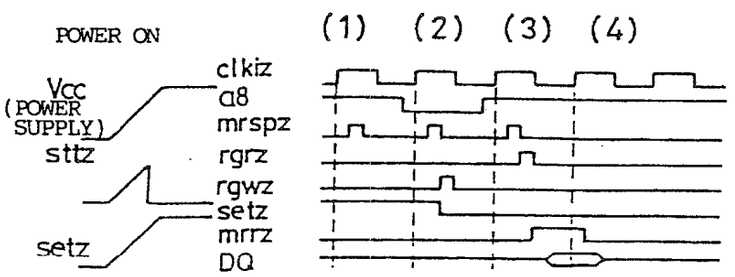


FIG. 4A

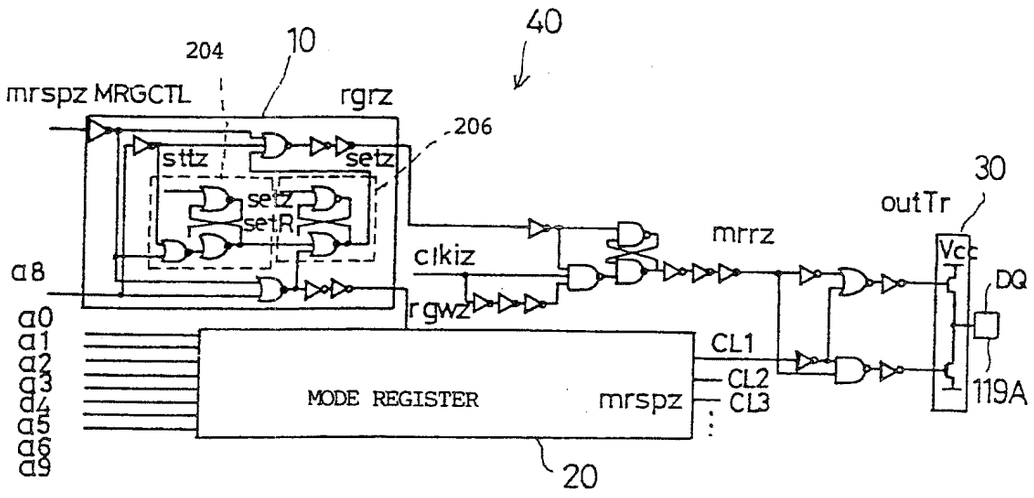


FIG. 4B

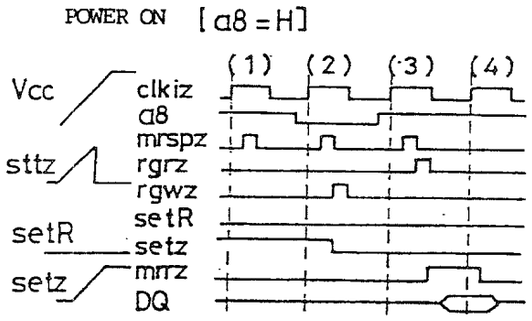
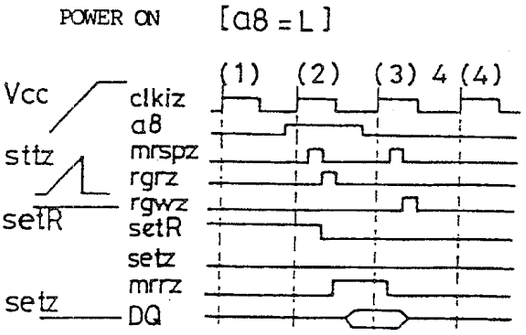


FIG. 4C



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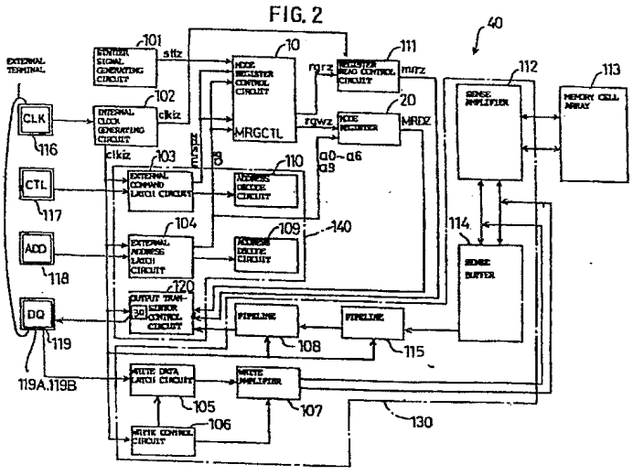
(54) Mode register control circuit and semiconductor device having the same

(57) A mode register control circuit (10) for a semiconductor device (40) includes a first control unit (202) for preventing the content of a mode register (20) from being read, using an initializing signal for instructing latching circuits (103, 104) to be initialized, the initialization being done in a transient occurring after the semiconductor device (40) is turned on; a second control unit (104) for instructing the mode register (20) to execute a mode register read command even if a mode register set command has not been executed, on the condition that an external command other than the mode register read command is detected when the semiconductor device (40) is turned on; or a third control unit (206) for instructing the mode register (20) to execute the mode register read command on the condition that the mode register set command is executed after the semiconductor device (40) is turned on.

FIG. 2



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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 5 448 528 A (NAGAI) * abstract * * column 3, line 29 - column 4, line 61; figures 1-3 *	1,3,4,7, 9	G11C7/00 G11C5/14
A	US 5 036 495 A (BUSCH ET AL.) * abstract * * column 2, line 21 - column 4, line 57; figures 1-7 *	1,3,4,7, 9	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 September 1997	Stecchina, A

CATEGORY OF CITED DOCUMENTS

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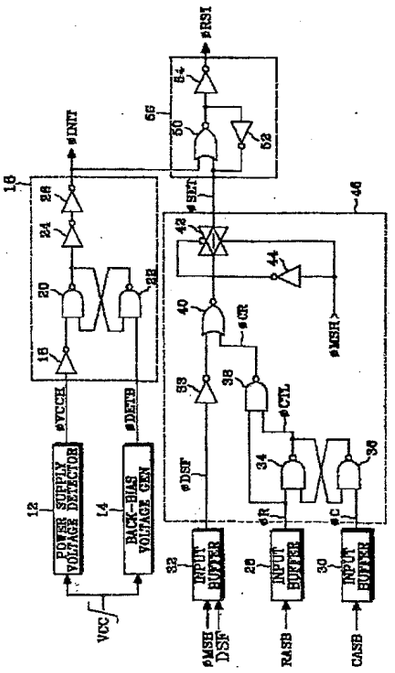
(54)【発明の名称】　半導体メモリ装置の初期化回路

(57)【要約】

【課題】　ＶＣＣの不安定により電源供給開始に伴う内部回路の初期化ができないような場合でも確実に初期化を行えるような初期化回路を提供する。

【解決手段】　外部提供の制御信号が所定の条件で活性入力されるとこれに応答して初期化信号を発生する初期化回路とする。即ち、従来の電源電圧検出部１２、バックバイアス電圧発生部１４、及び初期化信号発生部１６からなる構成に加え、バーＲＡＳ信号、バーＣＡＳ信号、及びモード選択信号ＤＳＦがＣＢＲモードで入力されるとこれに応答して第２初期化信号φＳＥＴを発生する第２初期化信号発生部４６と、第１初期化信号発生部１６による第１初期化信号φＩＮＩＴをラッチしまた第２初期化信号発生部４６による第２初期化信号φＳＥＴをラッチしてリセット信号φＲＳＴとし、内部回路へ出力する伝送部５６と、を備えるようにする。



【特許請求の範囲】

【請求項１】　電源供給開始に際して初期化信号を発生し内部回路を初期化する半導体メモリ装置の初期化回路において、

外部から提供される制御信号に応じて初期化信号を発生するようにしたことを特徴とする初期化回路。

【請求項２】　外部から提供される複数の制御信号が所定の条件で活性入力されるとこれに応答して初期化信号を発生する請求項１記載の初期化回路。

【請求項３】　外部から提供される第１制御信号及び第２制御信号の活性化に応答して前記第１制御信号の活性期間内で制御クロックを発生し、該制御クロックをモード選択信号による論理と組合せて初期化信号を発生する初期化信号発生部と、該初期化信号発生部による初期化信号をラッチして出力する伝送部と、を備えてなる請求項２記載の初期化回路。

【請求項４】　第１制御信号が行アドレスストローブ信号、第２制御信号が列アドレスストローブ信号であり、これらがＣＢＲモードで入力されると初期化信号を発生する請求項３記載の初期化回路。

【請求項５】　電源供給開始に際して初期化信号を発生し内部回路を初期化する半導体メモリ装置の初期化回路において、

電源電圧の入力に応じて第１初期化信号を発生する第１初期化信号発生部と、メモリアクセスに際して活性化される制御信号及び動作モードを決定するためのモード選択信号に応答して第２初期化信号を発生する第２初期化信号発生部と、前記第１、第２初期化信号をラッチして出力する伝送部と、を備え、前記第１初期化信号又は前記第２初期化信号を内部回路へ提供して初期化することを特徴とする初期化回路。

【請求項６】　第２初期化信号発生部は、行アドレスストローブ信号及び列アドレスストローブ信号の活性化に応答して行アドレスストローブ信号の活性期間内で制御クロックを発生し、該制御クロックをモード選択信号による論理と組合せて第２初期化信号を発生する請求項５記載の初期化回路。

【請求項７】　第２初期化信号発生部は、行アドレスストローブ信号を遅延させた遅延クロックに従い開閉して第２初期化信号を伝送部へ送る伝送ゲートを有する請求項６記載の初期化回路。

【請求項８】　行アドレスストローブ信号及び列アドレスストローブ信号がＣＢＲモードで提供されるとときに第２初期化信号を発生する請求項６又は請求項７記載の初期化回路。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は半導体メモリ装置に関し、特に、その内部回路の初期化回路に関する。

【０００２】

【従来の技術】大容量・高集積化が進むにつれて半導体メモリ装置は多機能、複雑化してきており、このような半導体メモリ装置では、内部回路をリセットして初期動作条件を設定する初期化回路が備えられている。初期化回路は、外部から初期供給される電源電圧ＶＣＣのレベルを検出して所定のパルス幅のリセットパルスを発生するパワーオンリセット回路と呼ばれるものが一般的である。即ち、パワーオンリセット回路は、電源電圧の供給による電圧レベルを検出して予め設定された所定のレベル以上になると内部回路を初期化する初期化パルス信号を発生する回路で、図１にその構成を示している。

【０００３】電源電圧検出部１２は、電源電圧ＶＣＣの入力レベルを検出して電源電圧検出信号φＶＣＣＨを発生し、また、バックバイアス電圧発生部１４は、電源電圧ＶＣＣの入力状態が安定した後にバックバイアス電圧ＶＢＢを発生し、そしてこれを検出してバックバイアス検出信号φＤＥＴＢを出力する。発生された電源電圧検出信号φＶＣＣＨ及びバックバイアス検出信号φＤＥＴＢは初期化信号発生部１６へ提供され、これに従って初期化信号発生部１６は、電源電圧検出信号φＶＣＣＨの発生からバックバイアス検出信号φＤＥＴＢの発生までの間で初期化信号φＩＮＩＴを発生する。図示のように初期化信号発生部１６は、電源電圧検出信号φＶＣＣＨにより出力端子が論理“ハイ”セットされ、バックバイアス検出信号φＤＥＴＢにより出力端子が論理“ロウ”リセットされるフリップフロップの構成とされる。

【０００４】図２には、図１の初期化回路のタイミング図を示してある。チップに対し電源供給が開始され電源電圧ＶＣＣが０Ｖから徐々に増加すると、電源電圧検出部１２は、例えば３Ｖの動作レベルまで上昇する電源電圧ＶＣＣの入力状態を検出した電源電圧検出信号φＶＣＣＨを発生し、適正時間後に論理“ロウ”へ遷移させる。このように出力される電源電圧検出信号φＶＣＣＨが初期化信号発生部１６内のインバータ１８に提供される。インバータ１８は、動作レベルまで上昇する電源電圧ＶＣＣの入力状態を検出した電源電圧検出信号φＶＣＣＨに従って、互いの出力と入力を交差接続したＮＡＮＤゲート２０，２２からなるＲＳフリップフロップをセットし、その結果、インバータ２４，２６を通じて論理“ハイ”の初期化信号φＩＮＩＴが出力される。この状態は、インバータ１８から論理“ハイ”が出力され且つＮＡＮＤゲート２２に論理“ロウ”が入力されるまで継続する。

【０００５】一方、電源電圧ＶＣＣにより動作するバックバイアス電圧検出部１４は、入力される電源電圧ＶＣＣが予め設定された例えば３Ｖの動作レベルで安定化すると、図２に示すように負電圧－Ｖのバックバイアス電圧ＶＢＢを発生する。そして、負電圧－Ｖのレベルが例えば－３Ｖで安定するとバックバイアス検出信号φＤＥＴＢを論理“ロウ”遷移させる。このようにしてバック

バイアス検出信号φＤＥＴＢが論理“ロウ”遷移し、これが初期化信号発生部１６内のＮＡＮＤゲート２２へ入力されると、ＮＡＮＤゲート２０，２２よりなるＲＳフリップフロップがリセットされ、インバータ２４，２６を通じて初期化信号φＩＮＩＴは論理“ロウ”遷移する。

【０００６】以上のようにして発生されるパルスの初期化信号φＩＮＩＴが内部回路の各リセットノードへ供給される結果、初期化が行われる。

【０００７】

【発明が解決しようとする課題】図示のような従来の初期化回路では、電源電圧ＶＣＣの入力が不安定な場合には誤動作を起こす可能性がある。例えば、電源電圧ＶＣＣが０Ｖから動作レベルまで上昇する時間が数ｍｓ（通常は２００μｓ程度）以上かかってしまう場合（図２中点線）、或いは、何らかの理由で電源電圧ＶＣＣのレベルが内部回路の動作電圧より低く入力される場合は、電源電圧検出部１２が誤動作して電源電圧検出信号φＶＣＣＨが正常に出力されなくなる。このような事態になると、初期化信号発生部１６による初期化信号φＩＮＩＴのパルス幅が非常に短くなるか、或いは出力されなくなり、内部回路の初期化が行われなくなってしまう。

【０００８】

【課題を解決するための手段】上記課題に鑑みて本発明では、外部から提供される制御信号に応じて初期化信号を発生し内部回路の初期化を実行する初期化回路を提供する。好ましくは、外部から提供される複数の制御信号が所定の条件で活性入力されるとこれに応答して初期化信号を発生する初期化回路とする。即ち、パワーアップ時に電源電圧の不安定で誤動作を生じる可能性がある場合でも、別途の初期化情報の入力に応答して内部回路を確実に初期化できる初期化回路を提供する。例えば、バーＣＡＳ信号及びバーＲＡＳ信号がＣＢＲ(CAS before RAS)モードで入力されるとこれに応答して内部回路を初期化する初期化回路とするものである。

【０００９】具体的回路構成として本発明によれば、外部から提供される第１制御信号及び第２制御信号の活性化に応答して前記第１制御信号の活性期間内で制御クロックを発生し、該制御クロックをモード選択信号による論理と組合せて初期化信号を発生する初期化信号発生部と、該初期化信号発生部による初期化信号をラッチして出力する伝送部と、を備えてなる初期化回路とする。この場合、第１制御信号を行アドレスストローブ信号、第２制御信号を列アドレスストローブ信号とし、これらがＣＢＲモードで入力されると初期化信号を発生するようにしておくとよい。

【００１０】また、本発明によれば、電源供給開始に際して初期化信号を発生し内部回路を初期化する半導体メモリ装置の初期化回路において、電源電圧の入力に応じて第１初期化信号を発生する第１初期化信号発生部と、メモリアクセスに際して活性化される制御信号及び動作モードを決定するためのモード選択信号に応答して第２初期化信号を発生する第２初期化信号発生部と、前記第１、第２初期化信号をラッチして出力する伝送部と、を備え、前記第１初期化信号又は前記第２初期化信号を内部回路へ提供して初期化することを特徴とする。この場合の第２初期化信号発生部は、行アドレスストローブ信号及び列アドレスストローブ信号の活性化に応答して行アドレスストローブ信号の活性期間内で制御クロックを発生し、該制御クロックをモード選択信号による論理と組合せて第２初期化信号を発生するものとすることができる。またこのときの第２初期化信号発生部は、行アドレスストローブ信号を遅延させた遅延クロックに従い開閉して第２初期化信号を伝送部へ送る伝送ゲートを有するものとするとよい。そして、行アドレスストローブ信号及び列アドレスストローブ信号がＣＢＲモードで提供されるとときに第２初期化信号を発生するようにしておくとよい。

【００１１】

【発明の実施の形態】以下、本発明の実施形態につき添付図面を参照して詳細に説明する。

【００１２】図３に、一実施形態としてＤＲＡＭにおける初期化回路の例を示す。図示のように図１同様の構成に加えて、外部制御信号がＣＢＲモードで入力されるとこれに応答して第２初期化信号φＳＥＴを発生する第２初期化信号発生部４６と、図１同様の第１初期化信号発生部１６による第１初期化信号φＩＮＩＴをラッチした第２初期化信号発生部４６による第２初期化信号φＳＥＴをラッチしてリセット信号φＲＳＴとし、内部回路のリセットノードへ出力する伝送部５６と、を備えている。

【００１３】この初期化回路にパワーアップで電源電圧ＶＣＣの供給が開始されると、電源電圧検出部１２、バックバイアス電圧発生部１４、及び第１初期化信号発生部１６からなる部分により、図２同様のタイミングをもって第１初期化信号φＩＮＩＴが発生され、伝送部５６内のＮＯＲゲート５０へ提供される。このときＮＯＲゲート５０のもう一方の入力となる第２初期化信号φＳＥＴは論理“ロウ”の状態にある。従ってＮＯＲゲート５０は、第１初期化信号φＩＮＩＴに応じる論理“ロウ”を出力する。このＮＯＲゲート５０の出力はインバータ５２でラッチされると共にインバータ５４を経てリセット信号φＲＳＴとして出力される。即ち、電源電圧ＶＣＣの入力により論理“ハイ”パルスの第１初期化信号φＩＮＩＴが発生するとこれに従うリセット信号φＲＳＴが伝送部５６から発生され、内部回路が初期化される。尚、第１初期化信号φＩＮＩＴは直接的に内部回路へ提供されるようにしておいてもよい。

【００１４】一方、初期化情報として使用する制御信号が予め設定された真理値表を満足する条件で第２初期化

信号発生部４６へ提供されると、第２初期化信号発生部４６は、所定期間論理“ハイ”となるパルスの第２初期化信号φＳＥＴを図４のタイミング図のようにして発生する。本例における初期化情報は、メモリアクセスに際して活性化される第１制御信号及び第２制御信号としての行アドレスストローブ信号ＲＡＳＢ（＝バーＲＡＳ）及び列アドレスストローブ信号ＣＡＳＢ（＝バーＣＡＳ）と、メモリの動作モードを決定するモード選択信号ＤＳＦである。

【００１５】上記３種類の初期化情報がＣＢＲモードで入力されると、チップに備えられる入力バッファ２８，３０，３２からそれぞれ行アドレスクロックφＲ、列アドレスクロックφＣ、モード選択クロックφＤＳＦが発生される。モード選択クロックφＤＳＦは、モード選択信号ＤＳＦに従い論理“ハイ”に活性化され、行アドレスクロックφＲを遅延させた遅延クロックφＭＳＨが非活性化されるまで活性状態を維持する。

【００１６】行アドレスストーブ信ＲＡＳＢによる行アドレスクロックφＲはＮＡＮＤゲート３４の入力となり、列アドレスストローブＣＡＳＢによる列アドレスクロックφＣはＮＡＮＤゲート３６の入力となる。これらＮＡＮＤゲート３４，３６の他方の入力は、相手側の出力と互いに交差接続される。従って、列アドレスクロックφＣが論理“ハイ”へ活性化されると、これに応じるＮＡＮＤゲート３４，３６により論理“ハイ”の制御クロックφＣＴＬが発生される。発生した制御クロックφＣＴＬは、ＮＡＮＤゲート３８へ入力されて行アドレスクロックφＲとＮＡＮＤ演算され、行アドレスストローブ信号ＲＡＳＢの活性期間内で制御クロックφＣＲが発生される。この例では、行アドレスストローブ信号ＲＡＳＢの活性化後に列アドレスストローブ信号ＣＡＳＢが非活性化されるまでの間で制御クロックφＣＲは発生される。

【００１７】制御クロックφＣＲはＮＯＲゲート４０へ入力され、インバータ３３により反転したモード選択クロックφＤＳＦとＮＯＲ演算される。これによるＮＯＲゲート４０の出力は、遅延クロックφＭＳＨにより開閉する伝送ゲート４２を介し第２初期化信号φＳＥＴとして伝送部５６のＮＯＲゲート５０へ提供される。伝送ゲート４２は、遅延クロックφＭＳＨの論理“ハイ”活性でオンスイッチされる構成である。

【００１８】伝送部５６では、この場合論理“ロウ”で入力される第１初期化信号φＩＮＩＴと上記のようにして論理“ハイ”で入力される第２初期化信号φＳＥＴとをＮＯＲゲート５０が演算する結果、インバータ５２，５４の入力が論理“ロウ”となり、その論理状態がインバータ５２でラッチされると共にインバータ５４から論理“ハイ”のリセット信号φＲＳＴが出力され、内部回路が初期化される。

【００１９】第２初期化信号φＳＥＴにより論理“ハイ”となったリセット信号φＲＳＴは、列アドレスストローブ信号ＣＡＳＢが非活性化されるまでの間そのまま維持される。即ち、列アドレスストローブ信号ＣＡＳＢが論理“ハイ”に遷移すると、入力バッファ３０から出力される列アドレスクロックφＣが論理“ロウ”に非活性化され、そしてＮＡＮＤゲート３４，３６による制御クロックφＣＴＬが論理“ロウ”になる。これにより制御クロックφＣＲが論理“ハイ”になり、第２初期化信号φＳＥＴは論理“ロウ”へ遷移する。つまり、行アドレスストローブ信号ＲＡＳＢの活性期間で列アドレスストローブ信号ＣＡＳＢが非活性化されると第２初期化信号φＳＥＴは論理“ロウ”へ遷移し、これに従って伝送部５６の論理状態が変化してリセット信号φＲＳＴが初期化解除となる。

【００２０】この実施形態では、特に１つの伝送部５６を用いて第１初期化信号発生部１６による第１初期化信号φＩＮＩＴ及び第２初期化信号発生部４６による第２初期化信号φＳＥＴのいずれかをリセット信号φＲＳＴとして供給する例を示したが、両初期化信号をそれぞれ独立的に内部回路へ提供する構成でも初期化動作は可能である。

【００２１】

【発明の効果】本発明によれば、パワーアップによる初期化信号発生及び初期化条件を満たす制御信号による初期化情報に応答しての初期化信号発生の両方を可能としたので、パワーアップリセットで誤動作が発生したとしても、例えば行アドレスストローブ信号の活性サイクルの始めで確実に初期化を実行することができる。従って、より誤動作が少なく信頼性の高い半導体メモリ装置を提供することができるようになる。

【図面の簡単な説明】

【図１】一般的な初期化回路を示す回路図。

【図２】図１に示す初期化回路の動作を説明する信号波形図。

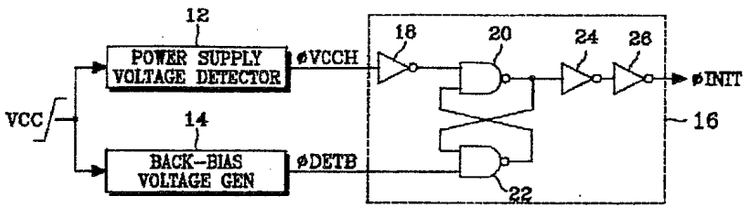
【図３】本発明による初期化回路の実施形態を示す回路図。

【図４】図３に示す初期化回路の動作を説明する信号波形図。

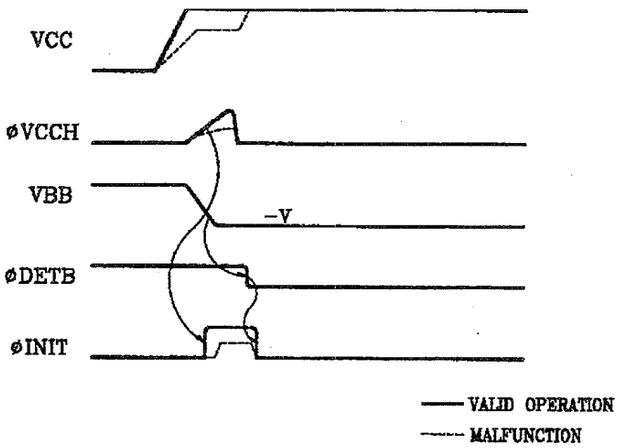
【符号の説明】

１２　電源電圧検出部
１４　バックバイアス電圧発生部
１６　第１初期化信号発生部
２８，３０，３２　入力バッファ
４６　第２初期化信号発生部
５６　伝送部

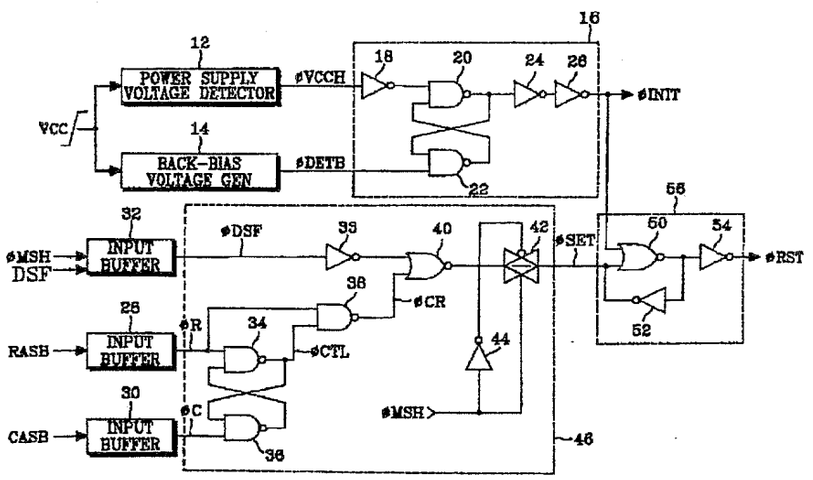
【図1】



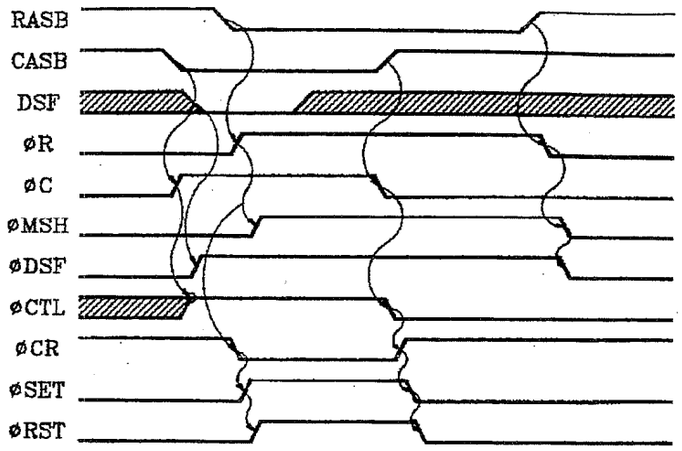
【図2】



【図3】



【図4】



Docket No.: GR 98 P 1989

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Gunnar Krause
Applic. No.	:	09/343,431
Filed	:	June 30, 1999
Title	:	Dynamic Semiconductor Memory Device And Method For Initializing A Dynamic Semiconductor Memory Device
Art Unit	:	2818

ASSOCIATE POWER OF ATTORNEY

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

S i r :

Please recognize MARK P. WEICHSELBAUM (Reg. No. 43,248) as my associate in the matter in the above-identified application, with full powers. Please continue addressing all communications to the following address:

Lerner and Greenberg, P.A.
P.O. Box 2480
Hollywood, Florida 33022-2480

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308

For Applicant

Date: December 20, 1999

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Tel: (954) 925-1100
Fax: (954) 925-1101

/bmb

UNITED STA DEPARTMENT OF COMMERCE
Patent and T. demark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
09/343,431	06/30/99	KRAUSE	GR98P1989

EXAMINER	
G	

MMC1/0717

LERNER AND GREENBERG PA
PO BOX 2480
HOLLYWOOD FL 33022-2480

ART UNIT	PAPER NUMBER
2824	8

DATE MAILED: 07/17/00

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☐ This communication is responsive to _____.

☑ The allowed claim(s) ~~is~~/are 1-13.

☐ The drawings filed on _____ are acceptable.

☑ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☑ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☑ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR REPLY to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☐ Applicant MUST submit NEW FORMAL DRAWINGS

☐ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☑ Notice of References Cited, PTO-892

☑ Information Disclosure Statement(s), PTO-1449, Paper No(s). 8

☑ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☐ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☑ Examiner's Statement of Reasons for Allowance

Vu A. Le
Primary Examiner

PTOL-37 (Rev. 8/97)

*U.S. GPO: 1998-433-221/82108

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance: the present invention relates to power on circuit. The independent claims 1 and 11 recite an initialization circuit for controlling a switch-on operation of a DRAM comprising an internal voltage regulation and detection outputting supply voltage stable signal and an enable circuit receiving the supply voltage stable signal and externally applied further command signals, said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit. The PRIOR ART fails to disclose or suggest such the initialization circuit having the enable circuit as described in the independent claims 1 and 11, therefore, claims 1 -13 are in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cu Le whose telephone number is (703) 308-1497.

Vu A. Le
July 11, 2000

Vu A. Le
Primary Examiner

Notice of References Cited

Application No.	Applicant(s)		
09/344,431	Krause		
Examiner	Group Art Unit	Page 8 of ___	
Vu Le	2824		

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
*	A	JP894446	4/13/99	Itou	365	222
*	B	JP841724	11/24/98	Ebel et al	365	226
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

*		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	U		
	V		
	W		
	X		

* A copy of this reference is not being funished with this Office action.
(See Manual of Patent Examining Procedure, Section 707.05(a).)

Form PTO 948 (Rev. 8-98) U.S. DEPARTMENT OF COMMERCE - Patent and Trademark Office Application No. 09/343,431

NOTICE OF DRAFTSPERSON'S PATENT DRAWING REVIEW

The drawing(s) filed (insert date) 06/30/99 are:

A. ☑ approved by the Draftsperson under 37 CFR 1.84 or 1.152.

B. ☐ objected to by the Draftsperson under 37 CFR 1.84 or 1.152 for the reasons indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawing must be sumitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings: Black ink. Color.
   - ____ Color drawings are not acceptable until petiton is granted. Fig(s) _____
   - ____ Pencil and non black ink not permitted. Fig(s) _____
2. PHOTOGRAPHS. 37 CFR 1.84 (b)
   - ____ 1 full-tone set is required. Fig(s) _____
   - ____ Photographs not properly mounted (must use brystol board or photographic double-weight paper). Fig(s) _____
   - ____ Poor quality (half-tone). Fig(s) _____
3. TYPE OF PAPER. 37 CFR 1.84(e)
   - ____ Paper not flexible, strong, white, and durable. Fig(s) _____
   - ____ Erasures, alterations, overwritings, interlineations, folds, copy machine marks not accepted. Fig(s) _____
   - ____ Mylar, velum paper is not acceptable (too thin). Fig(s) _____
4. SIZE OF PAPER. 37 CFR 1.84(f): Acceptable sizes:
   - ____ 21.0 cm by 29.7 cm (DIN size A4)
   - ____ 21.6 cm by 27.9 cm (8 1/2 x 11 inches)
   - ____ All drawing sheets not the same size. Sheet(s) _____
   - ____ Drawings sheets not an acceptable size. Fig(s) _____
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:

   Top 2.5 cm Left 2.5cm Right 1.5 cm Bottom 1.0 cm
   SIZE: A4 Size

   Top 2.5 cm Left 2.5 cm Right 1.5 cm Bottom 1.0 cm
   SIZE: 8 1/2 x 11

   Margins not acceptable. Fig(s) _____
   _____ Top (T) _____ Left (L)
   _____ Right (R) _____ Bottom (B)
6. VIEWS. 37 CFR 1.84(h)
   REMINDER: Specification may require revision to correspond to drawing changes.
   Partial views. 37 CFR 1.84(h)(2)
   - ____ Brackets needed to show figure as one entity. Fig(s) _____
   - ____ Views not labeled separately or properly. Fig(s) _____
   - ____ Enlarged view not labeled separetely or properly. Fig(s) _____
7. SECTIONAL VIEWS. 37 CFR 1.84 (h)(3)
   - ____ Hatching not indicated for sectional portions of an object. Fig(s) _____
   - ____ Sectional designation should be noted with Arabic or Roman numbers. Fig(s) _____
8. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
   - ____ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig(s) _____
9. SCALE. 37 CFR 1.84(k)
   - ____ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig(s) _____
10. CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(i)
    - ____ Lines, numbers & letters not uniformly thick and well defined, clean, durable, and black (poor line quality). Fig(s) _____
11. SHADING. 37 CFR 1.84(m)
    - ____ Solid black areas pale. Fig(s) _____
    - ____ Solid black shading not permitted. Fig(s) _____
    - ____ Shade lines, pale, rough and blurred. Fig(s) _____
12. NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.84(p)
    - ____ Numbers and reference characters not plain and legible. Fig(s) _____
    - ____ Figure legends are poor. Fig(s) _____
    - ____ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(1) Fig(s) _____
    - ____ English alphabet not used. 37 CFR 1.84(p)(2) Figs _____
    - ____ Numbers, letters and reference characters must be at least .32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig(s) _____
13. LEAD LINES. 37 CFR 1.84(q)
    - ____ Lead lines cross each other. Fig(s) _____
    - ____ Lead lines missing. Fig(s) _____
14. NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
    - ____ Sheets not numbered consecutively, and in Arabic numerals beginning with number 1. Sheet(s) _____
15. NUMBERING OF VIEWS. 37 CFR 1.84(u)
    - ____ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig(s) _____
16. CORRECTIONS. 37 CFR 1.84(w)
    - ____ Corrections not made from prior PTO-948 dated _____
17. DESIGN DRAWINGS. 37 CFR 1.152
    - ____ Surface shading shown not appropriate. Fig(s) _____
    - ____ Solid black shading not used for color contrast. Fig(s) _____

COMMENTS

REVIEWER LAM DATE 12/29/99 TELEPHONE NO. _____

ATTACHMENT TO PAPER NO. 8

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities--37 CFR 1.85

File new drawings with the changes incorporated therein. The application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application, should be placed on the back of each sheet of drawings in accordance with 37 CFR 1.84(c). Applicant may delay filing of the new drawings until receipt of the Notice of Allowability (PTOL-37). Extensions of time may be obtained under the provisions of 37 CFR 1.136. The drawing should be filed as a separate paper with a transmittal letter addressed to the Drawing Processing Branch.

2. Timing for Corrections

Applicant is required to submit **acceptable** corrected drawings within the three-month shortened statutory period set in the Notice of Allowability (PTOL-37). If a correction is determined to be unacceptable by the Office, applicant must arrange to have acceptable corrections resubmitted within the original three-month period to avoid the necessity of obtaining an extension of time and paying the extension fee. Therefore, applicant should file corrected drawings as soon a possible.

Failure to take corrective action within set (or extended) period will result in **ABANDONMENT** of the Application.

3. Corrections other than Informalities Noted by the Drawing Review Branch on the Form PTO-948

All changes to the drawings, other than informalities noted by the Drawing Review Branch, **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

MMC1/0717

LERNER AND GREENBERG PA
PO BOX 2480
HOLLYWOOD FL 33022-2480

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/343,431	06/30/99	013	LE, V	2824 07/17/00

First Named Applicant	35 USC 154(b) term ext. =	0 Days.
KRAUSE.		

TITLE OF INVENTION: DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INTIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 6R98P1989	365-226.000	P31	UTILITY	NO	$1210.00	10/17/00

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or

B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 06/30/99. (0651-0033)

PART B—ISSUE FEE TRANSMITTAL

Complete and mail this form, together with applicable fees, to: **Box ISSUE FEE**
Assistant Commissioner for Patents
Washington, D.C. 20231

JC

BP

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

MMC1/0717

LERNER AND GREENBERG PA
PO BOX 2480
HOLLYWOOD FL 33022-2480

OIPE
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PATENT & TRADEMARK OFFICE
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Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

RALPH E. LOCHER
REG. NO. 41,947 (Depositor's name)

(Signature)

Sept 28, 2000 (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/343,431	06/30/99	013	LE, V 2824	07/17/00

First Named Applicant: KRAUSE. 35 USC 154(b) term ext. = 0 Days.

TITLE OF INVENTION: DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INTIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 GR98P1989	365-226.000	P31	UTILITY	NO	$1210.00	10/17/00

1. Change of correspondence address or indication of " Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Herbet L. Lerner
2 Laurence A. Greenber
3 Werner H. Stemer

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropiate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a subsitiute for filing an assignment.

(A) NAME OF ASSIGNEE: Siemens Aktiengesellschaft

(B) RESIDENCE: (CITY & STATE OR COUNTRY): Muenchen, Germany

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

☒ Issue Fee

☐ Advance Order - # of Copies _____

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☐ Advance Order - # of Copies _____

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) RALPH E. LOCHER REG. NO. 41,947 (Date) 9/28/00

NOTE; The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

10/04/2000 MBERHE1 00000117 09343431
01 FC:142 1210.00 OP

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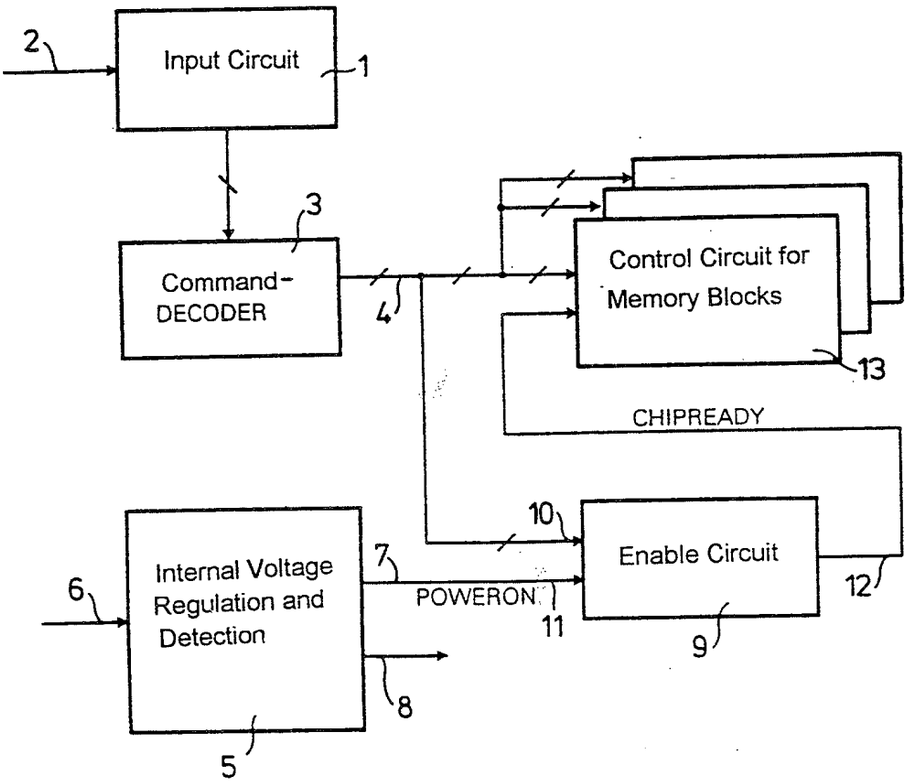
TRANSMIT THIS FORM WITH FEE

PRINT OF DRAWINGS
AS ORIGINALLY FILE

365/226

Fig 1



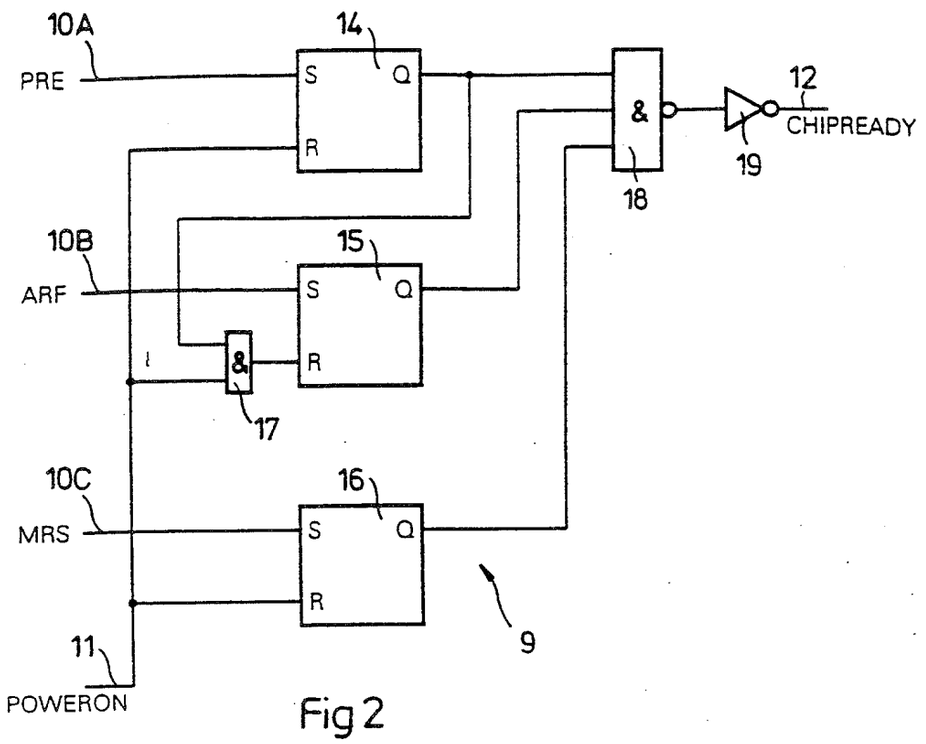


Fig 2

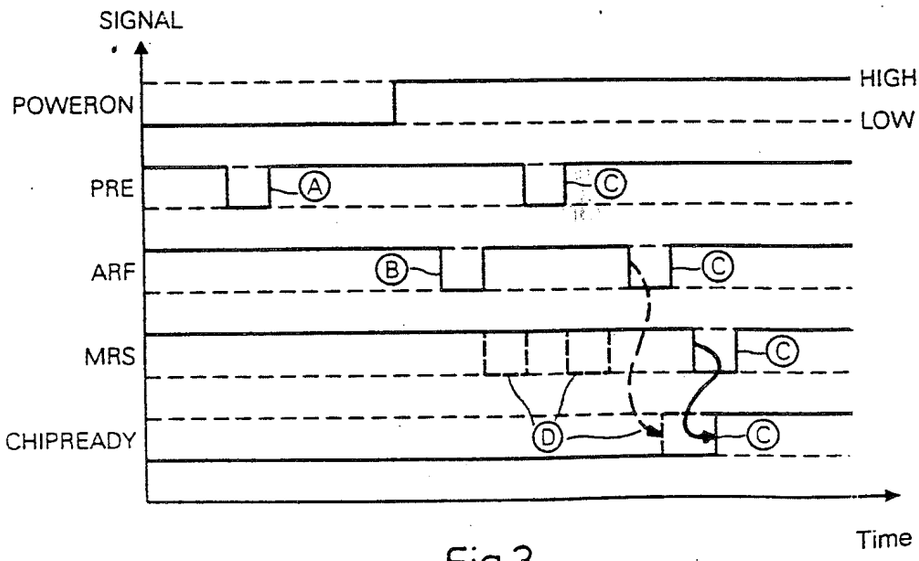


Fig 3

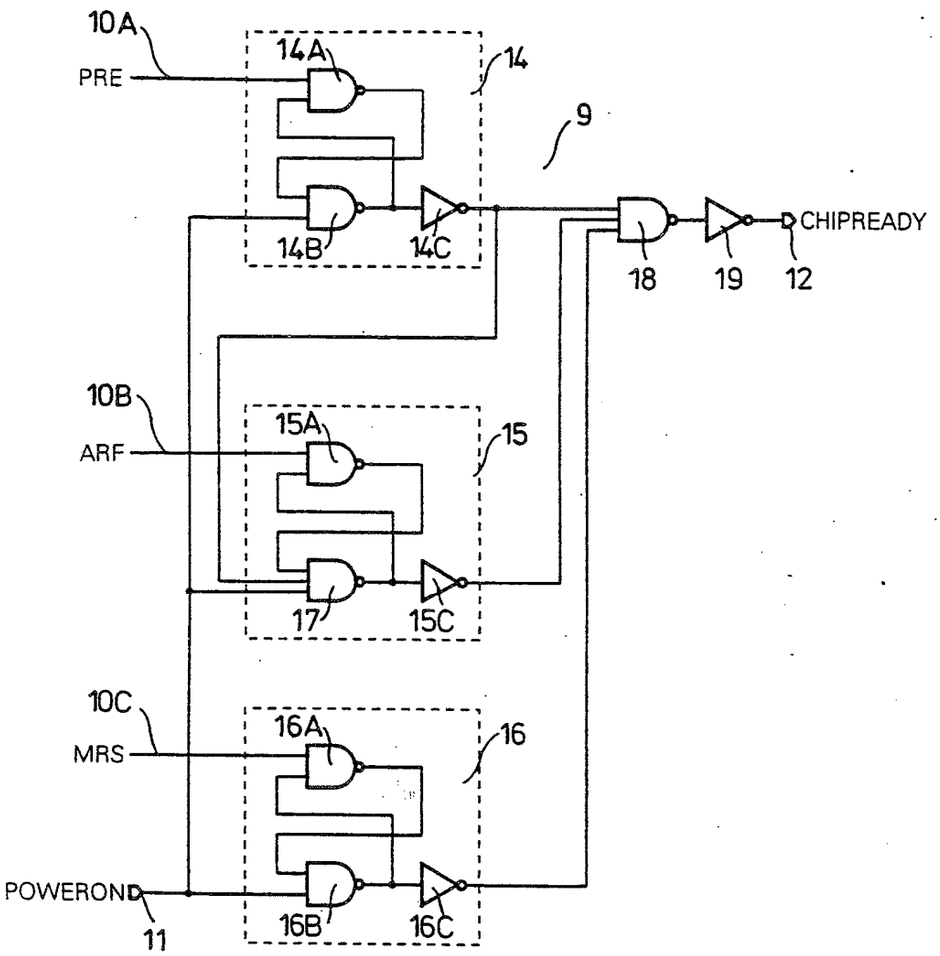
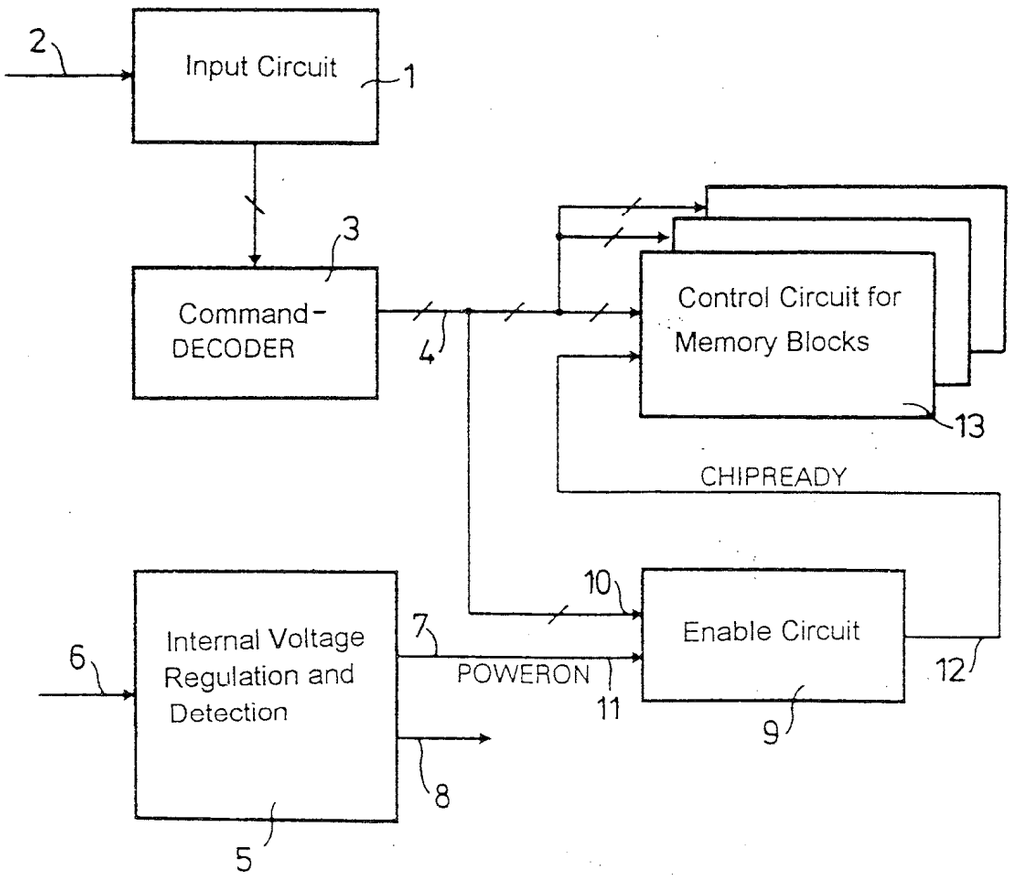


Fig 4

Fig 1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Input Circuit
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3
Command-
DECODER
4
Control Circuit for
Memory Blocks
13
CHIPREADY
10
Enable Circuit
12
9
7
POWERON
11
6
Internal Voltage
Regulation and
Detection
8
5

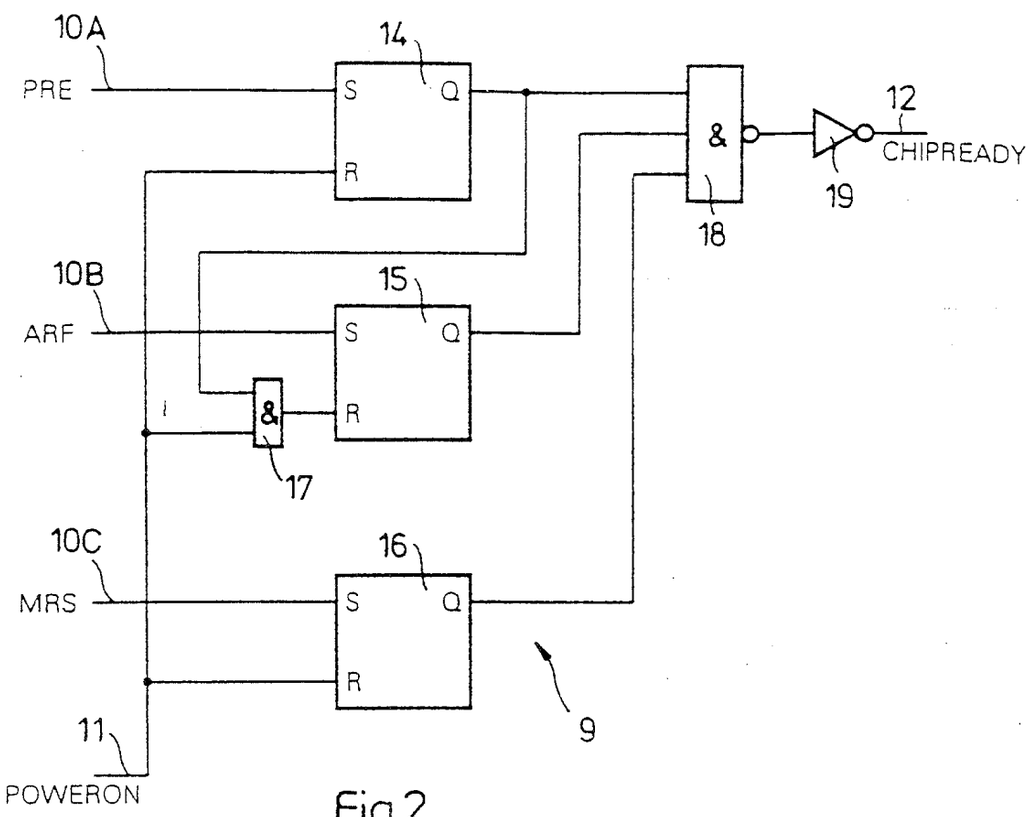


Fig 2

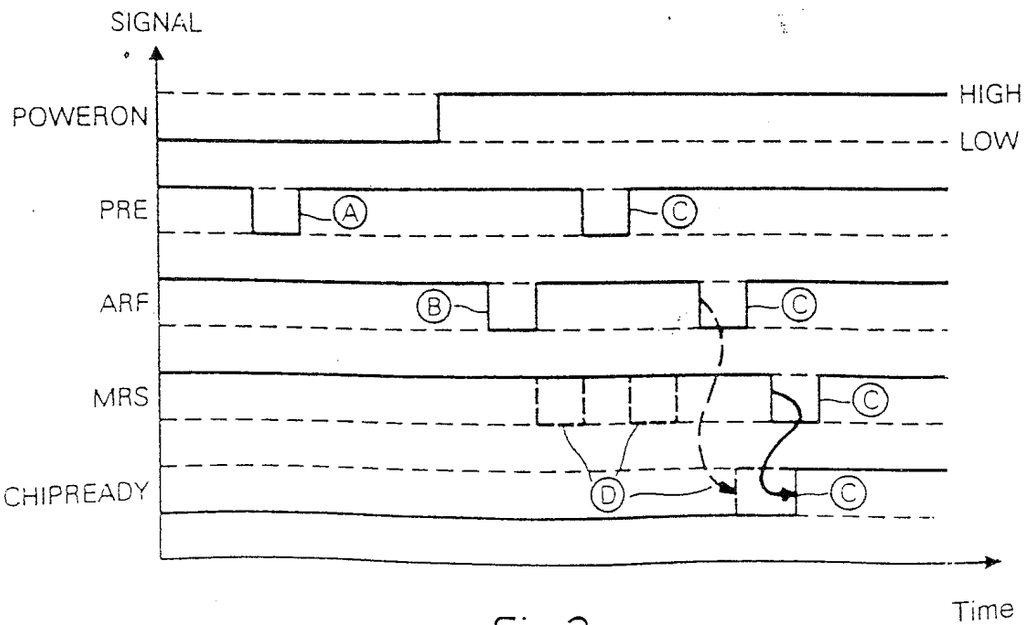


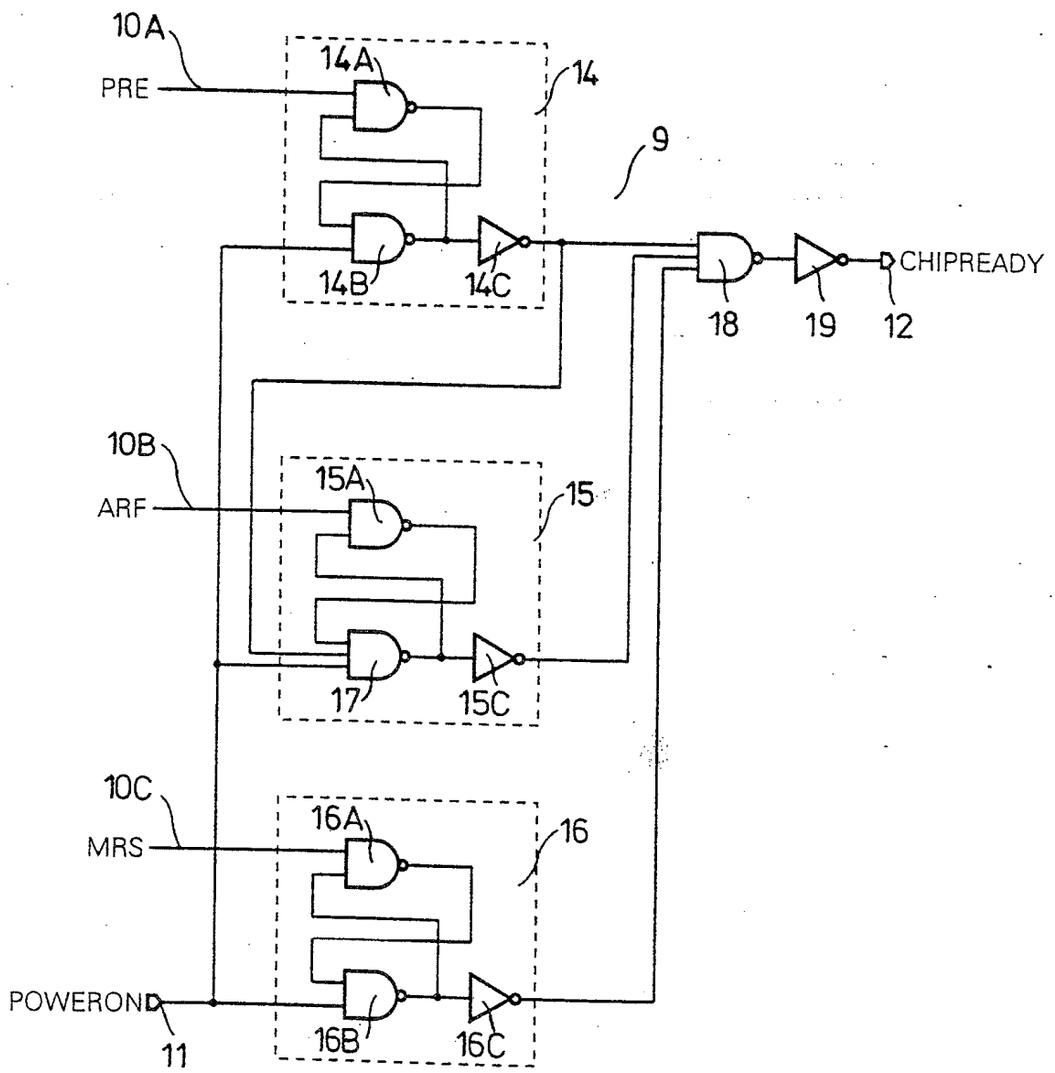
Fig 3

Docket # GR98P1989

Applic. #

Applicant: Glenna Mauss

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, Fl 33022-2480
Tel: (954) 925-1100 Fax: (954) 925-1101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16
POWERON
11
16B
16C

Fig 4

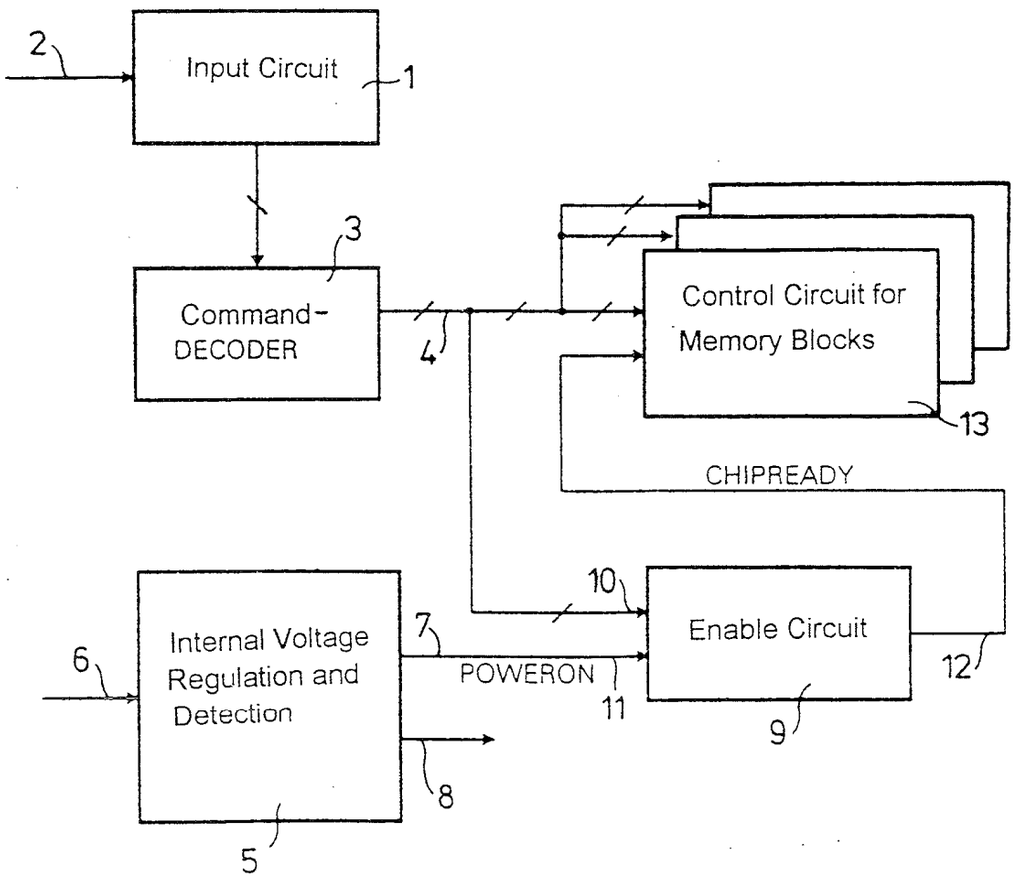
Docket # 6298P1989

Applic. #

Applicant: Gunnar Wause

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, Fl 33022-2480
Tel: (954) 925-1100 Fax: (954) 925-1101

Fig 1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DECODER
4
Control Circuit for
Memory Blocks
13
CHIPREADY
10
Enable Circuit
12
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6
Internal Voltage
Regulation and
Detection
7
POWERON
11
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5

Docket # 6298P1989

Applic. #

Applicant: GUNDA HAUSE

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, Fl 33022-2480
Tel: (954) 925-1100 Fax: (954) 925-1101

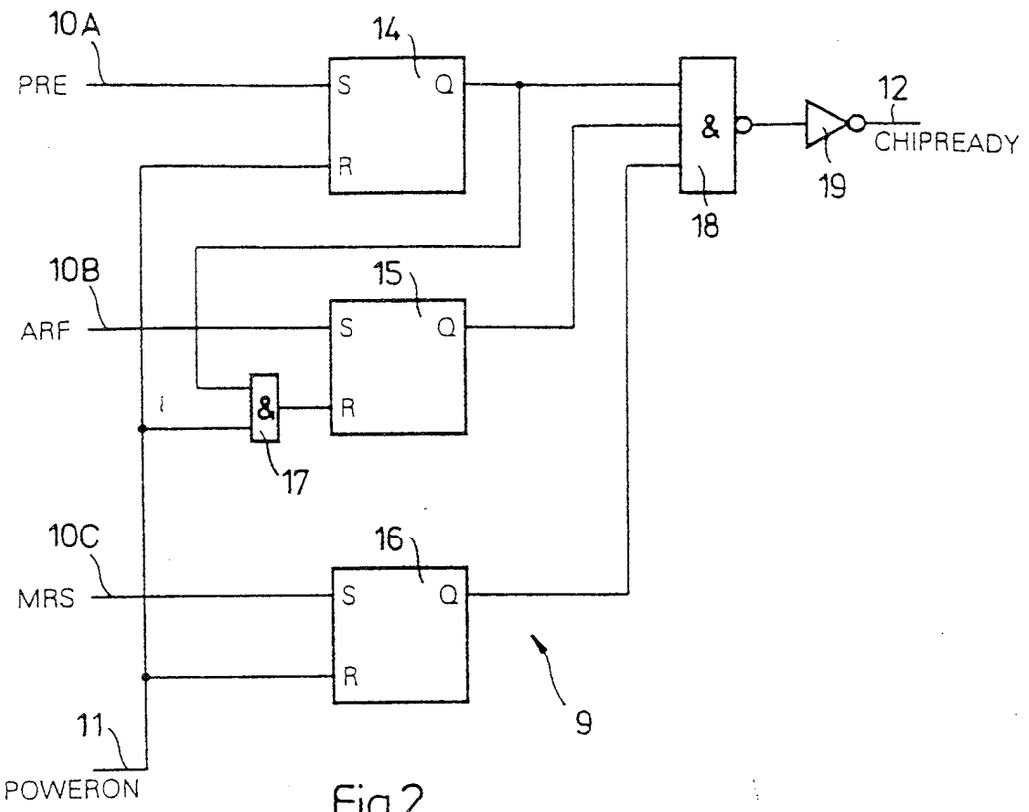
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Fig 2

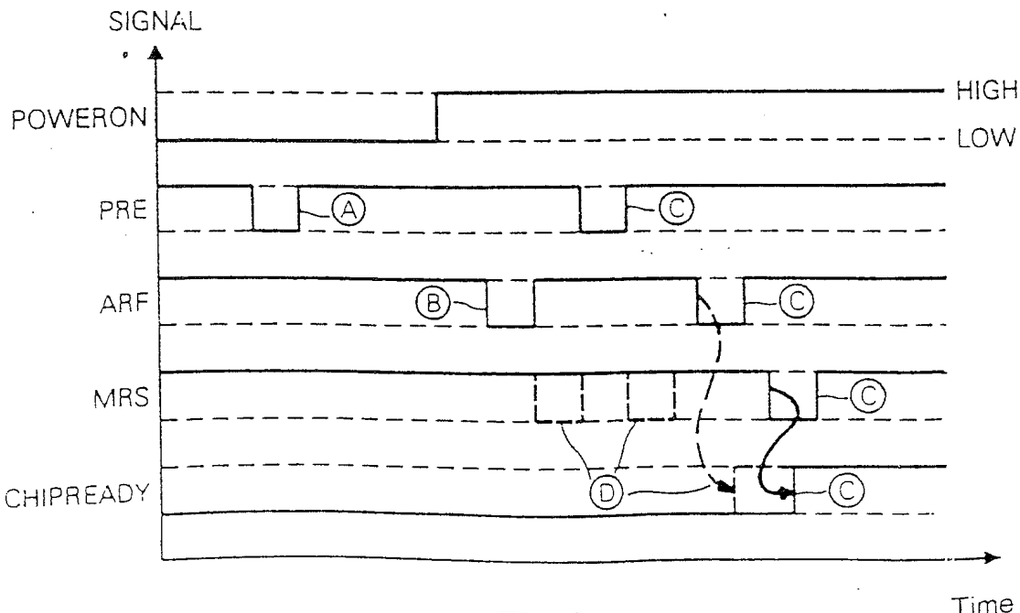
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Fig 3

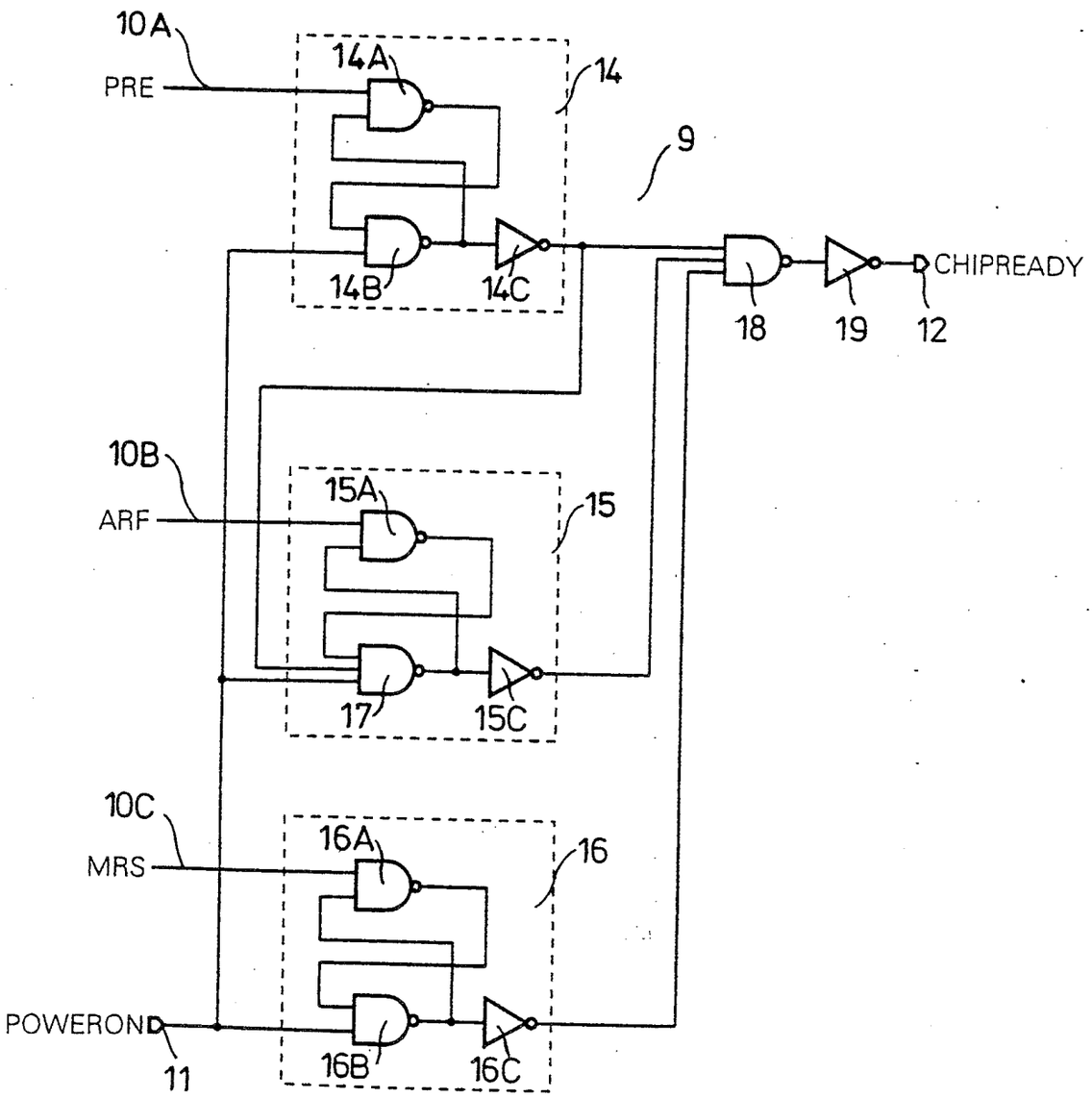
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Fig 4

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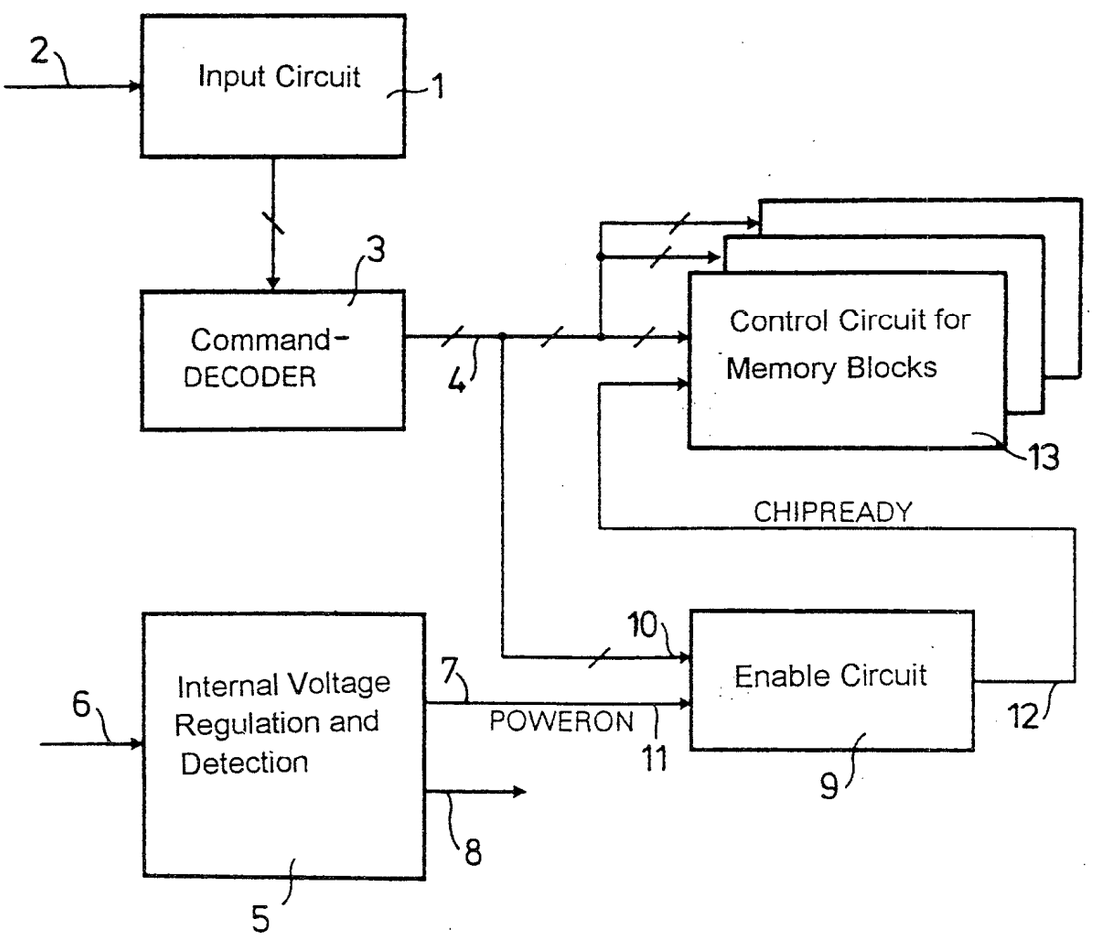
Fig 1



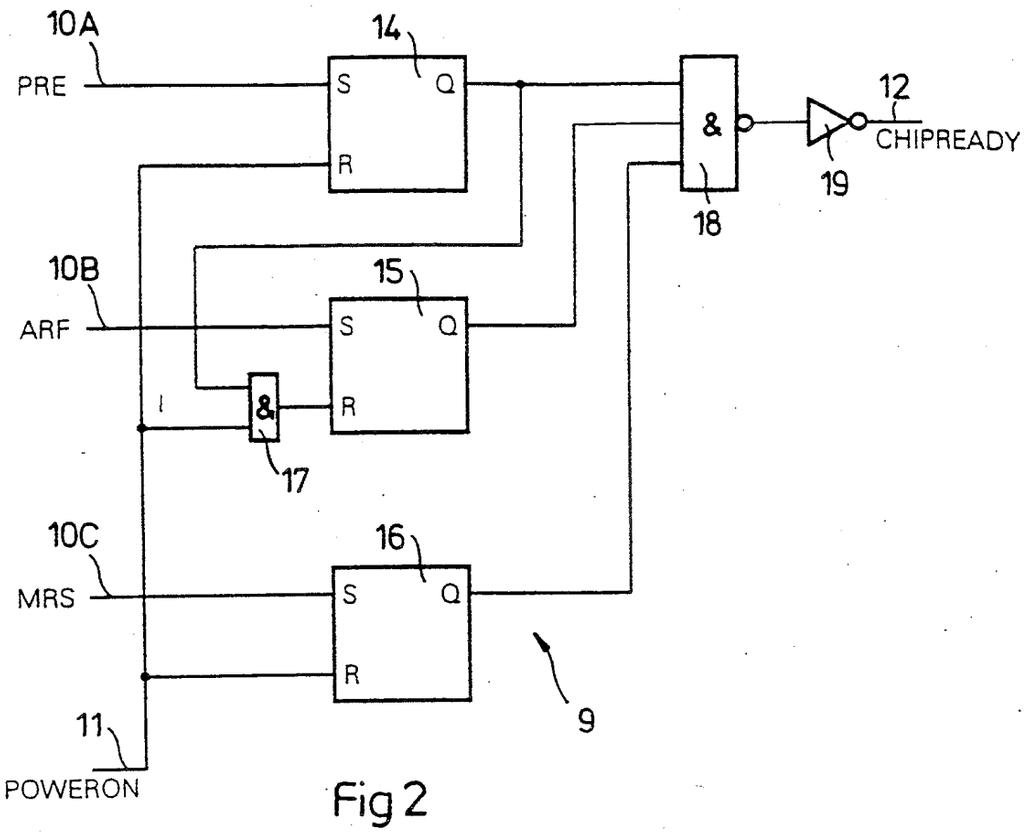

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Fig 2

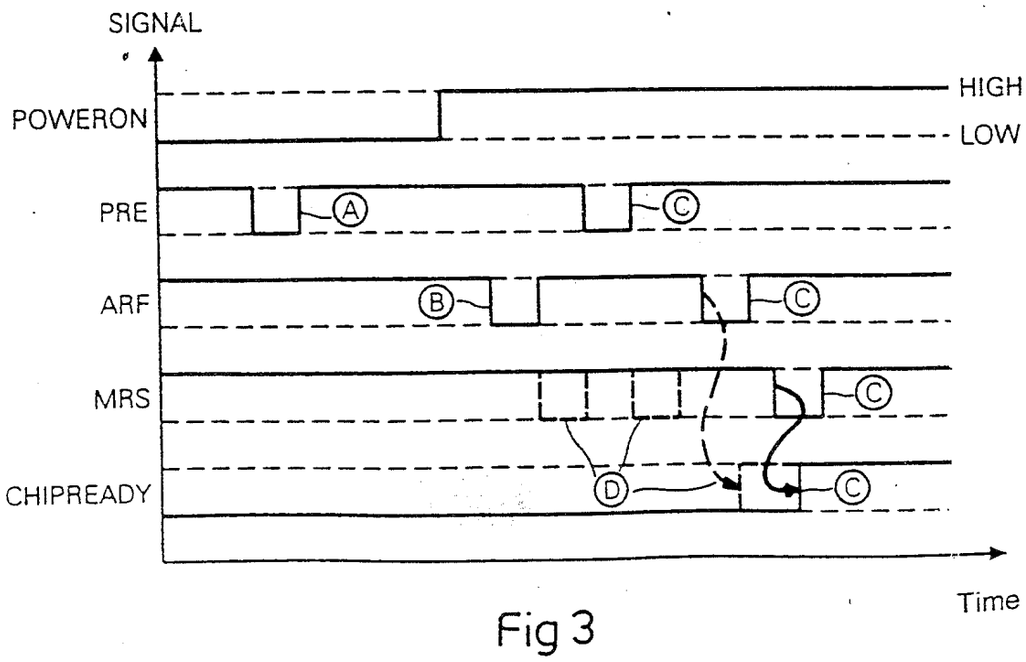
SIGNAL
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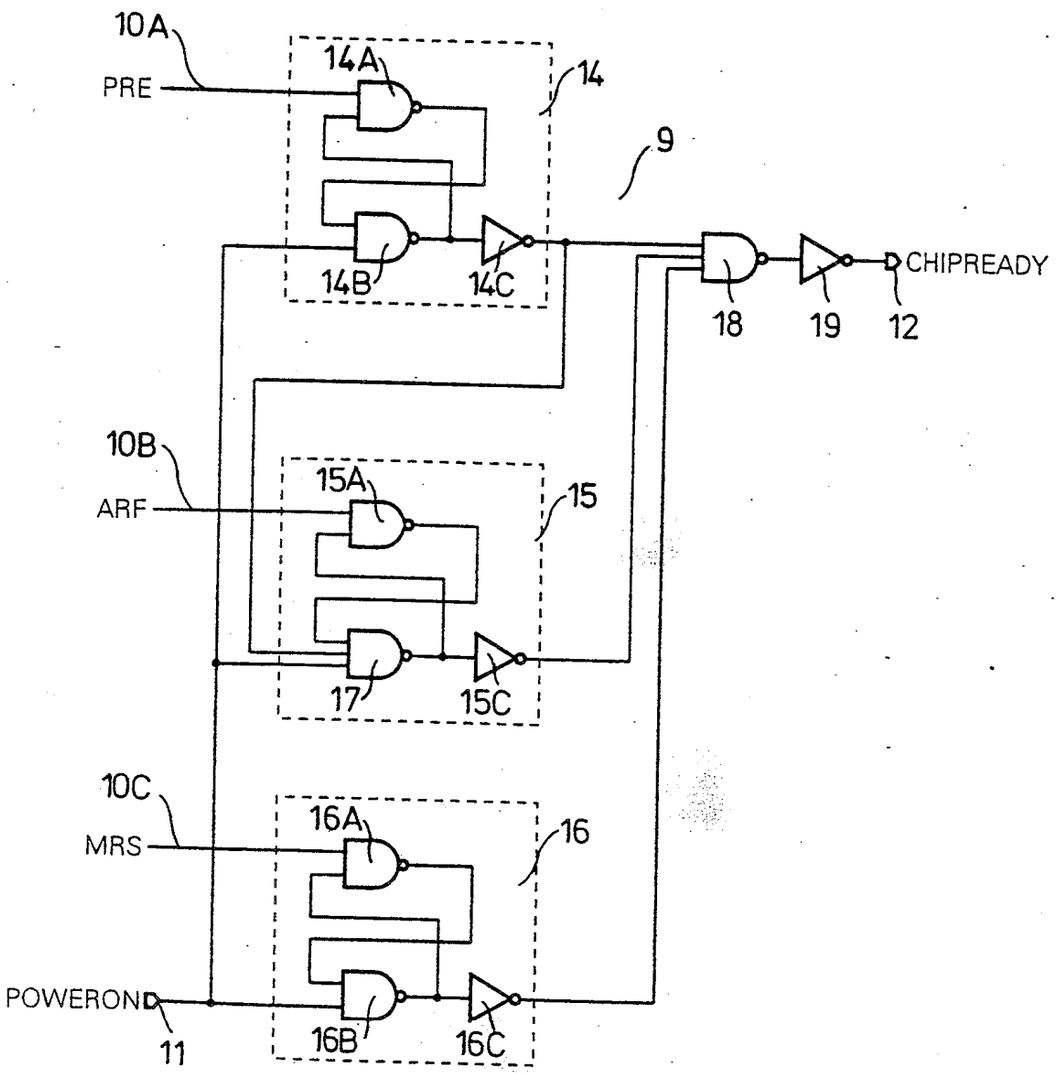
Fig 3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10C
MRS
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POWERON
11
16B
16C

Fig 4

Docket No.: GR 98 P 1989

COMBINED DECLARATION AND POWER OF ATTORNEY
IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

German Application No. 198 29 287.2, filed June 30, 1998, the International Priority of which is claimed under 35 U.S.C. §119.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

HERBERT L. LERNER (Reg.No.20,435)
LAURENCE A. GREENBERG (Reg.No.29,308)
WERNER H. STEMER (Reg.No.34,956)
RALPH E. LOCHER (Reg.No.41,947)

Address all correspondence and telephone calls to:

LERNER AND GREENBERG, P.A.
POST OFFICE BOX 2480
HOLLYWOOD, FLORIDA 33022-2480
TEL: (954) 925-1100
FAX: (954) 925-1101

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

PTO-103X
(Rev. 6-99)

FILING RECEIPT

CORRECTED

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTORNEY DOCKET NO.	DRWGS	TOT CL	IND CL
09/343,431	06/30/99	2818	$890.00	GR98P1989	3	13	2

LERNER AND GREENBERG PA
PO BOX 2480
HOLLYWOOD FL 33022-2480

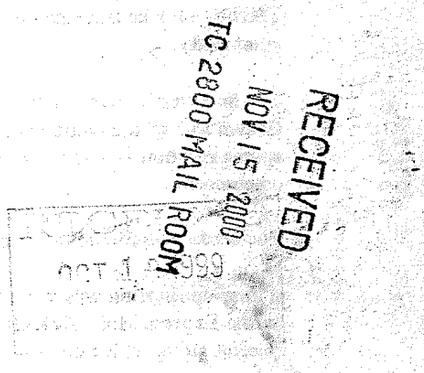
Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts of Application" ("Missing Parts Notice") in this application, please submit any corrections to this Filing Receipt with your reply to the "Missing Parts Notice." When the PTO processes the reply to the "Missing Parts Notice," the PTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s) GUNNAR KRAUSE, MUENCHEN, FED REP GERMANY.

FOREIGN APPLICATIONS- FED REP GERMANY 198 29 287.2 06/30/98

IF REQUIRED, FOREIGN FILING LICENSE GRANTED 07/26/99
TITLE
DYNA MIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INTIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

PRELIMINARY CLASS: 365



DATA ENTRY BY: HALLMAN, LINDA TEAM: 01 DATE: 10/06/99

(See reverse for new important information)

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NOT GRANTED

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The articles such as **"a," "an"** and **"the"** are not included as the first words in the title of an application. They are considered to be unnecessary to the understanding of the title.

The words **"new," "improved," "improvement," "improvements in or relating to"** are not included as the first words in the title of an application because a patent application is, by nature, a new idea or improvement.

The title may be truncated if it consists of more than 4 lines of 70 characters each (letters and spaces combined).

The inventor information may be truncated if the family name consists of more than 25 characters (letters and spaces combined) and if the given name consists of more than 25 characters (letters and spaces combined). The inventor's residence allows for up to 40 characters (letters and spaces combined).

The docket number allows a maximum of 12 characters.

If your application was submitted under 37 CFR 1.10, your filing date should be the "date in" found on the Express Mail label. If there is a discrepancy, you should submit a request for a corrected Filing Receipt along with a copy of the Express Mail label showing the "date in."

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Washington, DC 20231

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Docket No.: GR 98 P 1989

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

By: _____ Date: October 12, 1999

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Gunnar Krause
Appl. No.	:	09/343,431
Filed	:	June 30, 1999
Title	:	Dynamic Semiconductor Memory Device and Method For Initializing a Dynamic Semicondutor Memory Device
Art Unit	:	2818

LETTER

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

Undersigned counsel has received the Filing Receipt for the above-identified application.

However, the title has been listed incorrectly and should be listed as:

DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDCUTOR DEVICE

It is respectfully requested that the Patent Office Records be changed and that a new Filing Receipt be issued, so that the printed patent will show the correct title.

Respectfully submitted,

RALPH E.LOCHER
REG NO. 41,947

/av

Date: October 12, 1999

Lerner and Greenberg, P.A.
Post Office Box 2480
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Tel: (954) 925-1100
Fax: (954) 925-1101

US006157589A

United States Patent [19]

Krause

[11] Patent Number: 6,157,589

[45] Date of Patent: Dec. 5, 2000

[54] **DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE**

[75] Inventor: **Gunnar Krause**, Munich, Germany

[73] Assignee: **Siemens Aktiengesellschaft**, Munich, Germany

[21] Appl. No.: **09/343,431**

[22] Filed: **Jun. 30, 1999**

[30] **Foreign Application Priority Data**

Jun. 30, 1998 [DE] Germany 198 29 287

[51] **Int. Cl.**[7] **G11C 8/00**

[52] **U.S. Cl.** **365/226**; 365/228

[58] **Field of Search** 365/226, 227, 365/228

[56] **References Cited**

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Primary Examiner—Vu A. Le

Attorney, Agent, or Firm—Herbert L. Lerner; Laurence A. Greenber; Werner H. Stemer

[57] **ABSTRACT**

A dynamic semiconductor memory device of a random access type has an initialization circuit that controls the switching-on operation of the semiconductor memory device and of its circuit components. The initialization circuit supplies a supply voltage stable signal once the supply voltage has been stabilized after the switching-on of the semiconductor memory device. The initialization circuit has an enable circuit that receives the supply voltage stable signal and further command signals externally applied to the semiconductor memory device. The enable circuit supplies an enable signal after a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is identified. The enable signal effects the unlatching of a control circuit provided for the proper operation of the semiconductor memory device.

13 Claims, 3 Drawing Sheets

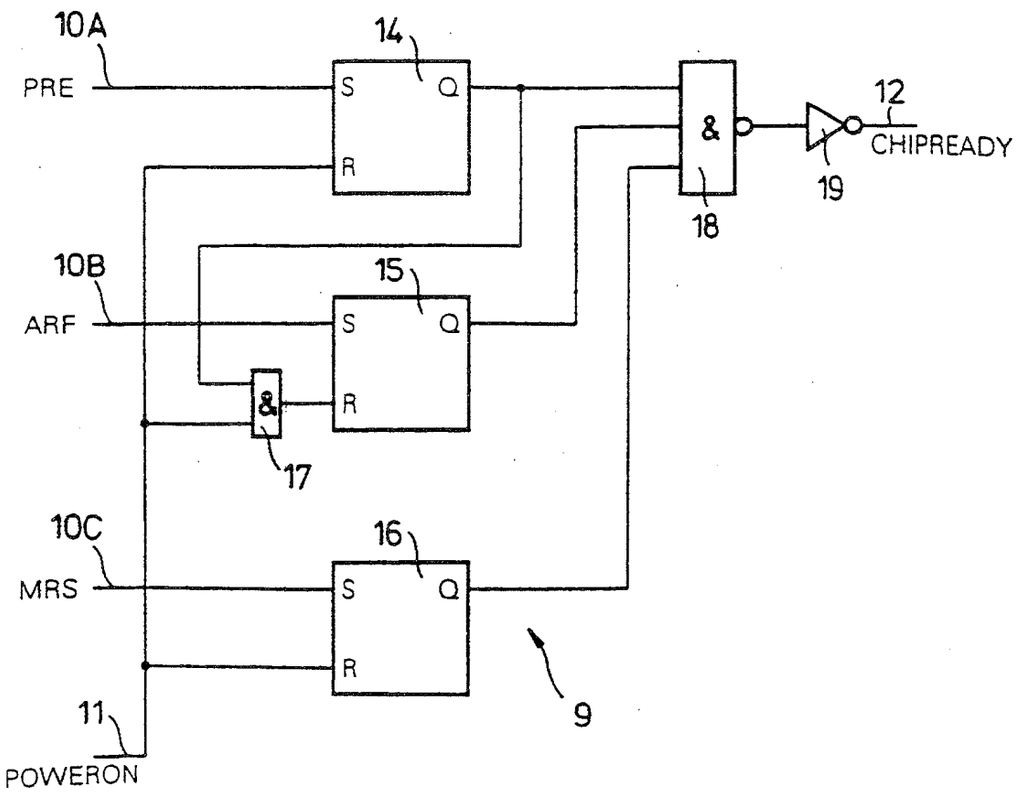
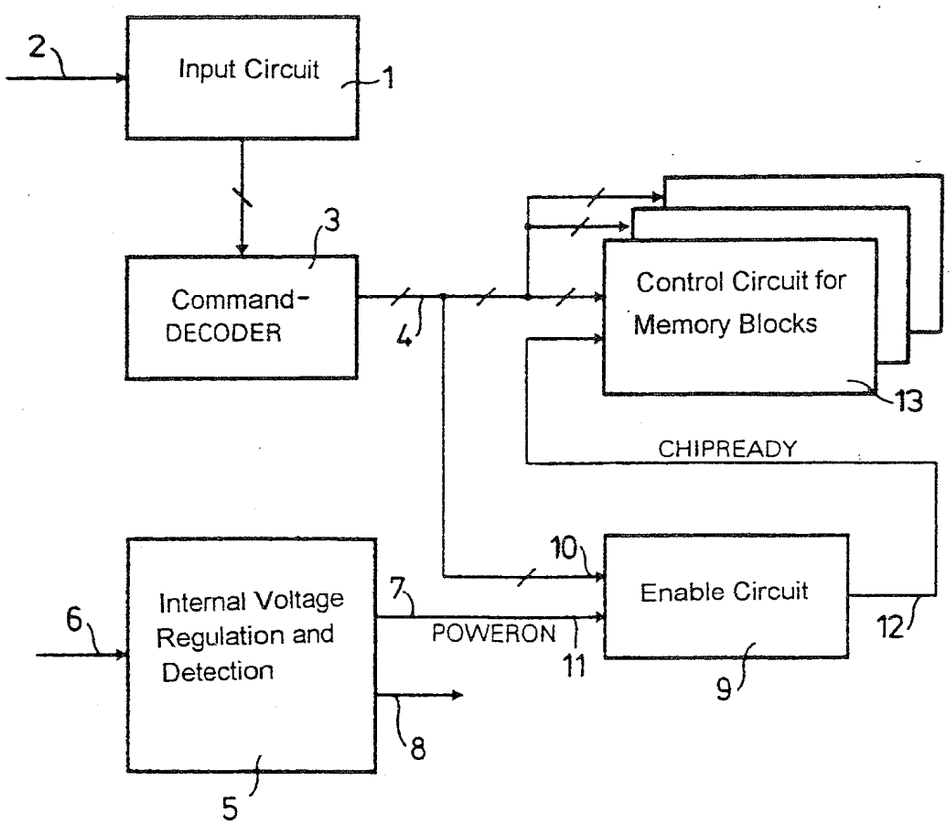
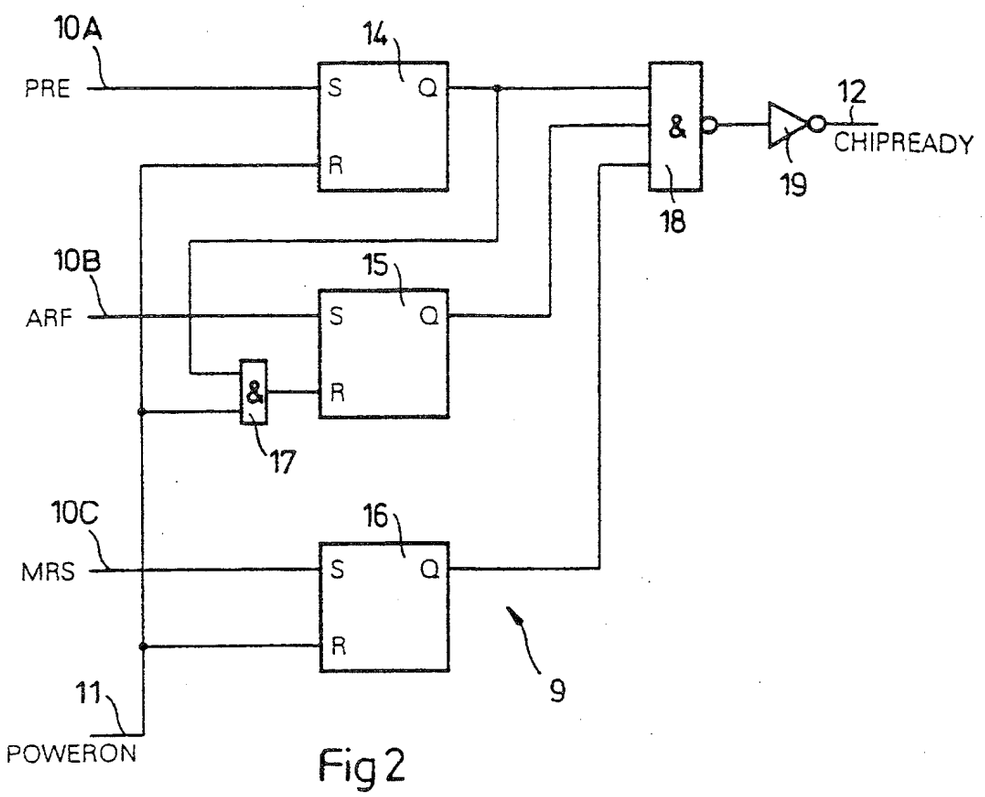


Fig 1


2
Input Circuit
1
3
Command-
DECODER
4
Control Circuit for
Memory Blocks
13
CHIPREADY
10
7
Internal Voltage
Regulation and
Detection
6
POWERON
11
Enable Circuit
12
9
8
5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14
S
Q
R
&
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CHIPREADY
19
18
10B
ARF
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Q
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MRS
16
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9
11
POWERON

Fig 2

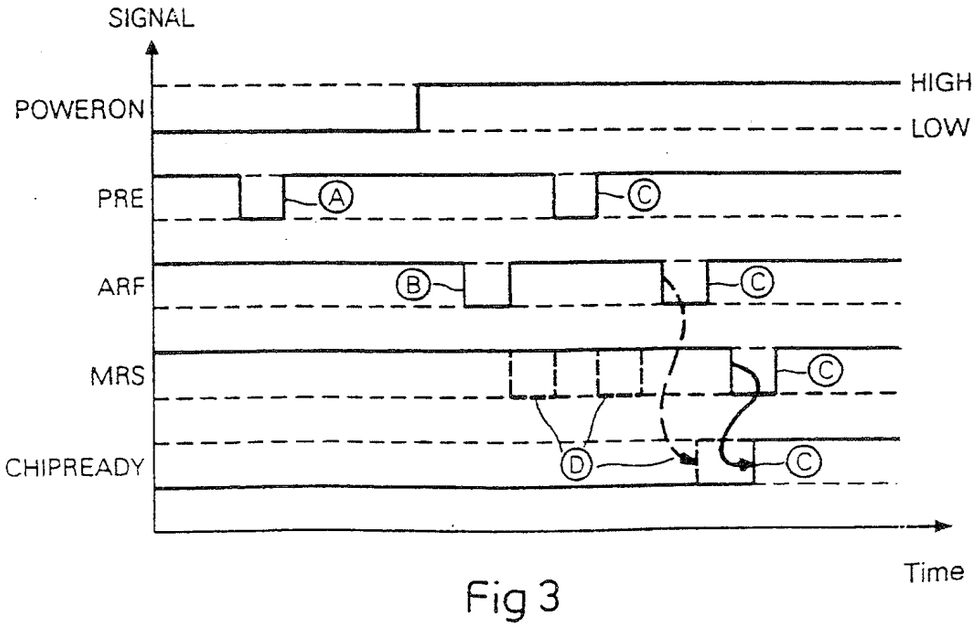
SIGNAL
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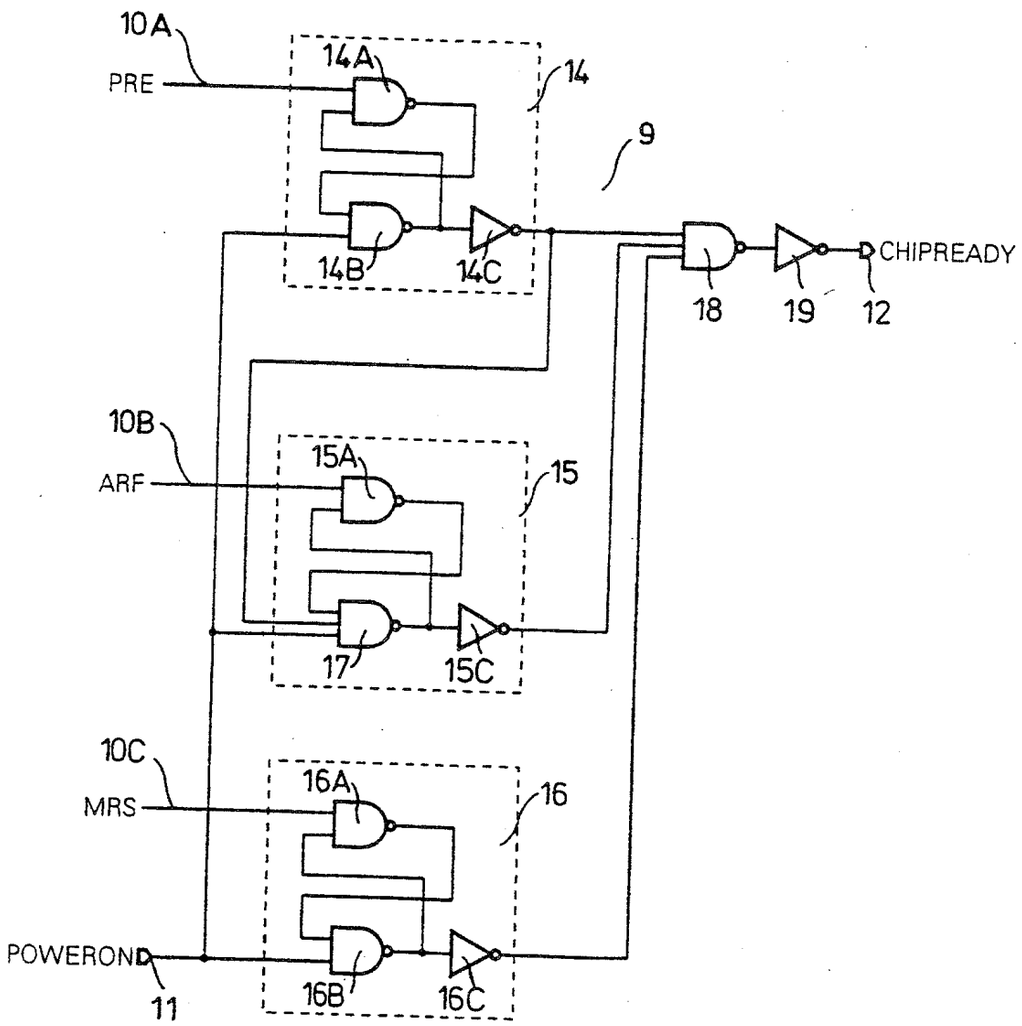
Fig 3


10A
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15C
10C
MRS
16A
16
POWERON
11
16B
16C

Fig 4

DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a dynamic semiconductor memory device of the random access type (DRAM/SDRAM) having an initialization circuit which controls a switching-on operation of the semiconductor memory device and of its circuit components. The initialization circuit supplies a supply voltage stable signal (POWERON) once a supply voltage has been stabilized after the switching-on of the semiconductor memory device. The invention also relates to a method for initializing such a dynamic semiconductor memory device, and also to the use of an enable circuit, that supplies an enable signal, for controlling the switching-on operation of the dynamic semiconductor memory device.

In the case of SDRAM semiconductor memories according to the JEDEC standard, it is necessary to ensure during the switch-on operation ("POWERUP") that the internal control circuits provided for the proper operation of the semiconductor memory device are reliably held in a defined desired state, in order to prevent undesirable activation of output transistors that would cause, on the data lines, a short circuit (so-called "bus contention" or "data contention") or uncontrolled activation of internal current loads. The solution to the problem turns out to be difficult on account of a fundamental unpredictability of the time characteristic of the supply voltage and of the voltage level or levels at the external control inputs during the switch-on operation of the semiconductor memory. According to the specifications of the manufacturer an SDRAM component should ignore all commands which are present chronologically before a defined initialization sequence. The sequence consists of predetermined commands that must be applied in a defined chronological order. However, a series of functions and commands which are allowed during proper operation of the component are desired or allowed chronologically only after the initialization sequence. According to the JEDEC standard for SDRAM semiconductor memories, a recommended initialization sequence (so-called "POWERON-SEQUENCE") is provided as follows:

a. the application of a supply voltage and a start pulse in order to maintain an NOP condition at the inputs of the component;

b. the maintenance of a stable supply voltage of a stable clock signal, and of stable NOP input conditions for a minimum time period of 200 us;

c. the preparation command for word line activation (PRECHARGE) for all the memory banks of the device;

4. the activation of eight or more refresh commands (AUTOREFRESH); and

5. the activation of a loading configuration register command (MODE-REGISTER-SET) for initializing the mode register.

After the identification of such a defined initialization sequence, the memory module is normally in a so-called IDLE state, that is to say it is precharged and prepared for proper operation. In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.

SUMMARY OF THE INVENTION

It is accordingly an object of the invention to provide a dynamic semiconductor memory device and a method for initializing a dynamic semiconductor memory device which overcome the above-mentioned disadvantages of the prior art methods and devices of this general type, which is as simple as possible in structural terms and which effectively prevents the risk of a short circuit of the data lines and/or of uncontrolled activation of internal current loads.

With the foregoing and other objects in view there is provided, in accordance with the invention, a dynamic semiconductor memory device of a random access type, containing an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. The initialization circuit has a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals. The enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals are identified and the enable signal effecting an unlatching of the control circuit.

The invention provides for the initialization circuit to have an enable circuit, which receives the supply voltage stable signal and the externally applied further command signals. The enable circuit generates the enable signal after the identification of the predetermined proper initialization sequence of the command signals is achieved. The enable signal effects the unlatching of the control circuit provided for the proper operation of the semiconductor memory device.

Following the principle of the invention, the enable signal (CHIPREADY) is generated and becomes active in dependence on further internal signals and the initialization sequence and then unlatches predetermined circuits. The predetermined circuits remain latched until the end of the predetermined initialization sequence. By way of example, commands are decoded but not executed and the output drivers are held at high impedance.

According to the preferred application in SDRAM memory devices according to the JEDEC standard, it is provided that the command signals, externally applied to the semiconductor memory device, of the initialization sequence are to be identified by the enable circuit. The command signals include a preparation command signal for word line activation (PRECHARGE), and/or a refresh command signal (AUTOREFRESH), and/or a loading configuration register command signal (MODE-REGISTER-SET).

According to an advantageous structural refinement of the initialization circuit according to the invention, it is provided that the enable circuit has at least one bistable multivibrator stage with a set input which receives the command signal (PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET). The bistable multivibrator also has a reset input to which the supply voltage stable signal (POWERON), a signal derived therefrom, or a linked signal is applied. The bistable multivibrator further has an output at which the enable signal (CHIPREADY) is outputted.

In particular, the enable circuit has a plurality of bistable multivibrator stages respectively receiving the command signals.

In an expedient refinement of the invention, it is provided that the output of at least one of the bistable multivibrator stages is passed to a reset input of a further multivibrator stage. In this case, it may furthermore be provided that, in one of the bistable multivibrator stages, the supply voltage stable signal (POWERON) and the signal output from the output of the further multivibrator stage are passed, after having been logically combined by a gate, to the reset input of the multivibrator stage.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a dynamic semiconductor memory device and a method for initializing a dynamic semiconductor memory device, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagrammatic, block diagram of components of an initialization circuit which controls a switching-on operation of a semiconductor memory and its circuit components according to the invention;

FIG. **2** is circuit diagram of an enable circuit that supplies an enable signal (CHIPREADY);

FIG. **3** is a time sequence diagram for elucidating a method of operation of the circuit according to FIG. **2**; and

FIG. **4** is a circuit diagram of the enable circuit according to an exemplary embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to FIG. **1** thereof, there are shown circuit components, important for understanding the invention, of an SDRAM memory device operating according to the JEDEC standard. The circuit components include an initialization circuit controlling a switching-on operation of the SDRAM memory device and its circuit components. The initialization circuit has an input circuit **1**, to whose input **2** command and clock signals that are externally applied in reference to the semiconductor memory are provided. The command and clock signals are amplified and conditioned before being received by a command decoder **3** connected downstream of the input circuit **1** and at whose output **4**, inter alia, the command signals PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command) and MRS or MODE-REGISTER-SET (loading configuration register command) are output. The initialization circuit further has a circuit **5** for internal voltage regulation and/or detection, at whose input **6** the external supply voltages that are externally applied to the semiconductor memory externally are fed in. The circuit **5** has a first output **7** outputting a POWERON signal and a second output **8** supplying stabilized internal supply voltages. The method of operation and the structure of the circuits **1**, **3** and **5** are sufficiently known to the person skilled in the art and therefore do not need to be explained in any more detail. What is important for understanding the invention is the fact that the circuit **5** supplies an active POWERON signal if, after the POWERUP phase of the SDRAM memory, the internal supply voltages present at the output **8** have reached the values necessary for proper operation of the component.

According to the invention, the initialization circuit furthermore has an enable circuit **9** connected downstream of the circuits **3** and **5**. The command signals PRE, ARF and MRS are applied to an input **10** of the enable circuit **9** and the POWERON signal is applied to an input **11** of the enable circuit **9**. An enable signal CHIPREADY is supplied at an output **12** of the enable circuit **9** after the identification of a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is achieved. The enable signal effects unlatching of control circuits **13** provided for proper operation of the semiconductor memory device. The internal control circuits **13** serve inter alia for sequence control for one or more of the memory blocks of the SDRAM memory and are known as such.

FIG. **2** shows a preferred exemplary embodiment of the enable circuit **9** according to the invention. The enable circuit **9** contains three bistable multivibrator stages **14**, **15** and **16** each having a set input S, a reset input R, and also an output Q. An AND gate **17** connected upstream of the reset input R of the multivibrator stage **15** and an AND gate **18** connected downstream of all the outputs Q of the multivibrator stages **14**, **15**, **16** are further provided. The enable circuit further has an inverter **19** connected downstream of the AND gate **18**. The enable signal CHIPREADY being output at the output **12** of the inverter **19** and the enable signal CHIPREADY is active HIGH, that is to say activated when its voltage level is at logic HIGH. The command signals PRE, ARF, MRS applied to the respective set inputs S of the bistable multivibrator stages **14**, **15**, **16** are each active LOW, that is to say these signals are active when their voltage level is at logic LOW, while the POWERON signal is again active HIGH. The POWERON signal is applied directly to the reset inputs R in the case of the multivibrator stages **14** and **16** and is firstly applied to one input of the AND gate **17** in the case of the multivibrator stage **15**, the signal output from the output Q of the multivibrator stage **14** is applied to the other input of the AND gate **17**, the output of the AND gate **17** is connected to the reset input of the multivibrator stage **15**.

The method of operation of the enable circuit **9** illustrated in FIG. **2** is such that activation of the enable signal CHIPREADY at is the output **12** to logic HIGH is generated only when a predetermined chronological initialization sequence of the command signals PRE, ARF and MRS and activation of the POWERON signal to the logic level HIGH are detected. Only then are the control circuits **13** unlatched on account of the activation of the enable signal CHIPREADY; the control circuits **13** remaining latched prior to this.

In the schematic time sequence diagram according to FIG. **3**, exemplary command sequences during the switching-on operation of the semiconductor memory device are illustrated in order to elucidate the method of operation of the enable circuit **9**. In the case situation A, the signal PRECHARGE is activated to active LOW too early relative to the activation of the POWERON signal, with the result that, the enable signal CHIPREADY is not yet activated to logic HIGH since the proper initialization sequence requires a

waiting time before the first command. The signal swing of the command PRECHARGE according to case situation A is thus correctly ignored. In case situation B, the chronological order of the activation of the signal AUTOREFRESH to logic LOW is incorrect since the proper initialization sequence prescribes a previous PRECHARGE command before the AUTOREFRESH command. The signal swing of the AUTOREFRESH signal to logic LOW according to case situation B is therefore likewise ignored, and the enable signal does not go to logic HIGH. In case situation C, a correct chronological order of the commands PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET is present conforming to the JEDEC standard, in a logically consistent manner, since the POWERON signal is also at logic HIGH, an enable signal CHIPREADY at logic HIGH is now supplied. Illustrated using dashed lines, another further conceivable initialization sequence that is allowed and therefore triggers an enable signal is represented by the symbol D; activation of the command MODE-REGISTER-SET to logic LOW is allowed at any time after the activation of the POWERON signal.

FIG. **4** shows further details of a preferred exemplary embodiment of the enable circuit **9** according to the invention. In this exemplary embodiment, each of the bistable multivibrators **14**, **15**, **16** is constructed from in each case two NAND gates **14**A, **14**B, **15**A, **17**, **16**A, **16**B and also an inverter **14**C, **15**C and **16**C, which are connected to one another in the manner illustrated. The NAND gate **17** is provided with three inputs in the bistable multivibrator **15**.

I claim:

1. A dynamic semiconductor memory device of a random access type, comprising:

an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation, said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals, said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

2. The semiconductor memory device according to claim **1**, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal.

3. The semiconductor memory device according to claim **1**, wherein said enable circuit has at least one bistable multivibrator stage having a set input receiving the externally applied further command signals, a reset input receiving one of the supply voltage stable signal, a signal derived from the supply voltage stable signal and a linked signal, and an output outputting said enable signal.

4. The semiconductor memory device according to claim **3**, wherein said at least one bistable multivibrator stage is a plurlity of bistable multivibrator stages respectively receiving one of the externally applied further command signals.

5. The semiconductor memory device according to claim **4**, wherein said output of one of said plurality of bistable multivibrator stages is passed to said reset input of another of said plurality of bistable multivibrator stages.

6. The semiconductor memory device according to claim **4**, including an AND gate receiving the supply voltage stable signal and a signal output from said output of one of said plurality of bistable multivibrator stages, said AND gate outputting an output signal received at said reset input of another of said plurality of bistable multivibrator stages.

7. The semiconductor memory device according to claim **4**, wherein said plurality of bistable multivibrator stages are each formed of an RS flip-flop constructed from one of at least two NOR and at least two NAND gates.

8. The semiconductor memory device according to claim **1**, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.

9. The semiconductor memory device according to claim **1**, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.

10. The semiconductor memory device according to claim **1**, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences:

a) firstly PRE, secondly ARF, thirdly MRS;

b) firstly PRE, secondly MRS, thirdly ARF; and

c) firstly MRS, secondly PRE, or thirdly ARF;

where,

PRE=the preparation command signal for word line activation,

ARF=the refresh command signal, and

MRS=the loading configuration register command signal.

11. An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components, the improvement which comprises:

supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device; and

supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

12. The method according to claim **11**, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals.

13. The method according to claim **11**, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit.

* * * * *

PATENT APPLICATION FEE DETERMINATION RECORD

Effective November 10, 1998

Application or Docket Number: 09/343,483

CLAIMS AS FILED - PART I

	(Column 1)		(Column 2)	SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED		NUMBER EXTRA	RATE	FEE		RATE	FEE
BASIC FEE					380.00	OR		760.00
TOTAL CLAIMS	13	minus 20=	*	X$ 9=		OR	X$18=	
INDEPENDENT CLAIMS	2	minus 3 =	*	X39=		OR	X78=	
MULTIPLE DEPENDENT CLAIM PRESENT				+130=		OR	+260=	
				TOTAL		OR	TOTAL	760

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
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AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
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FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
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AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

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* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	RM	7091	7/13
O.I.P.E. CLASSIFIER		149	7/16/99
FORMALITY REVIEW	LH	60105	7/26/99

INDEX OF CLAIMS

✔ ..... Rejected
= ..... Allowed
— (Through numeral)... Canceled
÷ ..... Restricted
N ..... Non-elected
I ..... Interference
A ..... Appeal
O ..... Objected

Claim Final	Claim Original	Date
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If more than 150 claims or 10 actions
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SEARCHED

Class	Sub.	Date	Exmr.
365	226 227 228	7/11/00	DK

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
365	226 228	7/12/00	DK

SEARCH NOTES
(INCLUDING SEARCH STRATEGY)

	Date	Exmr.

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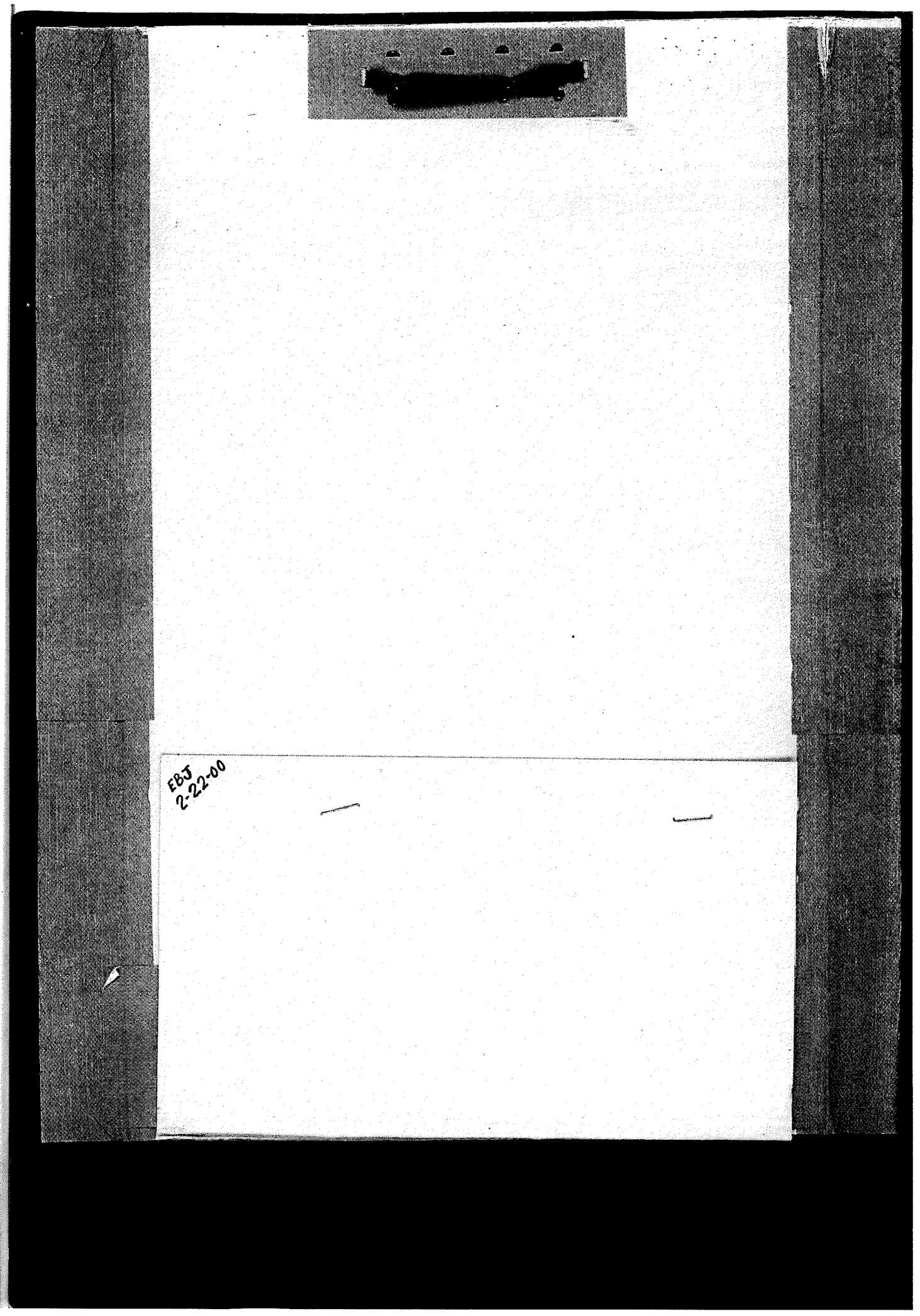
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PATENT APPLICATION

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INITIALS 7/3/99 LO

CONTENTS

		Date received (Incl. C. of M.) or Date Mailed
1.	Application 3 Pkts. papers.	
2.	Unsigned Dec	12-27-99
3.	Decl & Surchrg	9-30-99
4.	I.D.S. w/References	6-30-99
5.	Priority Paper	9-30-99
6.	Assignt P/A	9-30-99
7.	IDS	12-27-99
8.	PTOL-37	7-17-00
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