

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

XILINX, INC.,  
Petitioner

v.

POLARIS INNOVATIONS LIMITED,  
Patent Owner

---

Case No.: IPR2023-00516

Patent No.: 6,157,589

For: Dynamic Semiconductor Memory Device and Method for Initializing a  
Dynamic Semiconductor Memory Device

---

**DECLARATION OF TIMOTHY D. DORNEY, PH.D.**

**PURSUANT TO 37 C.F.R. § 1.68**

---

## TABLE OF CONTENTS

I.	INTRODUCTION .....	1
II.	PROFESSIONAL BACKGROUND.....	3
III.	MATERIALS REVIEWED AND RELIED UPON .....	7
IV.	LEGAL STANDARDS.....	8
	A. Anticipation.....	8
	B. Obviousness.....	8
	C. Claim Construction Standard .....	10
V.	THE '589 PATENT.....	11
	A. Overview of the '589 Patent Background.....	11
	B. The '589 Patent Invention.....	13
	1. The '589 Patent teaches “said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified”.....	13
	2. The '589 Patent teaches “the enable signal effecting an unlatching of said control circuit.”.....	15
	C. Prosecution History .....	18
VI.	KOCIS (EXHIBIT 1004).....	19
	A. Overview of Kocis' Background.....	19
	B. Kocis' Disclosure .....	20
	C. Limitations of the Kocis' Disclosure.....	23
VII.	LEE (EXHIBIT 1005) .....	24
	A. Overview of Lee's Background.....	24
	B. Lee's Disclosure .....	26
	C. Limitations of the Lee's Disclosure .....	29
VIII.	JESD 21-C (EXHIBIT 1006) .....	36
	A. Overview of JESD 21-C.....	36

B.	Limitations of the JESD 21-C Disclosure .....	38
IX.	IKETANI (EXHIBIT 1007) .....	40
A.	Overview of Iketani’s Background .....	40
B.	Iketani’s Disclosure .....	40
C.	Limitations of the Iketani’s Disclosure .....	43
X.	OPINIONS .....	43
A.	Standard for a POSITA .....	43
B.	Claim Construction For “Externally Applied Further Command Signals” .....	45
C.	Claims 1, 9, 11, and 13 are Not Invalid under Ground 1 .....	47
1.	Claim Element 1.2, “said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and <i>externally applied further         command signals</i> ” is not disclosed in Kocis .....	48
2.	Claim Element 1.3, “said enable circuit outputting an enable signal after <i>a predetermined proper initialization sequence of         the externally applied further command signals</i> being identified and <i>the enable signal effecting an unlatching of said control         circuit</i> ” is not disclosed in Kocis .....	49
3.	Claim 9, “said control circuit has <i>output drivers remaining         latched</i> during the switching-on operation until said enable signal is generated by said enable circuit” is not disclosed in Kocis .....	53
4.	Claim Element 11.2, “supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and <i>further command         signals externally applied</i> to the dynamic semiconductor memory device, after an identification of <i>a predetermined         proper initialization sequence of the further command signals</i> the enable signal being generated and <i>effecting an unlatching of         a control circuit</i> provided for a proper operation of the dynamic semiconductor memory device” is not disclosed in Kocis .....	56

5.	Claim 13, “ <i>maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit</i> ” is not disclosed in Kocis .....	57
D.	Claims 2, 8, 10, and 12 are Not Invalid under Ground 2 .....	58
1.	Claim 2, “ <i>externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal</i> ” is not disclosed in Kocis in view of JESD 21-C.....	60
2.	Claim 8, “ <i>the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard</i> ” is not disclosed in Kocis in view of JESD 21-C .....	62
3.	Claim 10, “ <i>the predetermined proper initialization sequence includes one of the following chronologically successive command sequences: a) firstly PRE, secondly ARF, thirdly MRS; b) firstly PRE, secondly MRS, thirdly ARF; and c) firstly MRS, secondly PRE, or thirdly ARF; where, PRE=the preparation command signal for word line activation, ARF=the refresh command signal, and MRS=the loading configuration register command signal</i> ” is not disclosed in Kocis in view of JESD 21-C.....	63
4.	Claim 12, “ <i>providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals</i> ” is not disclosed in Kocis in view of JESD 21-C.....	64
E.	Claims 1 and 11 are Not Invalid under Ground 3A/3B .....	64
1.	Claim Element 1.2, “ <i>said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals</i> ” is not disclosed in Lee.....	65

2. Claim Element 1.3, “said enable circuit outputting an enable signal after a *predetermined proper initialization sequence of the externally applied further command signals* being identified and *the enable signal effecting an unlatching of said control circuit*” is not disclosed in Lee.....68
  3. Claim Element 11.2, “supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and *further command signals externally applied* to the dynamic semiconductor memory device, after an identification of a *predetermined proper initialization sequence of the further command signals* the enable signal being generated and *effecting an unlatching of a control circuit* provided for a proper operation of the dynamic semiconductor memory device” is not disclosed in Lee .....72
- F. Claims 1 and 11 are Not Invalid under Ground 4 .....73
1. Claim Element 1.2, “said initialization circuit having a control circuit for controlling operations and an enable circuit *receiving* the supply voltage stable signal and *externally applied further command signals*” is not disclosed in Lee in view of Iketani ..73
  2. Claim Element 1.3, “said enable circuit outputting an enable signal after a *predetermined proper initialization sequence of the externally applied further command signals* being identified and *the enable signal effecting an unlatching of said control circuit*” is not disclosed in Lee in view of Iketani .....74
  3. Claim Element 11.2, “supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and *further command signals externally applied* to the dynamic semiconductor memory device, after an identification of a *predetermined proper initialization sequence of the further command signals* the enable signal being generated and *effecting an unlatching of a control circuit* provided for a proper operation of the dynamic semiconductor memory device” is not disclosed in Lee in view of Iketani .....76
- G. Claims 2, 8, 10, and 12 are Not Invalid under Ground 5 .....77

# Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

## Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

## Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

## Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

## API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

## LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

## FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

## E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.