LATCH-UP IN CMOS INTEGRATED CIRCUITS*

B. L. Gregory and B. D. Shafer
Sandia Laboratories
Albuquerque, New Mexico 87115

Abstract

The parasitic transistors and pnpn paths present on junction-isolated CMOS circuits have been identified and studied quantitatively. Active SCR structures exist which can be triggered electrically or by a radiation pulse. Detailed studies of SCR paths have been performed on two circuits, the CD4007A and the CD4041A, to relate geometrical and materials parameters to latch-up sensitivity. Both normal bias conditions and bias optimum for obtaining SCR action are employed. Several techniques are proposed to eliminate radiation-induced latch-up in future CMOS designs.

Introduction

Latch-up[1] through the parasitic pnpn structures in bipolar integrated circuits has been responsible, in part, for the development of dielectric isolation as an important hardening technology. Since pnpn paths are again present in Complementary MOS integrated circuits,[2] it is important to explore latch-up effects in this technology to determine if dielectric isolation is required. In the present studies, latch-up is considered to be the creation of a low resistance path between power supply and ground on a circuit, during a radiation or electrical pulse, which remains low resistance after the pulse. The studies in Reference 1 explored the possibility of achieving circuit latch-up due to transistor sustaining voltage breakdown or due to second breakdown. The conclusion was that only the pnpn mechanism was important in most bipolar IC's. This is certainly true in CMOS circuits.

The present study will identify the pnpn paths present on CMOS circuits and demonstrate that active SCR's can result. Detailed studies on two particular circuits (RCA CD4007A and CD4041A) relate both geometry and material parameters to latch-up sensitivity. In both circuits the parasitic npn and pnp transistors have been separately characterized and a variety of pnpn paths have been explored. The activity of pnpn paths is determined by attempting to induce latch-up electrically. The studies employ bias conditions of two types. First, bias conditions are used which are optimum for obtaining SCR action through each pnpn path. Second, bias which duplicates actual circuit operation is employed to provide a direct measurement of the latch-up susceptibility. The former studies provide a worst-case situation for latch-up. If it is not observed in these studies, it will not be present for normal bias conditions.

Subsequent to the electrical studies, transient radiation experiments have been performed to verify the electrically-detected latch-up paths and to determine the radiation dose rate at which latch-up occurs.

Description of Latch-up Paths

In CMOS circuits the n-channel transistors are formed in p-wells diffused into the n-type substrate, while the p-channel transistors are formed directly on the substrate material. The structure is complicated by the presence of protection diodes from each input gate to the substrate (p^+n diode) and to the p-well (n^+p diode). The structure of a typical CMOS circuit is shown schematically in cross section in Figure 1.† Figures 2 and 3 show the layout and schematics for the two CMOS circuits studied most exhaustively in this work (4007 and 4041).

It is straightforward to identify several parasitic npn and pnp transistors on the 4007 and 4041 by examining the structure in Figure 1. First, the three-layer structure formed by the source, drain, or n^+p protection diode of the n-channel transistor (n^+), the p-well (p), and the substrate (n), consitutes a double-diffused npn device with an n^+ emitter. Similarly, the three-layer structure formed by either of the p^+ diffusions (p^+), the substrate (n), and the p-well (p), constitutes a pnp transistor. The pnp transistor is a wide-base lateral structure with relatively low gain. The two complementary pairs on the 4007 can be investigated as separate transistors, or as inverters if the p and n transistor drains are tied together. For transistor operation, there is a pnpn path from each input (gate) to the source or drain of the n-channel device. Similarly, between the source or drain of the p-channel and the source or drain of the n-channel (or gate), there is another pnpn structure.

For these pnpn paths to be active SCR structures which can latch-up during a transient radiation environment, several conditions must be met. First, the npn and pnp transistor gains must be such that $h_{fe}(npn) * h_{fe}(pnp) \geq 1$. Secondly, the bias conditions applied must allow the two end junctions of the pnpn structure to become forward biased. Finally, the V_{DD} and input bias circuits must be capable of supplying current equal to the holding current of the SCR. In an actual inverter, the p and n channel source diodes are shorted to the substrate and p-well, respectively, and do not become forward biased in normal operation. However, lateral voltage drops can exist during exposure to a transient radiation pulse, due primarily to p-well photocurrent, which can cause forward bias to appear over portions of the source contacts, even though they are elsewhere shorted to substrate or p-well. In Figure 4 we show the equivalent circuits of SCR's present on a CMOS circuit (4007) for the worst-case (A) and normal (B) bias conditions. The same essential pnpn structures are active in both bias situations; however, for the normal bias case, the forward bias on the two emitter junctions (gates) must be provided by lateral voltage drops due to the p-well photocurrent (or SCR current after turn-on) flowing laterally through the substrate and p-well resistances, R_s and R_p. For this reason, the active SCR in case B will be less sensitive to radiation than in case A and will be characterized by a larger holding current. Measurements made using the circuit elements wired as in case A maximize the likelihood of producing SCR action. If case A does not exhibit SCR behavior, case B most certainly will not.

Electrical Measurements

Parasitic Transistors

The circuit topologies of the 4007 and 4041 permit direct measurement of the parasitic npn and pnp transistor current gain. Hence, it is possible to calculate

*This work was supported by the U. S. Atomic Energy Commission.

†The p+ and n+ channel-stop regions have not been shown since they do not enter in the latch-up paths to be discussed.

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

the activity of various potential SCR paths by measuring the current gain product for the path (i.e., SCR action can occur if $h_{fe}(npn) * h_{fe}(pnp) \geq 1$). Current gains ($h_{fe}$) for a variety of parasitic npn and pnp paths are given in Table I for both the 4007 and 4041. The gain values given correspond approximately to the peak ac gain for the indicated path. The gain values for the characteristic connections identified in the table are averaged over the different connections which yield similar device structures.

Basic SCR Structures

Although our basic interest is in radiation-induced latch-up, the presence of SCR's on CMOS circuits can be observed more easily by simple electrical measurement. In the present work, the various possible SCR paths were studied using a Tektronix curve-tracer, with the base drive output providing gate current to trigger the SCR. Both self-triggering (no-gate current) and gate triggering (at fixed anode-cathode voltages) have been studied. The two paths identified in Table II have been explored on the 4007 circuit. The self-triggering characteristics of both connections for the 4007 are shown in Figure 5. Typically, the holding current of Connection 2 (1.0 ma) is much greater than Connection 1 (300 µA) due to the lower gain (wider base) of the parasitic pnp for Connection 2.

Both Connection 1 and Connection 2 SCR's on the 4007 could be triggered on by a small gate current. Approximately 5 µA and 50 µA were required at Gate 1, respectively, for these two connections (10V bias).

The on-circuit wiring of the 4041 inverters prevented observation of the intrinsic SCR's formed by the pnp and npn transistor. However, the following section discusses SCR action which can occur in this unit due to lateral voltage drops caused by photocurrent during a radiation transient.

SCR Action-Normal Bias Conditions

As discussed above, latch-up can be observed for normal inverter bias conditions if the lateral voltage drops across R_p and R_s (Figure 4) produced by the p-well photocurrent are sufficient to forward bias the SCR gate junctions during a radiation transient. This behavior can be simulated electrically by overvoltaging the potential SCR into breakdown to trigger SCR action. Figure 6 shows the SCR behavior exhibited by one inverter on a 4007 circuit for two input conditions: (a) input high and (b) input low. For case (a) (pins 14,6-V_{DD}, pin 7-V_{SS}) the substrate current flows through R_s and produces a lateral voltage drop which forward biases the p^+n gate protection diode at pin 6. The current flowing laterally through the p-well produces forward bias along a section of the n^+ source junction which allows the SCR to turn on. Since the measured substrate resistance between p-well and the V_{DD} terminal (on the 4007) is approximately 30-50 ohms, the holding current of 45 ma in Figure 6a is to be expected ($I \times R_s$ = 45 ma x 30 ohms = 1.35 volts). When the input is low, as in 6b, the gate protection diode cannot become forward biased, hence, sufficient lateral voltage drop must exist under the p-channel source fingers to create a forward biased region. This can occur in the 4007 since the source fingers are parallel to the direction of current flow between V_{DD} and p-well. The holding current for this case is approximately 70 ma since a sufficient lateral voltage drop must be developed under the source finger of the 4007, a relatively short distance, in order to forward bias these junctions.

The only SCR exhibited by the 4041 when biased normally is that which occurs when the p^+ gate protection diode becomes forward biased due to a lateral voltage drop across the chip. This occurs only when the input is high, as shown in Figure 7a. The holding current for this case is approximately 60 ma. If an external resistance (1k) is inserted in the V_{DD} line, but the input is supplied by a low impedance source (7b), the SCR holding current is reduced to 28 ma. No SCR action can be produced in the 4041 when the input is low, indicating that it is impossible to forward bias any portion of the p-transistor source diode due to lateral voltage drops. As will be shown in the next section, this is due to the layout of the p-transistor.

Radiation Studies

Transient radiation studies have been performed on the above IC's at the Febetron 705 and Hermes II facilities at Sandia and at the Gulf Radiation Technology Linac. All the latch-up modes discussed above have been confirmed as being triggerable by a radiation pulse. For example, the SCR corresponding to Connection 1 on normal CD4007A circuits is triggered into latch-up at a dose rate of 1×10^8 rads/s (3 rads), from the Febetron 705, when biased at 10 volts. Latch-up on the circuits biased normally did not occur until higher dose rates, 3×10^8 rads/s (10^3 rads - Linac) for the 4007 and 3×10^9 rads/s (90 rads - Febetron) for the 4041. However, all latch-up modes observed electrically could be stimulated by exposure to a dose of 2×10^{11} rads/s (10^4 rads) from the Hermes II. A series of Febetron 705 transient studies was performed on the CD4007A, using special circuits whose peak gain products (Connection 1) were less than unity (0.07, 0.14, 0.15, 0.18) and slightly greater than unity (1.3). No latch-up was observed for gain products less than unity. The device whose gain product exceeded unity (1.3) did latch-up (holding current = 34 ma), in agreement with electrically-induced latch-up measurements on the same unit.

Studies have been performed on a variety of other circuits (CD4009A, CD4010A, CD4020A, CD4011A-RCA) of varying complexity. Latch-up has been observed in the 4007, 4009, 4010, 4011, and 4041. In the 4020, a typical MSI complexity circuit, no latch-up is observed at 10^{12} rads/s. This is undoubtedly related to the much smaller p-well areas for the individual inverters in the 4020, which results in reduced photocurrents and lateral voltage drops.

Latch-up Prevention in CMOS

Although the above studies demonstrate that latch-up is prevalent in CMOS circuits, there are several techniques which can be employed to eliminate it. These techniques can be grouped in three categories: (1) variation in material parameters, (2) variation in circuit layout, and (3) variation in CMOS processing. These are discussed below.

Variations in Material Parameters

Lifetime. As shown above, SCR action occurs when the product of npn and pnp common emitter current gains exceeds unity. If this criteria is not met in the circuit, the effects of any radiation pulse will die away soon after the pulse. Latch-up can thus be eliminated if the minority carrier lifetime in the CMOS circuit is reduced to the point where all possible gain (h_{fe}) products are less than unity. Figure 8 shows the SCR activity of the Connection 1 SCR on the 4007 circuit for three values of substrate lifetime, 1×10^{-6}s, 2×10^{-7}s, and 1×10^{-7}s. At the intermediate lifetime latch-up can be induced, but it is characterized by a large holding current (> 10 ma). No latch-up is present at the lowest lifetime, even for very high injected gate current. This sequence illustrates that latch-up via this most susceptible path in the 4007 can be

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

eliminated by reducing the substrate lifetime to 1 x 10^{-7}s, or lower. Transient radiation studies on the reduced lifetime circuits confirmed the absence of latch-up in these units, even at dose levels near 10^{12} rads/s. Since CMOS characteristics are not strongly influenced by minority carrier lifetime, the transfer characteristics of the circuit are essentially identical for all three cases in Figure 3. These results demonstrate that latch-up can be eliminated in CMOS circuits by control of lifetime.

Variations in Circuit Layout

Several guidelines can be formulated for CMOS layout which will greatly reduce the sensitivity of CMOS circuits to latch-up, possibly eliminating it all together. These guidelines are:

1. Employ minimum area p-wells. This minimizes the p-well photocurrent during a transient radiation pulse.

2. Position the V_{DD} terminal for the circuit physically close to the input-protection-arrays and any large p-wells present, or, provide a low resistance substrate path between these regions.

3. Place the source fingers of the p-transistors such that they lie along equipotential lines when current flows between V_{DD} and the p-wells (e.g., photocurrent). This means that the source fingers should be perpendicular to the dominant direction of current flow, rather than parallel. This effect is observed in the comparison of latch-up through the p-transistor source for the 4007 and 4041. The source fingers of the 4007 are parallel to the direction of photocurrent flow; hence, a significant lateral drop can occur under a source finger causing it to become forward biased. The source fingers of the 4041 are perpendicular to the current flow and no latch-up through the p-transistor source diodes can be observed.

4. Short the p-transistor source finger to the substrate with metallization along its entire length. Short the n-transistor source to the p-well with metallization along its entire length. This effectively prevents either of these diodes from ever becoming forward biased, hence eliminates their participation in latch-up.

5. Operate CMOS gates from relatively high impedance or low capacity supplies. This reduces the gate current which can flow and can prevent latch-up through the protection array.

Variations in CMOS Processing

If major changes in the standard, junction-isolated CMOS processing are allowable, several changes can be made which could individually eliminate the problem of latch-up. These processing changes are indicated below:

1. Use epitaxial silicon with an n^+ buried layer for the CMOS starting material. This greatly reduces the lateral voltage drops when photocurrent flows and also reduces the gain of the parasitic pnp transistors. To implement this change, relatively shallow p-wells are required.

2. Perform an n^+ deep isolation diffusion around the p-wells to connect with the n^+ buried layer. This reduces the parasitic pnp gains to virtually zero and eliminates all active four-layer paths.

3. Use isoplanar, polyplanar, or some other oxide isolation technique, around the p-wells in particular, to eliminate parasitic transistor action.

4. Fabricate the structures on SOS or dielectrically isolated substrates to eliminate parasitic transistor structures.

Latch-up would probably be eliminated by step number 1 and would most certainly be eliminated by steps 2-4.

Conclusions

Latch-up has been produced in a variety of CMOS circuits both by electrical and radiation triggering. The most susceptible pnpn path has been identified and explored, on several circuits, to provide a worst-case measure of the sensitivity of each circuit. Latch-up has also been studied for normal inverter bias conditions. In this case the p-well photocurrent produced by a radiation transient can create lateral voltage drops in the substrate and p-well which forward biases regions of the p- and n-transistor source diodes to create an active SCR. Several suggestions have been made regarding variations in material parameters, variations in circuit layout, and finally, variations in CMOS processing which can eliminate the latch-up mechanism as a serious radiation threat to CMOS integrated circuits.

References

1. J. F. Leavy and R. A. Poll, "Radiation-Induced Integrated Circuit Latch-up," IEEE Trans. Nuc. Sci., NS-16, p. 96, December 1969.

2. W. J. Dennehy, A. G. Holmes-Siedle, and W. F. Leopold, "Transient Radiation Response of Complementary-Symmetry MOS Integrated Circuits," IEEE Trans. Nuc. Sci., NS-16, p. 114, December 1969.

Table I

Typical Common Emitter Current Gains for the Parasitic npn and pnp Transistors on the RCA CD4007A and CD4041A.

Circuit	Transistor	Emitter Connection	Base Connection	Collector Connection	h_{fe}(peak)
4007	npn1	3,6,10,4,9,5,8	7	14	100.
4007	pnp1	6	14	7	0.4
4007	pnp2	3,10	14	7	0.08
4007	pnp3	2,11	14	7	0.04
4041	npn1	1,2,4,5,8,9,11,12	7	14	13.
4041	pnp1	3,6,10,13	14	7	0.07
4041	pnp2	1,2,4,5,8,9,11,12	14	7	0.03

Table II

Pin Connections for Typical pnpn Paths on the 4007

Circuit	Path	Pin Numbers			
		Anode	Gate 2	Gate 1	Cathode
4007	Connection 1	6	14	7	4
4007	Connection 2	2	14	7	4

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

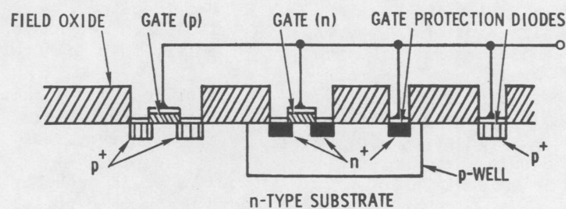
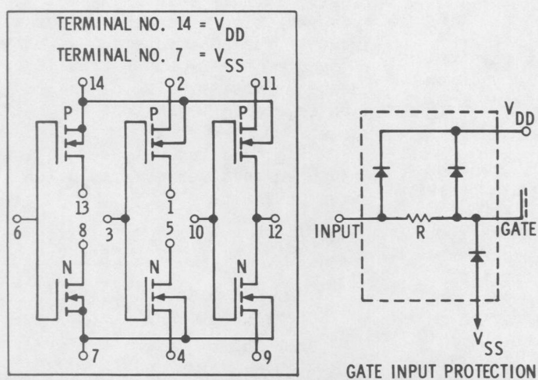


Figure 1. Cross-sectional View of a Typical CMOS Inverter Structure.



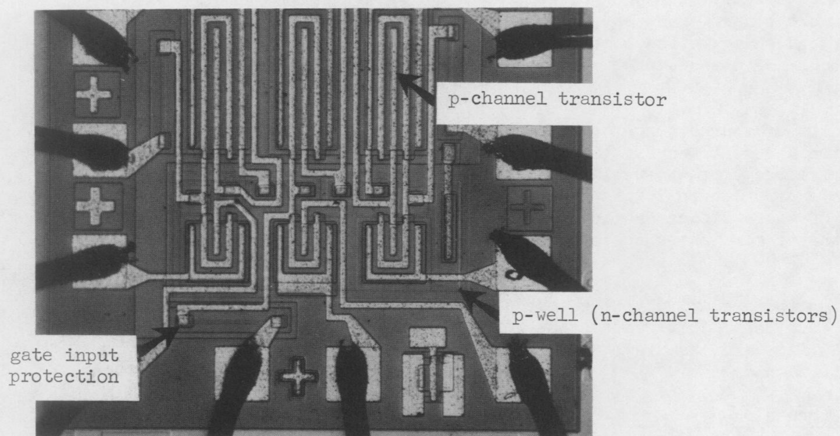


Figure 2. Layout and Schematic for the RCA CD4007A CMOS Integrated Circuit.

DOCKET ALARM
Find authenticated court documents without watermarks at docketalarm.com.

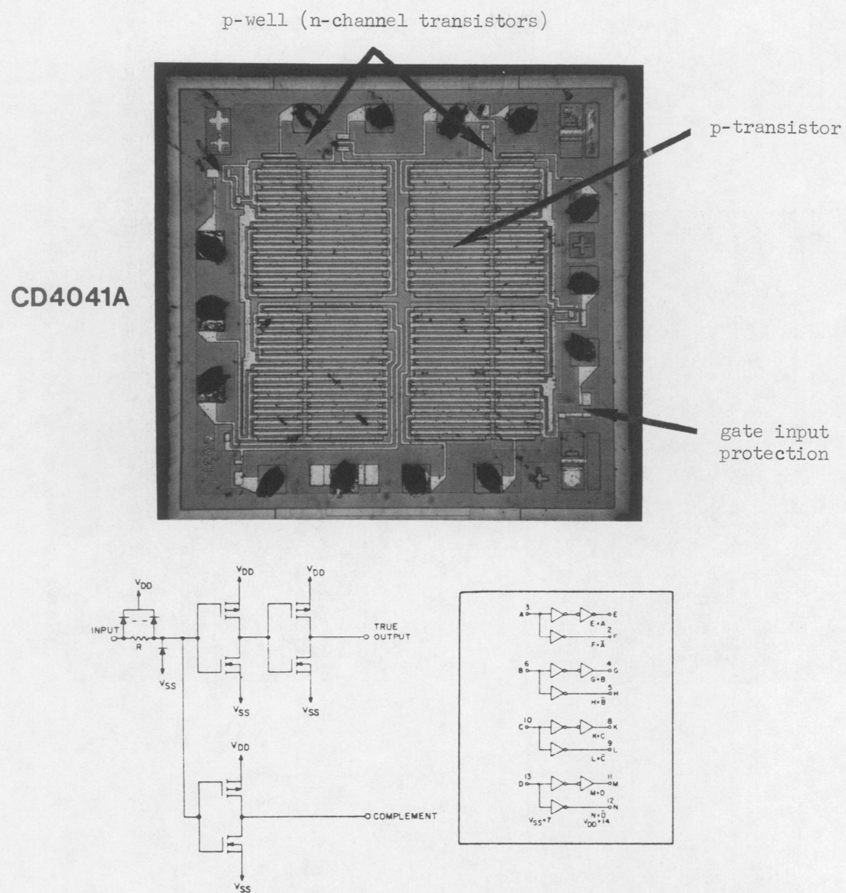


Figure 3. Layout and Schematic of the RCA CD4041A CMOS IC.

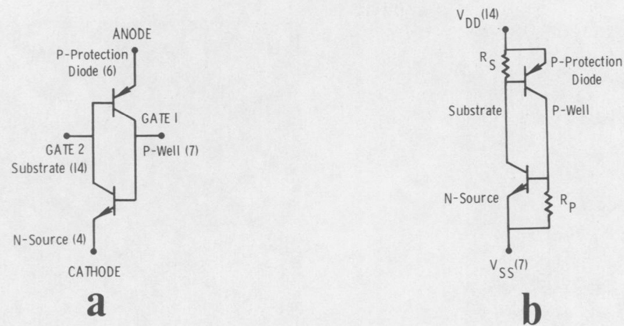


Figure 4. Equivalent Circuits for the SCR Structures Present on 4007 for a) Worst-Case Bias and b) Normal Inverter Bias -- Input High.

DOCKET ALARM Find authenticated court documents without watermarks at docketalarm.com.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.

WHAT WILL YOU BUILD? | sales@docketalarm.com | 1-866-77-FASTCASE

fastcase®
Smarter legal research.