which connection or isolation methods are used, and consequently determines the width and height of the cell.

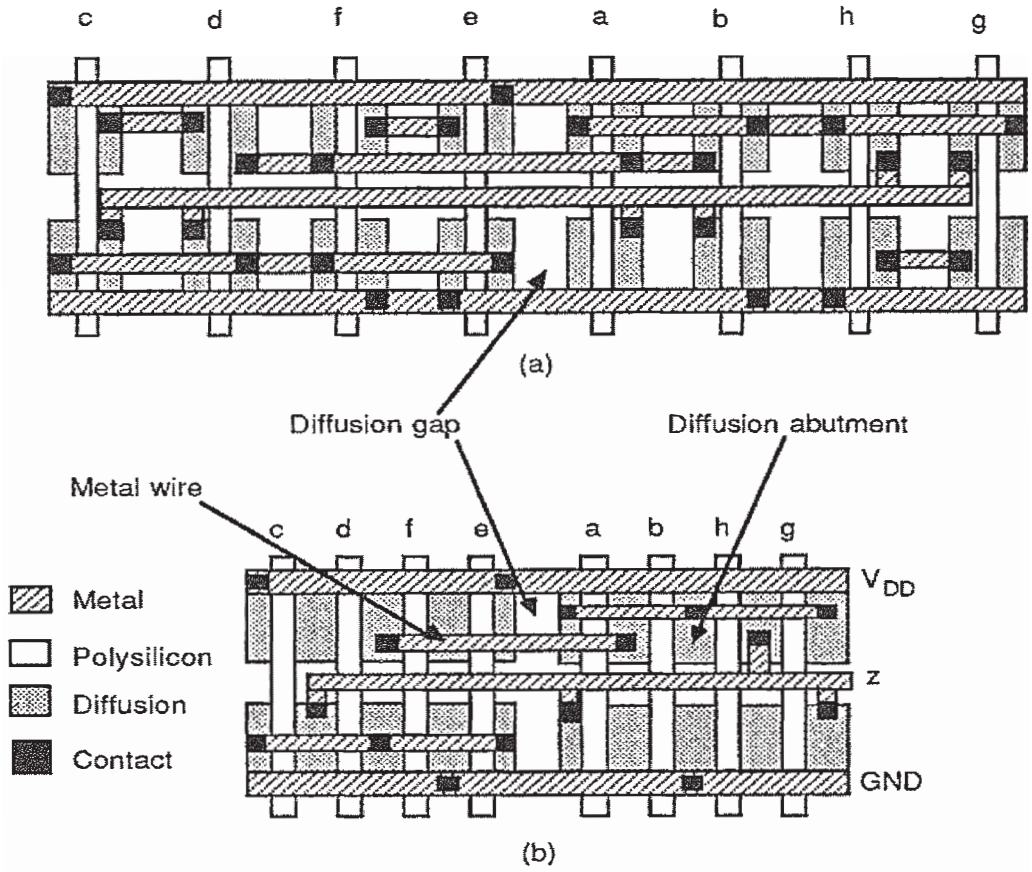

Fig. 2.3. A functional cell: (a) with no diffusion abutment; (b) with diffusion abutment.

The rules for the various interconnection methods allowed by the seventh assumption are now given. Drain-source terminals that are connected in the transistor circuit and that are also adjacent in the cell are connected by diffusion abutment; this case is illustrated in Fig. 2.3(b), where transistors *b* and *h* are connected in this way. Transistors connected in the circuit but nonadjacent in the

cell are connected by horizontal metal wires; Fig. 2.3(b) shows a metal wire in the pullup subcircuit connecting the diffusion region between columns d and f to the region between columns a and b. Drain or source terminals of two transistors not connected in the circuit but adjacent in the cell are isolated by an area-wasting diffusion gap. In Fig. 2.2, transistors e and a are not connected in the pulldown circuit, but are adjacent in the layout of Fig. 2.3(b); therefore, a diffusion gap is required between them.

We illustrate the layout process with Fig. 2.3. Assume we choose to place the dual transistor pairs in the cell in the left-to-right order of c, d, f, e, a, b, h and g. Each transistor is *oriented* in one of two ways, such that its drain terminal is either to the left or the right of its polysilicon gate terminal. First, let us consider the cell of Fig. 2.3(a) which uses only the metal layer to interconnect drain-source transistor terminals. A diffusion gap is placed between each pair of transistors, whether the adjacent terminals are to be electrically connected or not. Note that if only metal interconnections were used, all placements of transistors would result in a cell of the same width W. In this case, $W = T + G + 1 = 8 + 7 + 1 = 16$ units (columns). However, by choosing a good placement and orientation of the transistor pairs, and using diffusion abutment, the width of the cell can be reduced. Figure. 2.3(b) shows a layout having the same transistor placement and orientation as that in Fig. 2.3(a), but using abutment wherever applicable. The cell width $W = 8 + 1 + 1 = 10$ columns. The height of the cell of Fig. 2.3(b) in terms of the number of metal rows is seven.

The height minimization problem depends on the number of metal interconnection layers used within a cell. Traditionally, one layer of metal is provided for interconnection purposes by chip fabrication processes, although more recently two or more layers have become available. Some layout styles use more than one metal layer for routing within a cell, whereas other styles employ only one metal layer in the cell even when more are available, reserving the other layers of metal for connections between cells. If more than one layer of metal is used within a cell, then in some cases cell height can be made smaller than the height of a cell using only one metal layer. The height problem is also affected by the number of contacts required between a metal layer and the other layers to ensure that a given fabrication process produces a reasonable percentage of working chips and that the total contact resistance is low enough for good circuit performance. For these reasons, multiple contacts become particularly important for submicron processes. The height of a cell may be larger if multiple contacts are required, when compared to a cell using single contacts. The vast majority of prior layout methods use a single layer of metal for cell interconnection; moreover, almost all of them use a single contact between metal layers and the other layers.