PREFACE

The layout of an integrated circuit (IC) is the process of assigning geometric shape, size and position to the components (transistors and connections) used in its fabrication. Since the number of components in modern ICs is enormous, computer-aided-design (CAD) programs are required to automate the difficult layout process. Prior CAD methods are inexact or limited in scope, and produce layouts whose area, and consequently manufacturing costs, are larger than necessary. This book addresses the problem of minimizing exactly the layout area of an important class of basic IC structures called CMOS cells.

First, we precisely define the possible goals in area minimization for such cells, namely width and height minimization, with allowance for area-reducing reordering of transistors. We reformulate the layout problem in terms of a graph model and develop new graph-theoretic concepts that completely characterize the fundamental area minimization problems for series-parallel and nonseries-parallel circuits. These concepts lead to practical algorithms that solve all the basic layout minimization problems exactly, both for a single cell and for a one-dimensional array of such cells. Although a few of these layout problems have been solved or partially solved previously, we present here the first complete solutions to all the problems of interest.

We have implemented our algorithms by means of computer programs, and demonstrate that they efficiently generate minimum-area layouts for all possible cells of practical size. An analysis of these layouts permits us to make the first comprehensive evaluation of the quality and scope of prior layout methods. We show that most previous layout optimization algorithms are limited in scope, and cannot find optimal layouts for a large percentage of practical circuits. We also compare our optimal layouts to those of nonoptimal heuristic methods, and demonstrate that our exact algorithms produce significantly smaller cells.

This book will be of interest to designers of circuits or CAD tools, and others concerned with generating highly compact layouts for ICs. Chapter 1 introduces the subject of IC layout, and surveys traditional layout styles. Chapter 2 gives a brief tutorial on the cell layout problem, and evaluates the effectiveness of prior cell layout

techniques at minimizing area. Chapter 3 develops our general theory of cell layout and presents algorithms for generating minimum-width cells for series-parallel circuits; Chapter 4 generalizes these results for the nonseries-parallel case. Chapter 5 presents an algorithm that generates minimum-width and -height cells, and these results are extended to an array of cells in Chapter 6. Chapter 7 summarizes the book and suggests applications and extensions to this work.

Most of the material in this book was developed over the past few years as part of the first author's Ph.D. dissertation research at the University of Michigan. This research was supported by grants from the Office of Naval Research and the National Science Foundation, and by fellowships from the Burroughs (now part of Unisys) and Schlumberger Corporations. We wish to express our gratitude to these organizations. We also thank William P. Birmingham, Richard B. Brown, Philip J. Hanlon and Ronald J. Lomax of the University of Michigan for their suggestions.

LAYOUT MINIMIZATION OF CMOS CELLS

CHAPTER I
INTRODUCTION

We begin by discussing the general design problem for integrated circuits, and the role of the cell layout problem in relation to it. Next, we survey the popular cell layout styles for integrated circuits. The cell layout area minimization problem we address is defined and prior work on it is evaluated. We conclude with a discussion of our approach to exact layout optimization.

1.1 PROBLEM AND MOTIVATION

Since the introduction of the first commercial integrated circuit (IC) in 1961, the capacity of digital integrated circuits has been increasing at a rapid pace. Commercial IC chips in the 1960's had about 100 transistors. Through dramatic improvements in fabrication technology, very large scale integrated (VLSI) circuits with over ten million transistors are being fabricated at present, and the number of transistors per chip tends to double every year or two. The design of chips with such huge numbers of transistors presents major problems in design effort and cost. Computer-aided design (CAD) tools were developed to help designers cope with these problems. Such tools now play a key role in managing design complexity and improving designer productivity.

The design of a VLSI chip is a complicated process requiring many intermediate steps. Typically, several hierarchical levels of representation are used in the design process; see Fig. 1.1. One of the higher levels is the *register transfer level*, where the variables and the data operators represent the hardware registers and functional blocks of the data-processing section of a chip. The control section implements the sequencing of operations implied by the register transfer description. Next comes the *logic level*, at which the functional blocks are basic logic units called *gates*, such as the AND and NOR gates shown in Fig. 1.1(b); these gates implement the carry function of the adder in Fig. 1.1(a). At the *transistor level*, the logic gates are decomposed into transistor circuits. The NOR gate of Fig. 1.1(b) is translated into the transistor circuit of Fig. 1.1(c), where a *transistor* is a three-terminal device with

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.