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(54) **MEMORY SYSTEM TOPOLOGIES INCLUDING A BUFFER DEVICE AND AN INTEGRATED CIRCUIT MEMORY DEVICE**

(71) Applicant: **Rambus Inc.**, Sunnyvale, CA (US)

(72) Inventors: **Ian Shaeffer**, Los Gatos, CA (US); **Ely Tsern**, Los Altos, CA (US); **Craig Hampel**, Los Altos, CA (US)

(73) Assignee: **Rambus Inc.**, Sunnyvale, CA (US)

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(57) **ABSTRACT**

Systems, among other embodiments, include topologies (data and/or control/address information) between an integrated circuit buffer device (that may be coupled to a master, such as a memory controller) and a plurality of integrated circuit memory devices. For example, data may be provided between the plurality of integrated circuit memory devices and the integrated circuit buffer device using separate segmented (or point-to-point link) signal paths in response to control/address information provided from the integrated circuit buffer device to the plurality of integrated circuit buffer devices using a single fly-by (or bus) signal path. An integrated circuit buffer device enables configurable effective memory organization of the plurality of integrated circuit memory devices. The memory organization represented by the integrated circuit buffer device to a memory controller may be different than the actual memory organization behind or coupled to the integrated circuit buffer device. The buffer device segments and merges the data transferred between the memory controller that expects a
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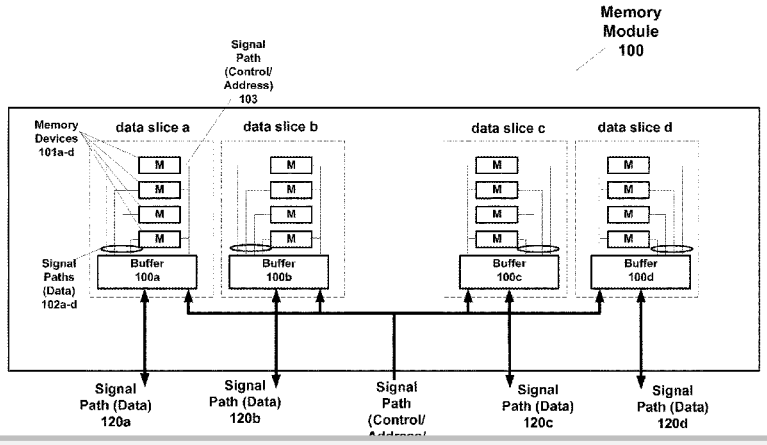

particular memory organization and actual memory organization.

20 Claims, 38 Drawing Sheets

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(58) **Field of Classification Search**

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See application file for complete search history.

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