



FEATURES

- Complete supervisory and sequencing solution for up to 10 supplies
- 10 supply fault detectors enable supervision of supplies to <0.5% accuracy at all voltages at 25°C
- <1.0 % accuracy across all voltages and temperatures
- 5 selectable input attenuators allow supervision
 - Supplies up to 14.4 V on VH
 - Supplies up to 6 V on VP1 to VP4
- 5 dual-function inputs, VX1 to VX5
 - High impedance input to supply fault detector with thresholds between 0.573 V and 1.375 V
 - General-purpose logic input
- 10 programmable output drivers, PDO1 to PDO10
 - Open collector with external pull-up
 - Push/pull output, driven to VDDCAP or VPn
 - Open collector with weak pull-up to VDDCAP or VPn
 - Internally charge-pumped high drive for use with external N-FET (PDO1 to PDO6 only)
- Sequencing engine (SE) implements state machine control of PDO outputs
 - State changes conditional on input events
 - Enables complex control of boards
 - Power-up and power-down sequence control
 - Fault event handling
 - Interrupt generation on warnings
 - Watchdog function can be integrated in SE
 - Program software control of sequencing through SMBus
- Complete voltage-margining solution for 6 voltage rails
- 6 voltage output 8-bit DACs (0.300 V to 1.551 V) allow voltage adjustment via dc-to-dc converter trim/feedback node
- 12-bit ADC for readback of all supervised voltages
- 2 auxiliary (single-ended) ADC inputs
- Reference input (REFIN) has 2 input options
 - Driven directly from 2.048 V ($\pm 0.25\%$) REFOUT pin
 - More accurate external reference for improved ADC performance
- Device powered by the highest of VPn or VH for improved redundancy
- User EEPROM: 256 bytes
- Industry-standard 2-wire bus interface (SMBus)
- Guaranteed PDO low with VH, VPn = 1.2 V
- 40-lead 6 mm x 6 mm LFCSP
- 48-lead 7 mm x 7 mm TQFP

For more information about the ADM1066 register map, refer to the [AN-698 Application Note](#).

Rev. B

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FUNCTIONAL BLOCK DIAGRAM

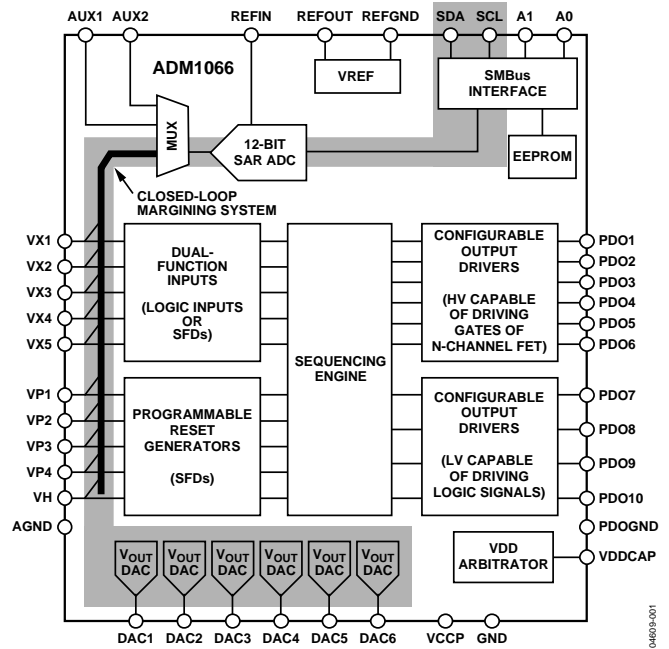


Figure 1.

APPLICATIONS

- Central office systems
- Servers/routers
- Multivoltage system line cards
- DSP/FPGA supply sequencing
- In-circuit testing of margined supplies

GENERAL DESCRIPTION

The ADM1066 is a configurable supervisory/sequencing device that offers a single-chip solution for supply monitoring and sequencing in multiple-supply systems. In addition to these functions, the ADM1066 integrates a 12-bit ADC and six 8-bit voltage output DACs. These circuits can be used to implement a closed-loop margining system that enables supply adjustment by altering either the feedback node or reference of a dc-to-dc converter using the DAC outputs.

(continued on Page 4)

TABLE OF CONTENTS

Features	1	SMBus Jump/Unconditional Jump	20
Functional Block Diagram	1	Sequencing Engine Application Example	21
Applications.....	1	Fault and Status Reporting.....	23
General Description	1	Voltage Readback.....	24
Revision History	3	Supply Supervision with the ADC.....	24
General Description	4	Supply Margining	25
Specifications.....	5	Overview	25
Pin Configurations and Function Descriptions	8	Open-Loop Margining	25
Absolute Maximum Ratings.....	10	Closed-Loop Supply Margining	25
Thermal Characteristics	10	Writing to the DACs	26
ESD Caution.....	10	Choosing the Size of the Attenuation Resistor.....	26
Typical Performance Characteristics	11	DAC Limiting/Other Safety Features	26
Powering the ADM1066	14	Applications Diagram	27
Inputs.....	15	Communicating with the ADM1066.....	28
Supply Supervision.....	15	Configuration Download at Power-Up.....	28
Programming the Supply Fault Detectors.....	15	Updating the Configuration	28
Input Comparator Hysteresis.....	16	Updating the Sequencing Engine.....	29
Input Glitch Filtering	16	Internal Registers.....	29
Supply Supervision with VXn Inputs	16	EEPROM	29
VXn Pins as Digital Inputs.....	16	Serial Bus Interface.....	29
Outputs	18	SMBus Protocols for RAM and EEPROM.....	32
Supply Sequencing through Configurable Output Drivers..	18	Write Operations	32
Default Output Configuration.....	19	Read Operations.....	34
Sequencing Engine	20	Outline Dimensions	35
Overview.....	20	Ordering Guide	36
Warnings.....	20		

REVISION HISTORY

5/06—Rev. A to Rev. B

Changes to Features Section 1
 Changes to Table 1 5
 Changes to Table 2 8
 Changes to Table 3 10
 Added Table 4 10
 Added Default Output Configuration Section..... 19
 Changes to Fault Reporting Section 19
 Added Table 11 30
 Changes to Ordering Guide..... 36

1/05—Rev. 0 to Rev. A

Changes to Figure 1 1
 Changes to Absolute Maximum Ratings Section 8
 Change to Supply Sequencing through Configurable
 Output Drivers Section 16
 Changes to Figure 33 23
 Change to Table 10..... 32

10/04—Revision 0: Initial Version

GENERAL DESCRIPTION

(continued from Page 1)

Supply margining can be performed with a minimum of external components. The margining loop can be used for in-circuit testing of a board during production (for example, to verify the board's functionality at -5% of nominal supplies), or can be used dynamically to accurately control the output voltage of a dc-to-dc converter.

The device also provides up to 10 programmable inputs for monitoring under, over, or out-of-window faults on up to 10 supplies. In addition, 10 programmable outputs can be used as logic enables. Six of them can also provide up to a 12 V output for driving the gate of an N-channel FET, which can be placed in the path of a supply.

The logical core of the device is a sequencing engine. This state-machine-based construction provides up to 63 different states. This design enables very flexible sequencing of the outputs, based on the condition of the inputs.

The device is controlled via configuration data that can be programmed into an EEPROM. The whole configuration can be programmed using an intuitive GUI-based software package provided by Analog Devices, Inc.

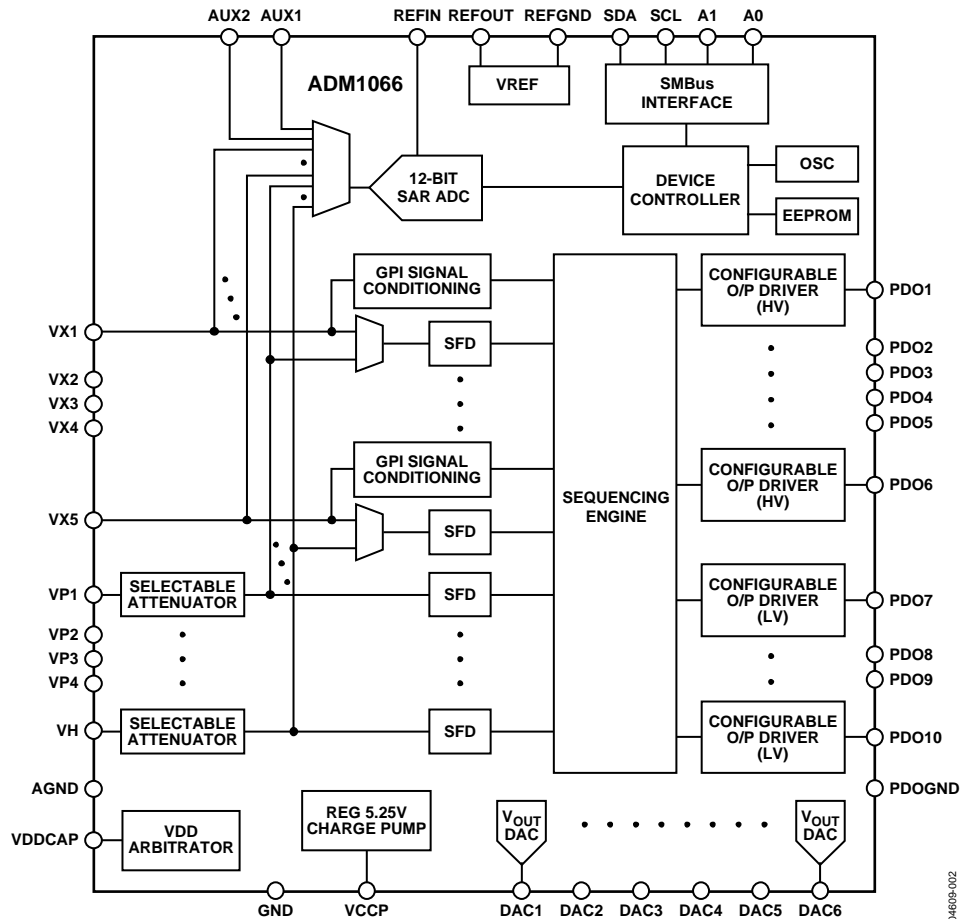


Figure 2. Detailed Block Diagram

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SPECIFICATIONS

V_H = 3.0 V to 14.4 V¹, V_{Pn} = 3.0 V to 6.0 V¹, T_A = -40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY ARBITRATION					
V _H , V _{Pn}	3.0			V	Minimum supply required on one of V _{Pn} , V _H
V _P			6.0	V	Maximum V _{DDCAP} = 5.1 V, typical
V _H			14.4	V	V _{DDCAP} = 4.75 V
V _{DDCAP}	2.7	4.75	5.4	V	Regulated LDO output
C _{VDDCAP}	10			μF	Minimum recommended decoupling capacitance
POWER SUPPLY					
Supply Current, I _{VH} , I _{VPn}		4.2	6	mA	V _{DDCAP} = 4.75 V, PDO1 to PDO10 off, DACs off, ADC off
Additional Currents					
All PDO FET Drivers On		1		mA	V _{DDCAP} = 4.75 V, PDO1 to PDO6 loaded with 1 μA each, PDO7 to PDO10 off
Current Available from V _{DDCAP}			2	mA	Maximum additional load that can be drawn from all PDO pull-ups to V _{DDCAP}
DACs Supply Current		2.2		mA	6 DACs on with 100 μA maximum load on each
ADC Supply Current		1		mA	Running round-robin loop
EEPROM Erase Current		10		mA	1 ms duration only, V _{DDCAP} = 3 V
SUPPLY FAULT DETECTORS					
V_H Pin					
Input Impedance		52		kΩ	Midrange and high range
Input Attenuator Error		±0.05		%	
Detection Ranges					
High Range	6		14.4	V	
Midrange	2.5		6	V	
V_{Pn} Pins					
Input Impedance		52		kΩ	Low range and midrange
Input Attenuator Error		±0.05		%	
Detection Ranges					
Midrange	2.5		6	V	
Low Range	1.25		3	V	
Ultralow Range	0.573		1.375	V	No input attenuation error
V_X Pins					
Input Impedance	1			MΩ	No input attenuation error
Detection Ranges					
Ultralow Range	0.573		1.375	V	
Absolute Accuracy			±1	%	
Threshold Resolution		8		Bits	
Digital Glitch Filter		0		μs	Minimum programmable filter length
		100		μs	Maximum programmable filter length
ANALOG-TO-DIGITAL CONVERTER					
Signal Range	0		V _{REFIN}	V	The ADC can convert signals presented to the V _H , V _{Pn} , and V _{Xn} pins. V _{Pn} and V _H input signals are attenuated depending on the selected range. A signal at the pin corresponding to the selected range is from 0.573 V to 1.375 V at the ADC input.
Input Reference Voltage on REFIN Pin, V _{REFIN}		2.048		V	
Resolution		12		Bits	
INL			±2.5	LSB	Endpoint corrected, V _{REFIN} = 2.048 V

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