October 2005

FAIRCHILD SEMICONDUCTOR®

FAN5026
Dual DDR/Dual-Output PWM Controller

Features

- Highly flexible dual synchronous switching PWM controller includes modes for:
  - DDR mode with in-phase operation for reduced channel interference
  - 90° phase shifted two-stage DDR Mode for reduced input ripple
  - Dual Independent regulators 180° phase shifted
- Complete DDR Memory power solution
  - VTT Tracks VDDQ/2
  - VDDQ/2 Buffered Reference Output
- Lossless current sensing on low-side MOSFET or Precision current sensing using sense resistor
- VCC Under-voltage Lockout
- Wide power input range: 3 to 16V
- Excellent dynamic response with Voltage Feed-Forward and Average Current Mode control
- Power-Good Signal
- Supports DDR-II and HSTL
- TSSOP28 package

Applications

- DDR V_{DDQ} and V_{TT} voltage generation
- Desktop computer
- Graphics cards

General Description

The FAN5026 PWM controller provides high efficiency and regulation for two output voltages adjustable in the range from 0.9V to 5.5V that are required to power I/O, chip-sets, and memory banks in high-performance computers, set top boxes, and VGA cards. Synchronous rectification contributes to high efficiency over a wide range of loads. Efficiency is even further enhanced by using MOSFET's $R_{DS(ON)}$ as a current sense component.

Feed-forward ramp modulation, average current mode control scheme, and internal feedback compensation provide fast response to load transients. Out-of-phase operation with 180° phase shift reduces input current ripple. The controller can be transformed into a complete DDR memory power supply solution by activating a designated pin. In DDR mode of operation one of the channels tracks the output voltage of another channel and provides output current sink and source capability — features essential for proper powering of DDR chips. The buffered reference voltage required by this type of memory is also provided. The FAN5026 monitors these outputs and generates separate PGx (power good) signals when the soft-start is completed and the output is within ±10% of its set point. A built-in over-voltage protection prevents the output voltage from going above 120% of the set point. Normal operation is automatically restored when the over-voltage conditions go away. Under-voltage protection latches the chip off when either output drops below 75% of its set value after the soft-start sequence for this output is completed. An adjustable over-current function monitors the output current by sensing the voltage drop across the lower MOSFET. If precision current-sensing is required, an external current-sense resistor may optionally be used.

Ordering Information

Part Number	Temperature Range	Package	Packing
FAN5026MTC	-40°C to 85°C	TSSOP-28	Rails
FAN5026MTCX	-40°C to 85°C	TSSOP-28	Tape and Reel

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Block Diagrams

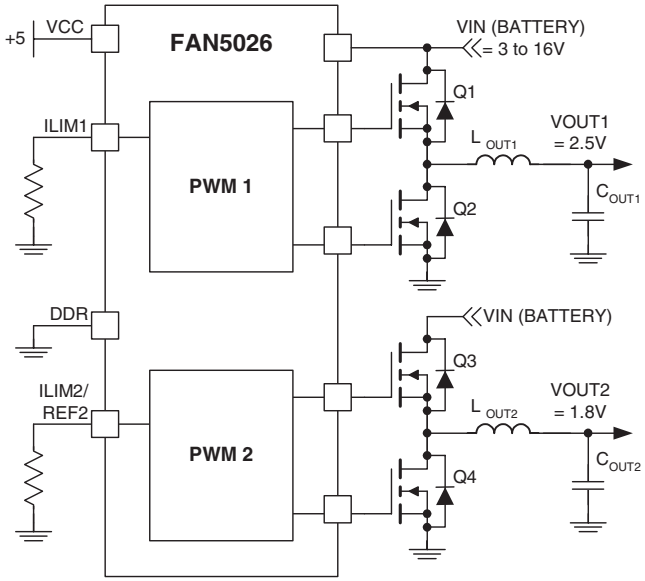

Figure 1. Dual Output Regulator

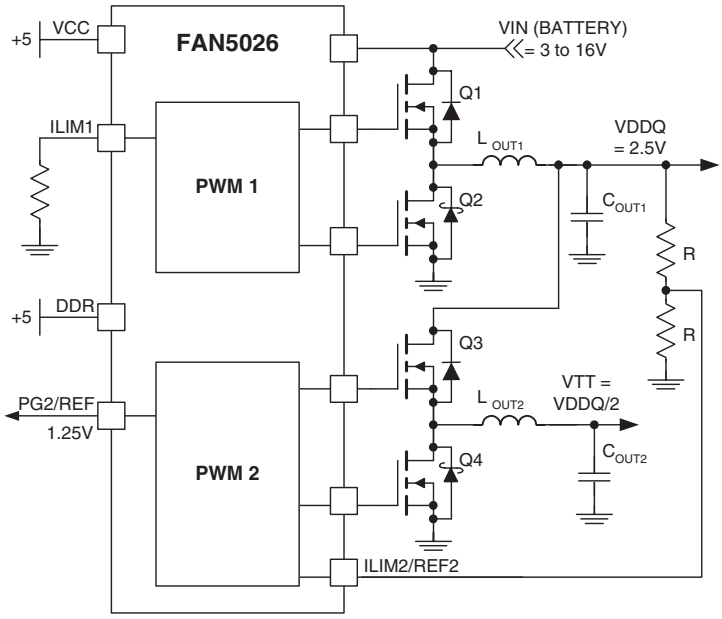

Figure 2. Typical Application

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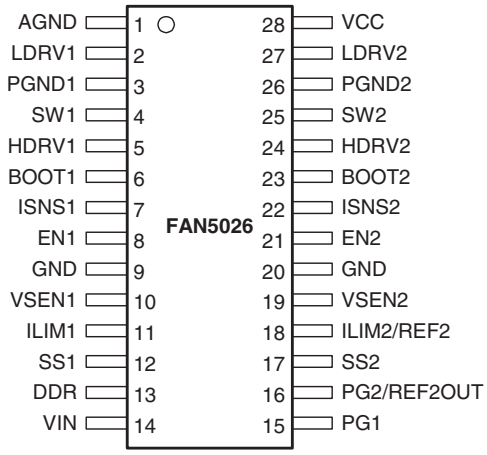
Pin Configurations



TSSOP-28

θ_{JA} = 50°C/W; θ_{JC} = 16°C/W. See note below.

Note: θ_{JA} and θ_{JC} values are determined using a 4 layer, 1" square PCB with 1 ounce copper.

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	AGND	**Analog Ground**. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
2 27	LDRV1 LDRV2	**Low-Side Drive**. The low-side (lower) MOSFET driver output. Connect to gate of low-side MOSFET.
3 26	PGND1 PGND2	**Power Ground**. The return for the low-side MOSFET driver. Connect to source of low-side MOSFET.
4 25	SW1 SW2	**Switching Node**. Return for the high-side MOSFET driver and a current sense input. Connect to source of high-side MOSFET and low-side MOSFET drain.
5 24	HDRV1	**High-Side Drive**. High-side (upper) MOSFET driver output. Connect to gate of high-side MOSFET.
6 23	BOOT1 BOOT2	**BOOT**. Positive supply for the upper MOSFET driver. Connect as shown in Figure 3.
7 22	ISNS1 ISNS2	**Current Sense Input**. Monitors the voltage drop across the lower MOSFET or external sense resistor for current feedback.
8 21	EN1 EN2	**Enable**. Enables operation when pulled to logic high. Toggling EN will also reset the regulator after a latched fault condition. These are CMOS inputs whose state is indeterminate if left open.
9 20	GND	**Ground**. These pins should be tied to AGND for proper operation.
10 19	VSEN1 VSEN2	**Output Voltage Sense**. The feedback from the outputs. Used for regulation as well as PG, under-voltage and over-voltage protection and monitoring.
11	ILIM1	**Current Limit 1**. A resistor from this pin to GND sets the current limit.
12 17	SS1 SS2	**Soft Start**. A capacitor from this pin to GND programs the slew rate of the converter during initialization. During initialization, this pin is charged with a 5µA current source.

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Pin Definitions (Continued)

Pin Number	Pin Name	Pin Function Description
13	DDR	**DDR Mode Control**. High = DDR mode. Low = 2 separate regulators operating 180° out of phase.
14	VIN	**Input Voltage**. Normally connected to battery, provides voltage feed-forward to set the amplitude of the internal oscillator ramp. When using the IC for 2-step conversion from 5V input, connect through 100K to ground, which will set the appropriate ramp gain and synchronize the channels 90° out of phase.
15	PG1	**Power Good Flag**. An open-drain output that will pull LOW when VSEN is outside of a ±10% range of the 0.9V reference.
16	PG2 / REF2OUT	**Power Good 2**. When not in DDR Mode: Open-drain output that pulls LOW when the VOUT is out of regulation or in a fault condition **Reference Out 2**. When in DDR Mode, provides a buffered output of REF2. Typically used as the VDDQ/2 reference.
18	ILIM2 / REF2	**Current Limit 2**. When not in DDR Mode, A resistor from this pin to GND sets the current limit. **Reference** for reg #2 when in DDR Mode. Typically set to VOUT1/2.
28	VCC	**VCC**. This pin powers the chip as well as the LDRV buffers. The IC starts to operate when voltage on this pin exceeds 4.6V (UVLO rising) and shuts down when it drops below 4.3V (UVLO falling).

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Parameter	Min.	Typ.	Max.	Units
VCC Supply Voltage			6.5	V
VIN			18	V
BOOT, SW, ISNS, HDRV			24	V
BOOT to SW			6.5	V
All Other Pins	–0.3		VCC+0.3	V
Junction Temperature (T_J)	–40		150	°C
Storage Temperature	–65		150	°C
Lead Soldering Temperature, 10 seconds			300	°C

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC		4.75	5	5.25	V
Supply Voltage VIN				16	V
Ambient Temperature (T_A)	note 1	–40		85	°C

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Electrical Specifications Recommended operating conditions, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies					
VCC Current	LDRV, HDRV Open, VSEN forced above regulation point		2.2	3.0	mA
	Shut-down (EN=0)			30	µA
VIN Current – Sinking	VIN = 15V	10		30	µA
VIN Current – Sourcing	VIN = 0V		–15	–30	µA
VIN Current – Shut-down				1	µA
UVLO Threshold	Rising VCC	4.3	4.55	4.75	V
	Falling	4.1	4.25	4.45	V
UVLO Hysteresis			300		mV
Oscillator					
Frequency		255	300	345	KHz
Ramp Amplitude, pk–pk	VIN = 16V		2		V
Ramp Amplitude, pk–pk	VIN = 5V		1.25		V
Ramp Offset			0.5		V
Ramp / VIN Gain	VIN ≥ 3V		125		mV/V
Ramp / VIN Gain	1V < VIN < 3V		250		mV/V
Reference and Soft Start					
Internal Reference Voltage		0.891	0.9	0.909	V
Soft Start Current (I_{SS})	at start-up		–5		µA
Soft Start Complete Threshold			1.5		V
PWM Converters					
Load Regulation	I_{OUTX} from 0 to 5A, VIN from 5 to 15V	-2		+2	%
VSEN Bias Current		50	80	120	nA
Under-Voltage Shutdown	as % of set point. 2µS noise filter	70	75	80	%
Over-Voltage Threshold	as % of set point. 2µS noise filter	115	120	125	%
I_{SNS} Over-Current Threshold	R_{ILIM}= 68.5KΩ see Figure 10.	112	140	168	µA
Minimum Duty Cycle		10			%
Output Drivers					
HDRV Output Resistance	Sourcing		12	15	Ω
	Sinking		2.4	4	Ω
LDRV Output Resistance	Sourcing		12	15	Ω
	Sinking		1.2	2	Ω
PG (Power Good Output) and Control pins					
Lower Threshold	as % of set point, 2µS noise filter	–86		–94	%
Upper Threshold	as % of set point, 2µS noise filter	108		116	%
PG Output Low	IPG = 4mA			0.5	V
Leakage Current	V_{PULLUP} = 5V			1	µA
PG2/REF2OUT Voltage	DDR = 1, 0 mA < $I_{REF2OUT}$ ≤ 10mA	99		1.01	% V_{REF2}
DDR, EN Inputs					
Input High		2			V
Input Low				0.8	V

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