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(54) **STORAGE SUBSYSTEM WITH EMBEDDED CIRCUIT FOR PROTECTING AGAINST ANOMALIES IN POWER SIGNAL FROM HOST**

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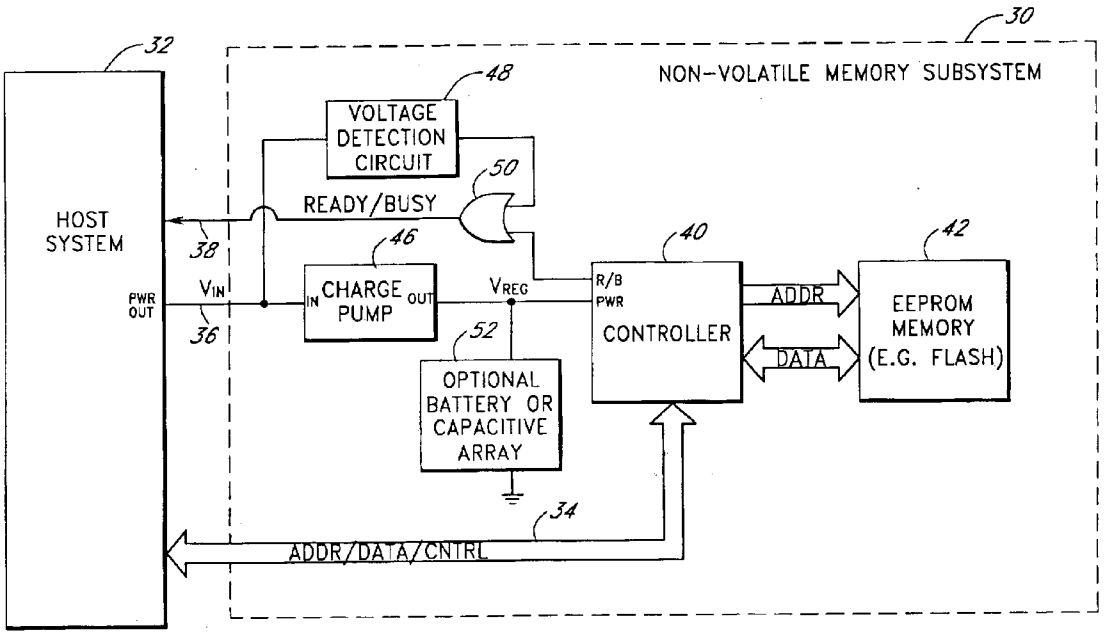
(57) **ABSTRACT**

A storage subsystem, such as a flash memory card, includes a charge pump that receives a power signal from a host system, and generates a regulated power signal that is provided to the storage subsystem's controller. When the power signal from the host is interrupted, the charge pump additionally acts as a backup power supply such that the storage subsystem can continue to operate temporarily. The storage subsystem also includes a voltage detection circuit that monitors the power signal from the host system to detect anomalies therein. The voltage detection circuit responds to detection of an anomaly by asserting a busy signal to block the host system from performing write operations to the storage subsystem. By asserting the busy signal, the voltage detection circuit substantially ensures that the backup, regulated power provided by the charge pump will be sufficient for the controller to complete all outstanding operations.

38 Claims, 2 Drawing Sheets



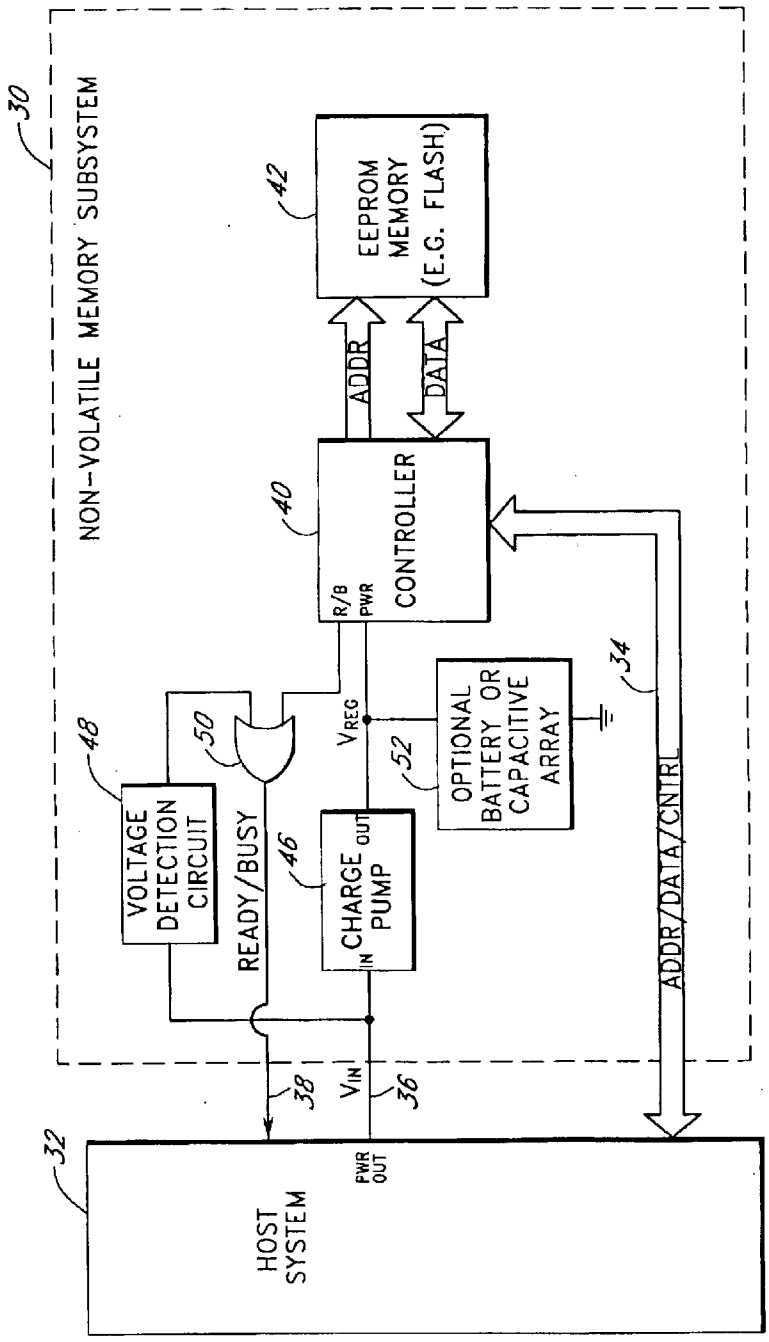


FIG. 1

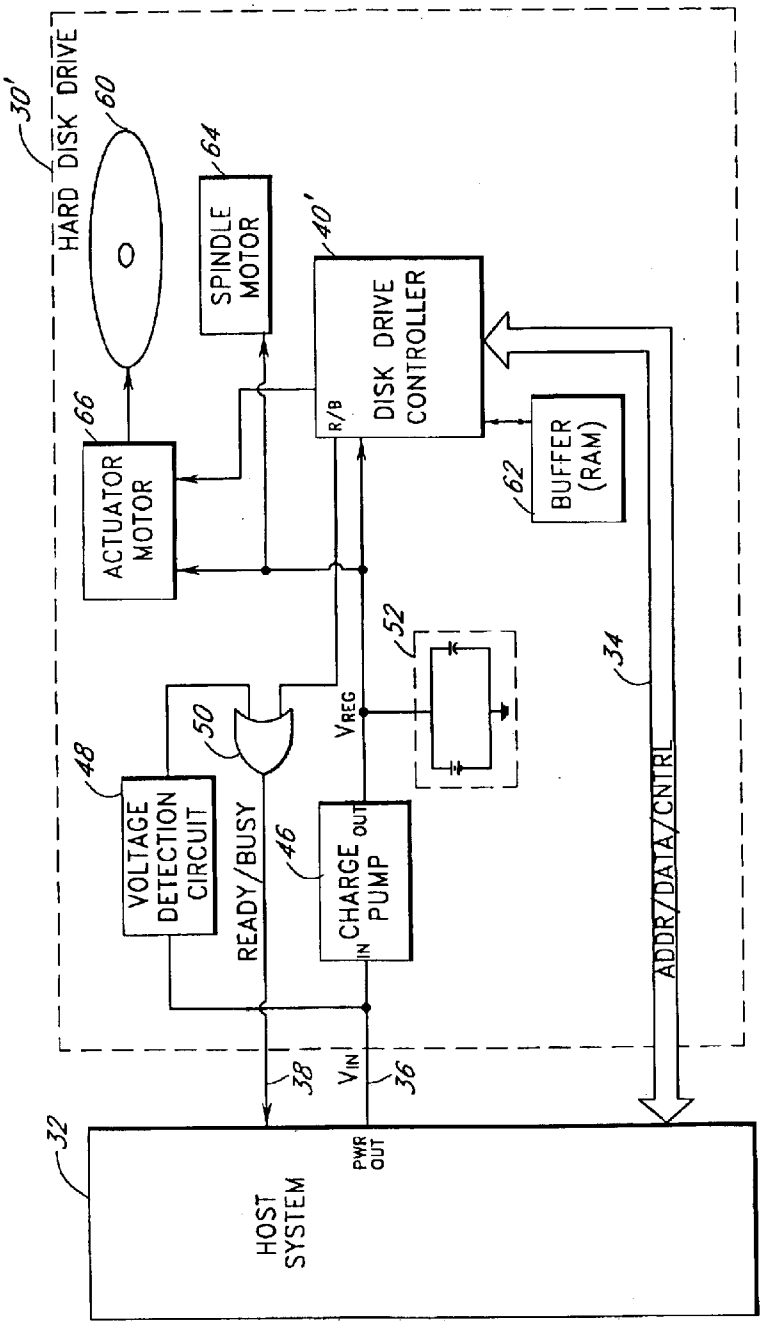


FIG. 2

STORAGE SUBSYSTEM WITH EMBEDDED CIRCUIT FOR PROTECTING AGAINST ANOMALIES IN POWER SIGNAL FROM HOST

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to circuits from protecting storage subsystems, such as but not limited to flash memory cards, from damage and data loss caused by irregularities in a power signal provided by a host.

2. Description of the Related Art

A significant problem in the area of storage subsystems relates to data loss, data corruption, and circuitry damage caused by interruptions and other irregularities in the power signal supplied by the host system. For example, in the context of a flash memory subsystem, an unexpected power loss can cause a sector write operation to terminate prematurely, resulting in a mismatch between a sector's data and ECC portions. In addition to losing the write data, the memory subsystem's controller may thereafter respond to the ECC mismatch condition by treating the sector as defective, and unnecessarily replacing the sector with a spare sector. Incomplete sector write operations can also result in data loss and sector replacement in disk drives that store data on a rotating medium. Other types of power signal anomalies, such as power surges and spikes, can additionally cause permanent damage to the circuitry of the storage subsystem.

SUMMARY OF THE INVENTION

The present invention provides a circuit and associated method for protecting a storage subsystem from irregularities in a power signal supplied by a host system. The invention may be embodied within a variety of different types of storage subsystems, including but not limited to non-volatile solid state memory cards (such as but not limited to those that comply with the CompactFlash, PCMCIA, SmartMedia, MultiMediaCard, SecureDigital and Memory Stick card specifications), volatile and non-volatile solid-state storage products in disk drive form factors, electro-mechanical disk drives, and volatile and non-volatile solid-state storage products in a variety of industry standard and custom form factors. No modifications are needed to the host system.

In one embodiment, the storage subsystem includes a charge pump circuit that receives the power signal from a host system, and generates a regulated power signal that is provided to the storage subsystem's controller (and possibly to other active components of the storage subsystem). When the power signal from the host is interrupted, the charge pump circuit acts as a backup power source such that the storage subsystem can continue to operate temporarily. A rechargeable battery and/or a capacitive array may also be provided as additional sources of backup power. In addition to providing backup power, the charge pump circuit protects the controller from potential damage caused by power surges and spikes.

The storage subsystem in the preferred embodiment also includes a voltage detection circuit that monitors the power signal from the host system to detect anomalies. The voltage detection circuit responds to detection of a power signal

By asserting the busy signal, the voltage detection circuit substantially ensures that backup power provided by the charge pump (and by the battery and/or capacitive array, if provided) will be sufficient for the controller to complete all outstanding operations. The likelihood that data will be lost as the result of the power signal anomaly is therefore significantly reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Specific embodiments of the invention will now be described with reference to the following drawings, which are intended to illustrate and not limit the invention:

FIG. **1** illustrates the design of a non-volatile solid state memory subsystem according to one embodiment of the invention; and

FIG. **2** illustrates the design of a hard disk drive subsystem according to another embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** illustrates a solid state memory subsystem **30** according to one embodiment of the invention. The memory subsystem **30** may, for example, be a flash memory card that conforms to one of the aforementioned card specifications, although the invention is not so limited. The memory subsystem plugs into a slot of, or otherwise attaches to, a host system **32** (hereinafter "host"). The host may be any type of conventional system or device that accepts the memory subsystem, and need not include any special hardware or software for implementing the present invention.

The interface between the memory subsystem **30** and the host **32** includes the following conventional signal lines: a set of address/data/control lines **34** for transferring data; at least one power line **36** over which the host provides a power signal to the memory subsystem; and a ready/busy signal line **38** that is driven by the memory subsystem to notify the host of the subsystem's current status. In implementations in which the particular interface does not include an actual "ready/busy" signal, a different signal or combination of signals may be used to notify the host of the memory subsystem's ready/busy status.

As is conventional, the memory subsystem **30** includes a controller **40** that controls, an array of solid state, non-volatile memory **42**, which may be flash memory or another type of EEPROM memory. A conventional flash memory controller **40** may be used, as no special controller circuitry or functionality is needed in the illustrated embodiment. In accordance with the invention, the memory subsystem **30** also includes the following components to protect against anomalies in the power signal supplied by the host: a charge pump circuit **46**, a voltage detection circuit **48**, and a logic gate or switch **50**. The switch is shown for illustrative purposes as an OR gate, although other types of gates and switches may be used. The charge pump circuit **46** ("charge pump"), voltage detection circuit **48**, and switch **50** may be integrated within a single analog ASIC (application specific integrated circuit), possibly together with other components of the memory subsystem. As depicted by block **52** in the drawing, an optional battery or capacitive array may also be included to provide an additional level of protection against power anomalies.

As illustrated in FIG. **1**, the charge pump **46** receives the power signal V_{IN} from the host **32**, and supplies a regulated,

memory subsystem, such as a volatile memory used as a buffer (not shown). Preferably, the charge pump is designed such that the voltage V_{REG} supplied to the controller **40** is maintained at the ideal level (e.g., 5.4 volts) in the event of a brief interruption, drop, increase, or spike in the voltage V_{IN} supplied by the host **32**. In addition, the charge pump is preferably designed to protect against sustained voltage drops; for example, in one embodiment, the charge pump is capable of maintaining V_{REG} at 5.4 volts indefinitely as long as V_{IN} exceeds 0.7 volts. The charge pump **46** thus allows the memory subsystem **30** to continue to operate during certain types of power anomalies, including brief power interruptions, spikes and sustained voltage drops. In addition, the charge pump **46** protects the controller **40** from being damaged by spikes and surges in the power signal provided by the host.

The charge pump **46** preferably is or comprises a DC-to-DC step-up/step-down converter. Examples of commercially available charge pump devices that may be used include the ILC6363CIR50 and ILC6383CIRADJ from Fairchild and the MAX849, MAX1705 from Maxim. As is known in the art, the charge pump may optionally include or be followed by a low drop-out (LDO) voltage regulator (not shown) to provide greater output voltage stability. This LDO voltage regulator may be provided in-line between the charge pump's output and the controller's power input, downstream from the optional battery or capacitive array **52** if provided. One example of a voltage regulator device that may be used is a Seiko Epson S80827C.

The voltage detection circuit **48** is responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line **36**, and for driving the ready/busy signal to the "busy" state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit **48** may be designed to generate a "busy" signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts. The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected. To inhibit rapid transitions between the "ready" and "busy" states, the voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition.

The logic switch **50** logically combines (e.g., ORs) the ready/busy signals generated by the voltage detection circuit **48** and the controller **40** to generate the ready/busy signal provided to the host **32** on line **38**. Specifically, if a busy signal is generated by the voltage detection circuit **48**, the controller **40**, or both the voltage detection and the controller, a busy signal is provided to the host **32**. As is known in the art and defined by various interface specifications, the host will not perform new write operations to the memory subsystem when the "busy" state is asserted. Thus, the host **32** is prevented from performing write operations to the memory subsystem when voltage anomalies are detected and signaled by the voltage detection circuit **48**. As mentioned above, in implementations in which the particular host-subsystem interface does not include a "ready/busy" signal, the ready/busy status of the memory subsystem **30** may be communicated to the host using a different signal line or combination of signal lines.

The illustrated memory subsystem **30** responds to power signal anomalies generally as follows. Upon detecting the anomaly, the voltage detection circuit **48** generates a busy signal on line **36**, causing the host to refrain from writing or

continues to provide a near-constant voltage V_{REG} to the controller **40** (for at least a minimum time period T_{VREG}, as described below). Because new write operations are inhibited, and because the charge pump continues to provide a regulated power signal to the controller **40**, the possibility of data corruption (e.g., as the result of incomplete write operations) is significantly reduced. The charge pump also serves to protect the controller **40** and other circuitry from damage caused by voltage surges and spikes.

Even if the anomaly is in the form of a complete interruption or termination of power from the host **32**, the charge pump **46** continues to provide power to the controller **40** (and possibly to other active components, as mentioned above) for at least the minimum time period, T_{VREG}, needed to complete all outstanding operations. For example, if a write operation is in progress and the memory subsystem **30** has write data stored in its volatile RAM buffer (not shown), backup power will be provided for a time period sufficient for the controller **40** to finish writing this data to the EEPROM memory **42**, and if necessary, to back up any configuration data stored in volatile memory. The memory subsystem **30** may also use the backup power to perform a shut down sequence. The value of T_{VREG} needed to protect against data loss will typically be in the range of several milliseconds to several seconds, depending upon the design and type of the memory subsystem **30**.

As depicted by block **52** in FIG. **1**, a battery or a capacitive array may be connected between ground and the output of the charge pump **46** to extend the time duration for which backup power is provided. If a battery is used, the battery may be a small, rechargeable, watch-type battery that is embedded within the memory subsystem's housing. Typically, a battery of this type can provide several minutes of backup power to the controller **40**. If a capacitive array is provided, the capacitive array may consist of a bank or array of capacitors, and may provide tens to thousands of microfarads of capacitance. The battery or capacitive array, if provided, is connected so as to become or remain charged from the output of the charge pump **46**.

The protection circuitry illustrated in FIG. **1** is particularly useful for protecting against power interruptions caused by the removal or movement of the memory subsystem **30** by the user. The protection circuitry also protects against power anomalies emanating from or experienced by the host, and may therefore also find utility in memory subsystems that are not intended to be removed by the user.

FIG. **2** illustrates an embodiment in which the power anomaly protection circuitry is included within a hard disk drive subsystem **30**, such as an ATA, Serial ATA, SCSI, or Serial-Attached SCSI disk drive. In this embodiment, the controller **40** is a conventional disk drive controller that controls reads and writes of data to/from a rotating magnetic disk **60**. In the illustrated embodiment, the controller **40'** accesses a buffer or cache **62** formed from volatile solid state RAM. The design and operation of the power anomaly protection circuitry in this disk drive embodiment may be substantially the same as described with reference to FIG. **1**, except that the charge pump (and the optional battery or capacitive array **52**) also provide backup power to the spindle and actuator motors **64**, **66** of the disk drive **30'**.

The protection circuitry and methods of the present invention may also be incorporated into other types of storage subsystems, including volatile storage subsystems that store data within DRAM or SRAM.

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