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Amidi et al.

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(54) **CLOCK AND POWER FAULT DETECTION FOR MEMORY MODULES**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 702 days.

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GIIC 5/14 (2006.01)

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365/233.11; 711/115; 711/154

(58) **Field of Classification Search** 365/228,
365/229, 51, 52, 226, 233.1, 233.11; 711/105,
711/115, 154

See application file for complete search history.

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Primary Examiner—Dang T Nguyen

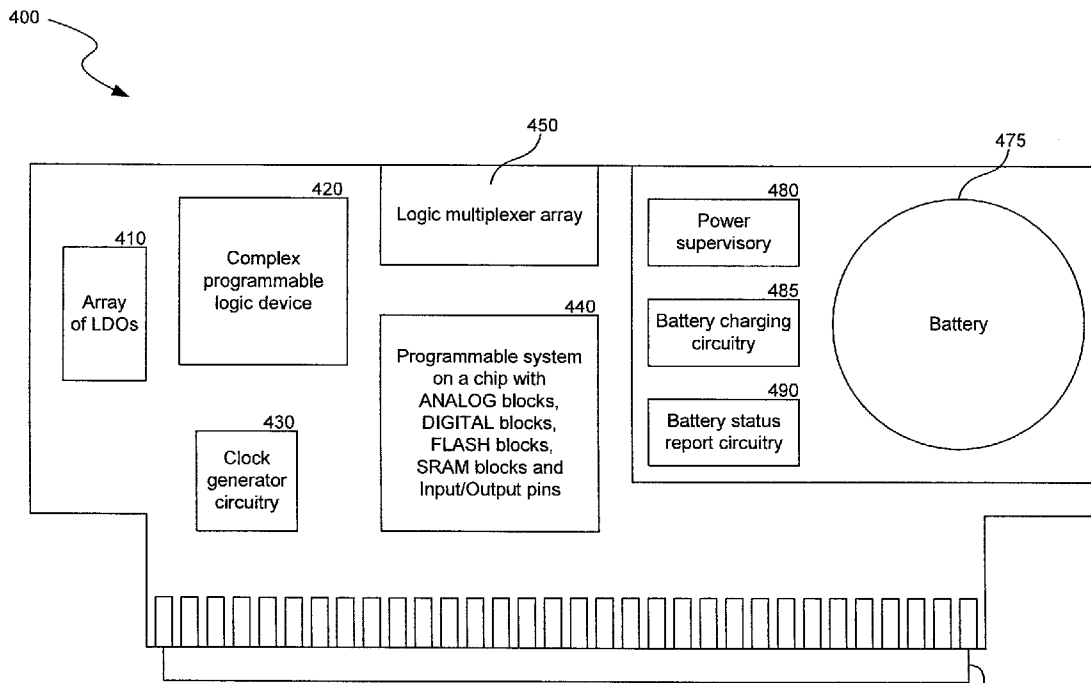
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(57) **ABSTRACT**

A system, method and apparatus for clock and power fault detection for a memory module is provided. In one embodiment, a system is provided. The system includes a voltage detection circuit and a clock detection circuit. The system further includes a controller coupled to the voltage detection circuit and the clock detection circuit. The system also includes a memory control state machine coupled to the controller. The system includes volatile memory coupled to the memory control state machine. The system further includes a battery and battery regulation circuitry coupled to the controller and the memory control state machine. The battery, battery regulation circuitry, volatile memory, memory control state machine, controller, clock detection circuit and voltage detection circuit are all collectively included in a unitary memory module.

22 Claims, 15 Drawing Sheets



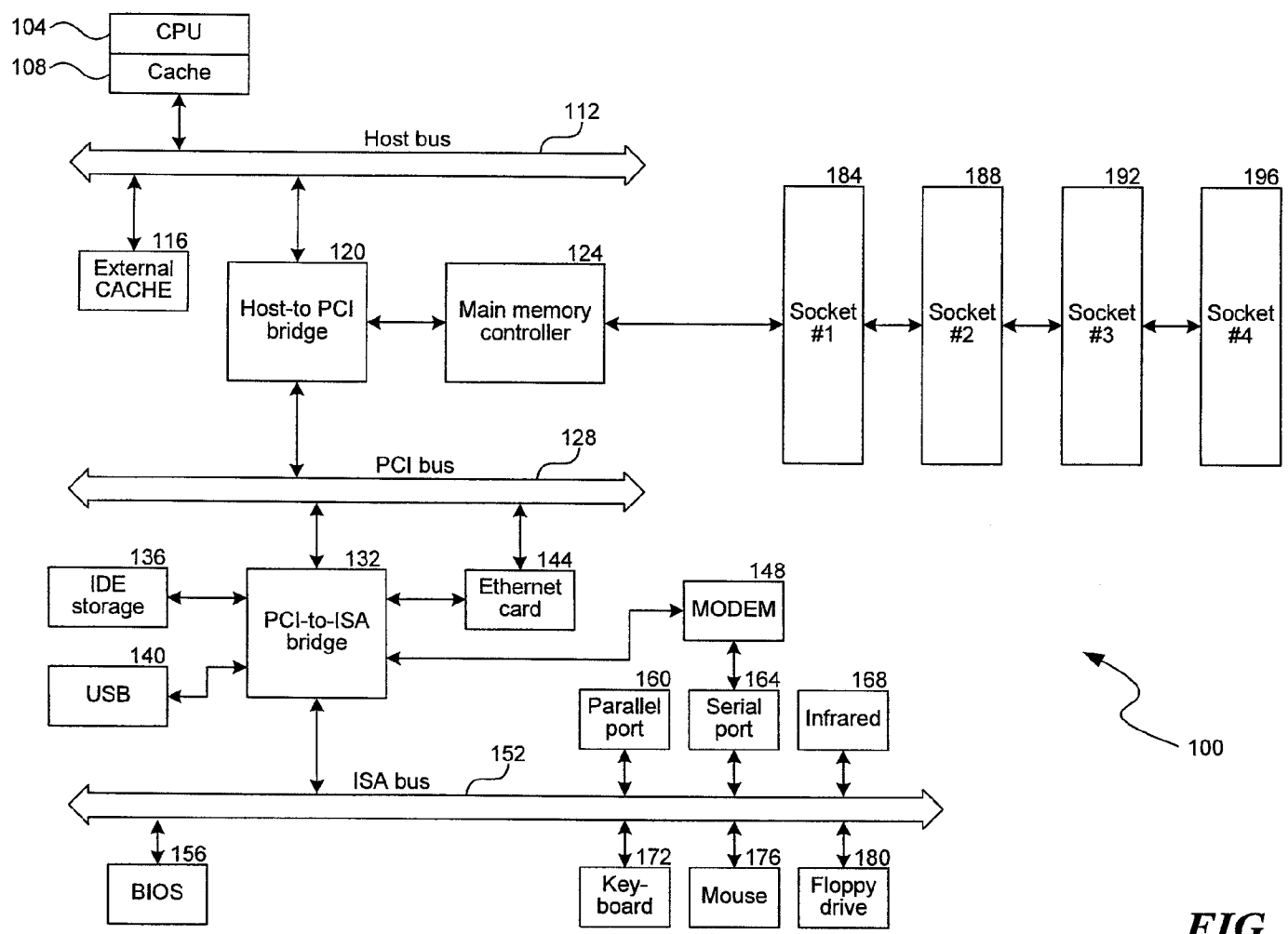


FIG. 1

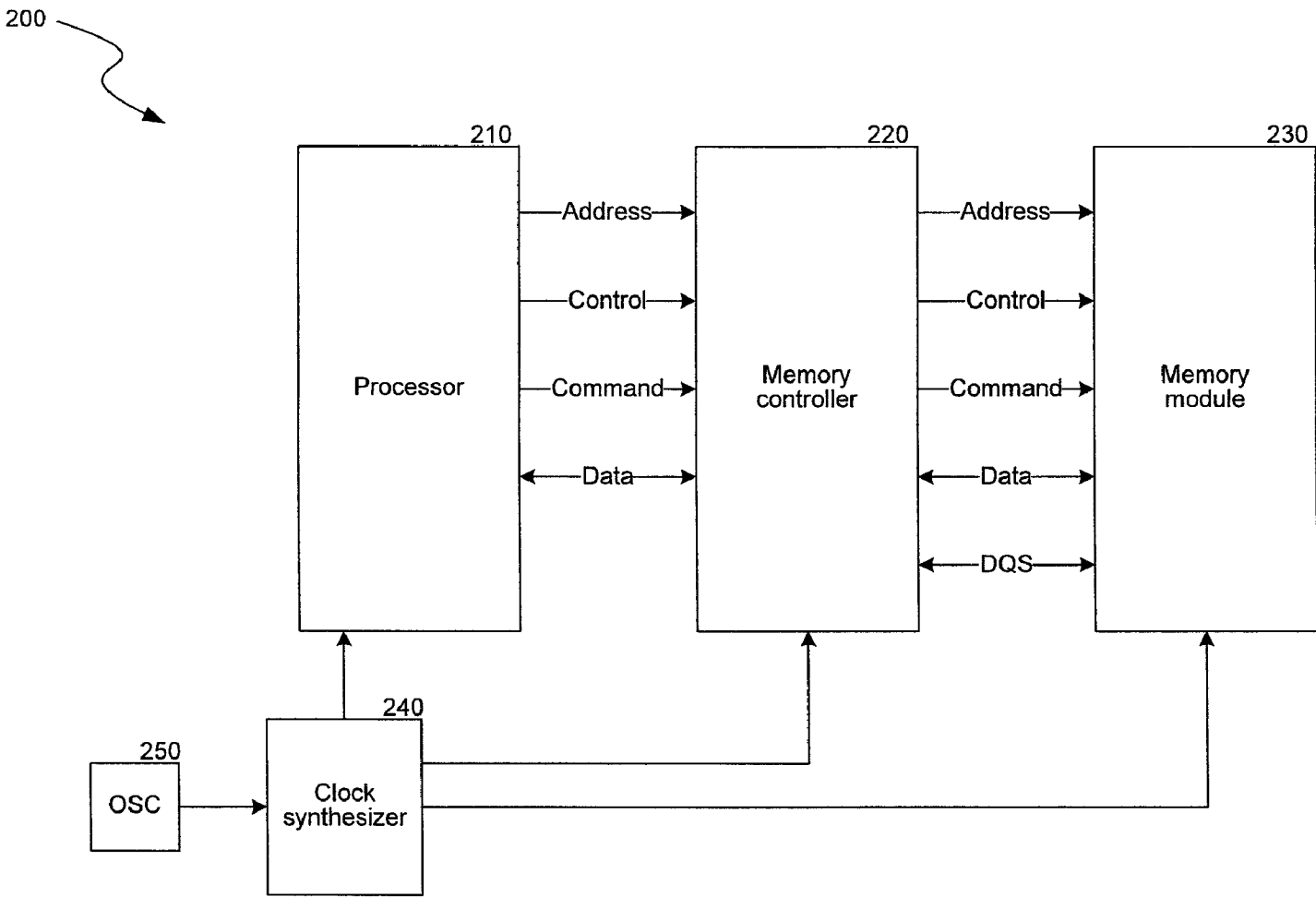


FIG. 2

300

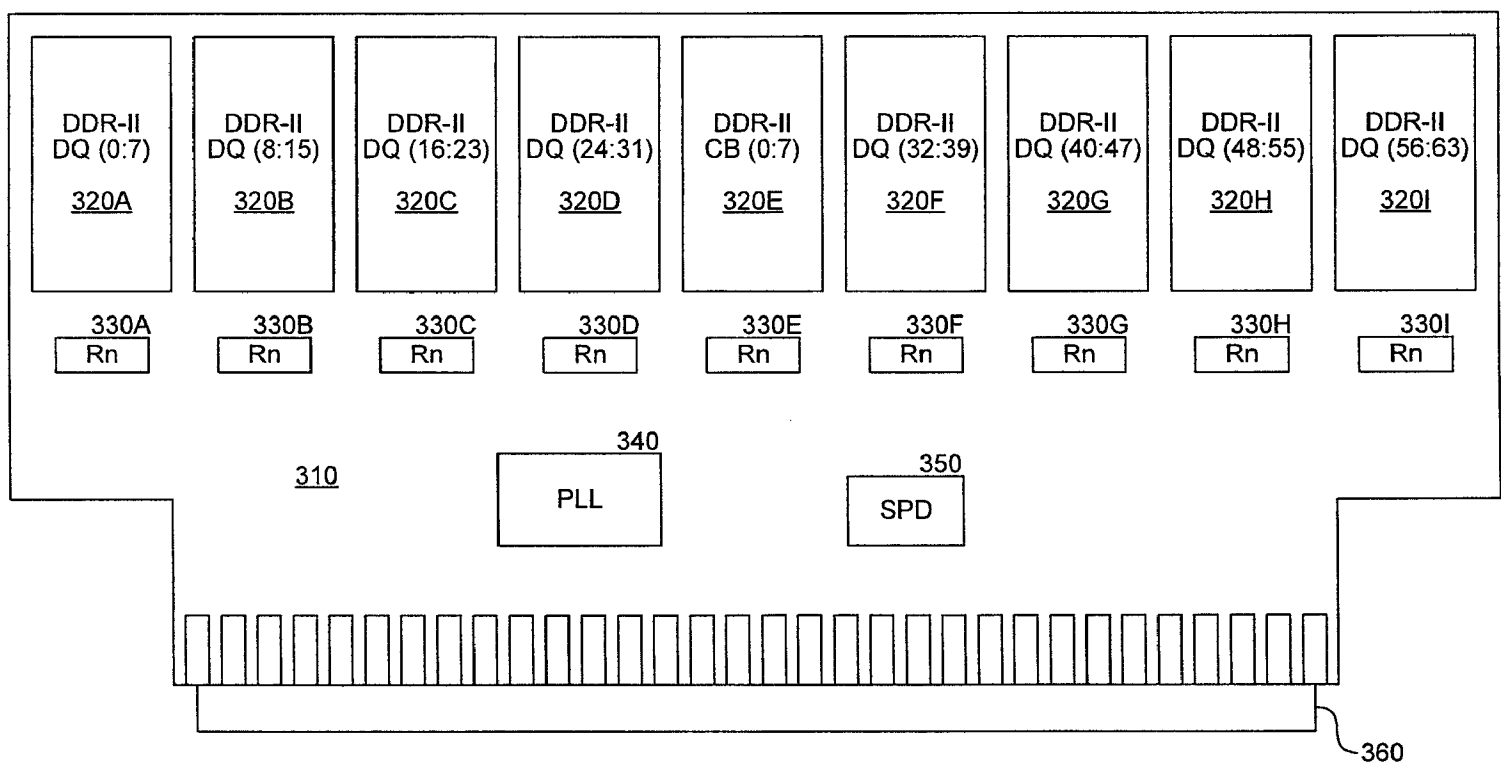


FIG. 3

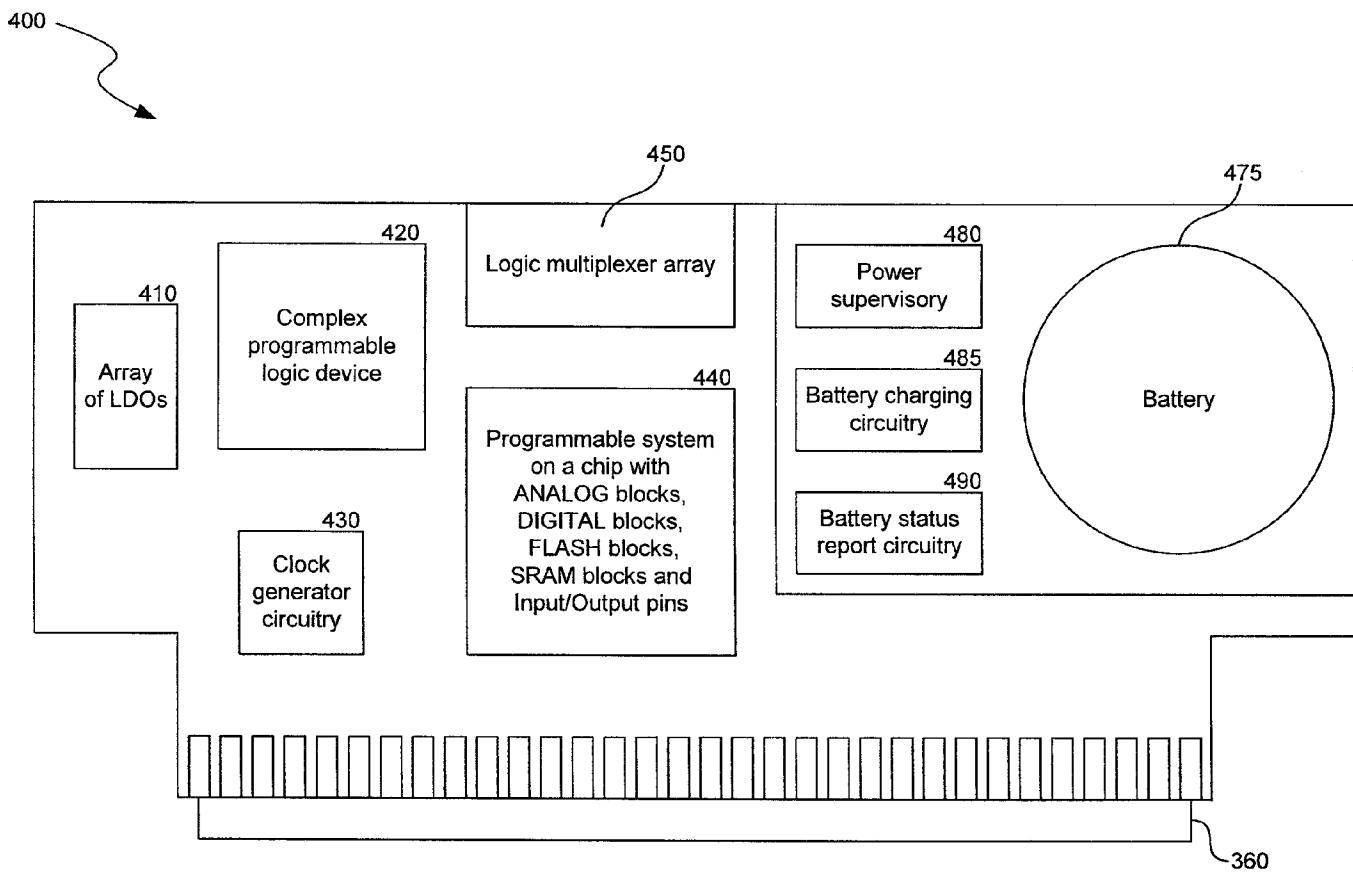


FIG. 4

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