UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

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IPR2023-00133
Patent 7,421,032 B2

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Before KEN B. BARRETT, JOHN A. HUDALLA, and
AMBER L. HAGY, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I.   INTRODUCTION

A. Background and Summary

Samsung Electronics Company, Ltd. ("Petitioner")[1] filed a Petition requesting *inter partes* review of U.S. Patent No. 7,421,032 B2 ("the '032 patent," Ex. 1001). Paper 1 ("Pet."). The Petition challenges the patentability of claims 1–8 and 10–22 of the '032 patent. California Institute of Technology ("Patent Owner")[2] filed a Preliminary Response to the Petition. Paper 7 ("Prelim. Resp."). With our authorization, Petitioner filed a Reply (Paper 8, "Pet. Reply") and Patent Owner filed a Sur-reply (Paper 9, "PO Sur-reply").

We have the authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2021). Under 35 U.S.C. § 314(a), an *inter partes* review may not be instituted "unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." Having considered the parties' submissions, and for the reasons explained below, we exercise our discretion under 35 U.S.C. § 314(a) to deny institution of *inter partes* review.

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[1] Petitioner identifies Samsung Electronics Co., Ltd. and Samsung Electronics America as the real parties-in-interest. Pet. 1.
[2] Patent Owner identifies California Institute of Technology as the real party-in-interest. Paper 5.

B. *Related Proceedings*

Both parties identify, as matters involving or related to the '032

patent, the following:

- *California Institute of Technology v. Samsung Electronics Co., Ltd.*,
  No. 2-21-cv-00446 (E.D. Tex.) ("the underlying litigation")
- *California Institute of Technology v. Microsoft Corp.*, No. 6-21-cv-
  00276 (W.D. Tex.);
- *California Institute of Technology v. HP Inc. f/k/a/ Hewlett-Packard
  Co.*, No. 6-20-cv-01041 (W.D. Tex.);
- *California Institute of Technology v. Dell Technologies Inc.*, No. 6-
  20-cv-01042 (W.D. Tex.);
- *California Institute of Technology v. Broadcom Ltd.*, No. 2-16-cv-
  03714 (C.D. Cal.), *aff'd, vacated, and remanded*, 25 F.4th 976 (Fed.
  Cir. 2022);
- *California Institute of Technology v. Hughes Communications, Inc.*,
  No. 2-15-cv-01108 (C.D. Cal.); and
- *California Institute of Technology v. Hughes Communications, Inc.*,
  No. 2-13-cv-07245 (C.D. Cal.).

Pet. 1–2; Paper 5; *see* Pet. 7–8 (citing, in the claim construction section, the

Federal Circuit's decision in *California Institute of Technology v. Broadcom

Ltd.*); Prelim. Resp. 3–5 (same).

The '032 patent was previously the subject of the following four *inter

partes* reviews identified by the parties (Pet. 1–2; Paper 5, 2–3):

IPR2015-00060 ("060 IPR"), IPR2017-00700 ("700 IPR"), IPR2017-00701

("701 IPR"), and IPR2017-00728 ("728 IPR"). In the 060 IPR, institution

was denied on the merits concerning challenges to claims 1, 8, 10, 18, 19,

and 22 of the '032 patent as allegedly being obvious over various combinations of references known as "Frey," "Divsalar," "Luby," "Hall," and "Kschischang." In the Final Written Decisions in the 700 IPR, the 701 IPR, and the 728 IPR, the Board determined that claims 11, 12, and 14–16 of the '023 patent were *not* shown to be unpatentable over "Ping," "MacKay," and "Divsalar," and claims 1, 4–10, 13, and 18–23, were *not* shown to be unpatentable over "Ping," "MacKay," "Divsalar," and "Luby97." None of those references are at issue in this proceeding.

Patent Owner additionally identifies the following co-pending *inter partes* review proceedings: *Samsung Electronics Co., Ltd. v. California Institute of Technology*, IPR2023-00130; *Samsung Electronics Co., Ltd. v. California Institute of Technology*, IPR2023-00131; *Samsung Electronics Co., Ltd. v. California Institute of Technology*, IPR2023-00137. Paper 5, 2–3. Patent Owner also identifies several other Patent Trial and Appeal Board cases as related matters. *Id.*

C. The '032 Patent

The '032 patent is titled "Serial Concatenation of Interleaved Convolutional Codes Forming Turbo-Like Codes." Ex. 1001, [54]. The '032 patent explains some of the prior art with reference to its Figure 1, reproduced below.
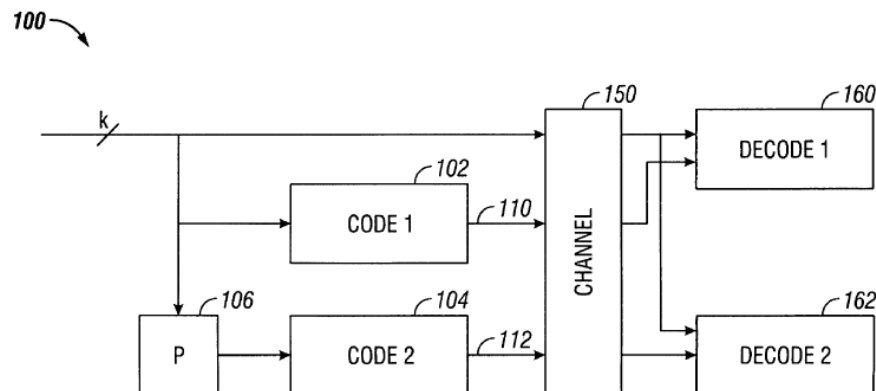
Figure 1 is a schematic diagram of a prior "turbo code" system. *Id.* at 2:16–

17. The '032 patent specification describes Figure 1 as follows:

> A block of k information bits is input directly to a first coder
> 102. A k bit interleaver 106 also receives the k bits and
> interleaves them prior to applying them to a second coder 104.
> The second coder produces an output that has more bits than its
> input, that is, it is a coder with rate that is less than 1. The
> coders 102, 104 are typically recursive convolutional coders.
>   Three different items are sent over the channel 150: the
> original k bits, first encoded bits 110, and second encoded
> bits 112. At the decoding end, two decoders are used: a first
> constituent decoder 160 and a second constituent decoder 162.
> Each receives both the original k bits, and one of the encoded
> portions 110, 112. Each decoder sends likelihood estimates of
> the decoded bits to the other decoders. The estimates are used
> to decode the uncoded information bits as corrupted by the
> noisy channel.

Id. at 1:41–56.

A coder 200, according to a first embodiment of the invention, is

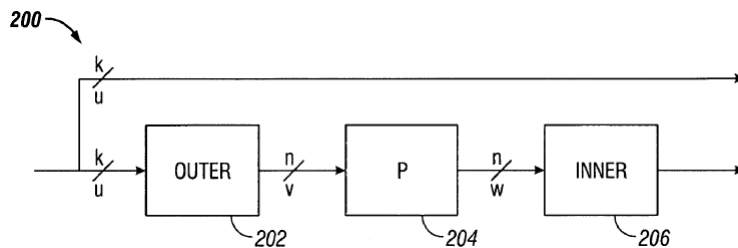described with reference to Figure 2, reproduced below.

Figure 2 of the '032 patent is a schematic diagram of coder 200.

> The coder 200 may include an outer coder 202, an interleaver
> 204, and inner coder 206. . . . The outer coder 202 receives the
> uncoded data. The data may be partitioned into blocks of fixed
> size, say k bits. The outer coder may be an (n,k) binary linear
> block coder, where n>k. The coder accepts as input a block u
> of k data bits and produces an output block v of n data bits.

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