Paper 10 Date: May 4, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY, Patent Owner.

IPR2023-00130 Patent 7,116,710 B1

Before KEN B. BARRETT, JOHN A. HUDALLA, and AMBER L. HAGY, *Administrative Patent Judges*.

HAGY, Administrative Patent Judge.

DECISION
Denying Institution of *Inter Partes* Review 35 U.S.C. § 314



I. INTRODUCTION

A. Background and Summary

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition requesting *inter partes* review of claims 11–17 and 19–33 of U.S. Patent No. 7,116,710 B1 ("the '710 patent," Ex. 1001). Paper 1 ("Pet."). California Institute of Technology ("Patent Owner") filed a preliminary response to the Petition. Paper 7 ("Prelim. Resp."). With our authorization, Petitioner filed a Preliminary Reply (Paper 8, "Pet. Reply") and Patent Owner filed a Preliminary Sur-reply (Paper 9, "PO Sur-reply") directed to the issue of discretionary denial under 35 U.S.C. § 314.

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2016); 37 C.F.R. § 42.4(a) (2019). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an inter partes review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons explained below, we decline to institute an *inter partes* review of the '710 patent.

B. Real Parties in Interest

The parties each identify themselves as the real parties in interest. Pet. 1; Paper 5, 1.

C. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify the following related matters (Pet. 1–2; Paper 5, 1–2):

Cal. Inst. of Tech. v. Samsung Elecs. Co., No. 2-21-cv-00446 (E.D. Tex. filed Dec. 3, 2021) ("the Underlying Litigation");



Cal. Inst. of Tech. v. Microsoft Corp., No. 6-21-cv-00276 (W.D. Tex. filed Mar. 19, 2021);

Cal. Inst. of Tech. v. HP Inc. f/k/a/ Hewlett-Packard Co., No. 6-20-cv-01041 (W.D. Tex. filed Nov. 11, 2020);

Cal. Inst. of Tech. v. Dell Techs. Inc., No. 6-20-cv-01042 (W.D. Tex. filed Nov. 11, 2020);

Cal. Inst. of Tech. v. Broadcom Ltd., No. 2:16-cv-03714 (C.D. Cal. filed May 26, 2016);

Cal. Inst. of Tech. v. Hughes Commc'ns, Inc., No. 2:15-ev-01108 (C.D. Cal. filed Feb. 17, 2015); and

Cal. Inst. of Tech. v. Hughes Commc'ns, Inc., 2:13-cv-07245 (C.D. Cal. filed Oct. 1, 2013).

The '710 patent was previously the subject of five *inter partes* reviews identified by the parties (Pet. 2; Paper 5, 2–3): IPR2015-00067 ("067 IPR"), IPR2017-00068 ("068 IPR"), IPR2017-00210 ("210 IPR"), IPR2017-00211 ("211 IPR"), and IPR2017-00219 ("219 IPR"). In the Final Written Decisions from the 210 and 219 IPRs, the Board determined that claims 1–8, 10–17, and 19–33 of the '710 patent were not shown to be unpatentable over "Frey," "Divsalar," and "Luby" (for the 210 IPR) and "Divsalar," "Luby," and "Luby97" (for the 219 IPR). None of those references are at issue in this proceeding.

Patent Owner also identifies the following prior *inter partes* review proceedings for patents related to the '710 patent (Paper 5, 2–3): IPR2015-00059, IPR2015-00060, IPR2015-00061, IPR2015-00067, IPR2015-00068, IPR2015-00081, IPR2017-00297, IPR2017-00423,



IPR2017-00700, IPR2017-00701, IPR2017-00702, IPR2017-00703, and IPR2017-00728.

We additionally identify the following co-pending *inter partes* review proceedings between the parties: IPR2023-00131, IPR2023-00133, and IPR2023-00137.

D. The '710 Patent

The '710 patent describes the serial concatenation of interleaved convolutional codes forming turbo-like codes. Ex. 1001, code (54). It explains some of the prior art with reference to its Fig. 1, reproduced below.

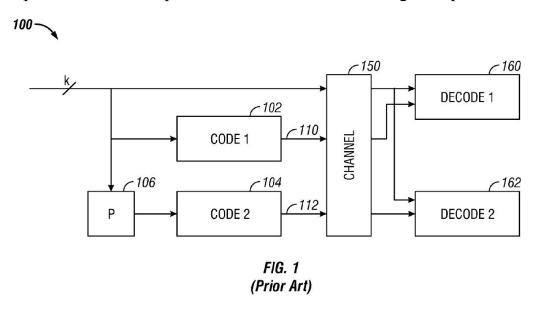


Figure 1 is a schematic diagram of a prior "turbo code" system. *Id.* at 2:14–15. The '710 patent specification describes Figure 1 as follows:

A standard turbo coder 100 is shown in FIG. 1. A block of k information bits is input directly to a first coder 102. A k bit interleaver 106 also receives the k bits and interleaves them prior to applying them to a second coder 104. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders 102,104 are typically recursive convolutional coders.



Three different items are sent over the channel 150: the original k bits, first encoded bits 110, and second encoded bits 112. At the decoding end, two decoders are used: a first constituent decoder 160 and a second constituent decoder 162. Each receives both the original k bits, and one of the encoded portions 110, 112. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

Id. at 1:38–53 (emphasis omitted).

A coder 200, according to a first embodiment of the invention, is described with respect to Figure 2, reproduced below.

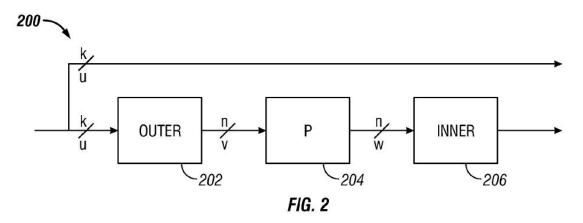


Figure 2 of the '710 patent is a schematic diagram of coder 200. *Id.* at 2:16–17.

The specification states that "coder 200 may include an outer coder 202, an interleaver 204, and inner coder 206." *Id.* at 2:34–35. It further states as follows:

The outer coder 202 receives uncoded data. The data may be partitioned into blocks of fixed size, say k bits. The outer coder may be an (n,k) binary linear block coder, where n>k. The coder accepts as input a block u of k data bits and produces an output block v of n data bits. The mathematical relationship



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