Paper No. ___
Filed: February 10, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

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Case No. IPR2023-00130
Patent No. 7,116,710

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**PATENT OWNER'S PRELIMINARY RESPONSE PURSUANT TO 37 C.F.R. § 42.107**

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## I. INTRODUCTION

This is the sixth IPR petition challenging the claims of U.S. Patent No. 7,116,710 ("the '710 patent"). Despite five prior petitions[1] and two instituted trials, the Board has never found a single claim of the '710 patent unpatentable.[2] The present petition does not warrant a different outcome.

Petitioner Samsung Electronics Co., Ltd. advances a challenge premised on anticipation by Kobayashi, yet various aspects of the challenged claims are simply missing from Kobayashi. Rather than meeting its burden to show that Kobayashi discloses each limitation, Petitioner seeks to avoid the claims' requirements by misreading limitations or simply assuming that Kobayashi meets the claims despite its silence on the issue. For example, each independent claim includes a limitation directed to irregular repetition—expressed either as repeating received bits "a different number of times," as recited in claim 11, or simply as "repeat[ing] said stream of bits irregularly," as recited in claims 15 and 25. Kobayashi does not disclose irregular repetition as recited, and Petitioner fails to show that it is

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[1] IPR2017-00210; IPR2017-00211; IPR2017-00219; IPR2015-00067; IPR2015-00068.

[2] The Federal Circuit summarily affirmed the final written decisions upholding all claims. *Apple Inc. v. Cal. Inst. of Tech.*, 796 F. App'x 743 (Fed. Cir. 2020).

inherent. In fact, Petitioner actually provides examples of encoding techniques that undermine the logic on which Petitioner grounds its inherency argument.

The petition is similarly deficient with respect to other limitations. Independent claim 11 recites that a first encoded data block is formed by repeating bits of a received data block different numbers of times. Yet what Petitioner identifies in Kobayashi for this element is not a block formed by irregularly repeating bits, but a block consisting of one copy of each original bit plus parity bits that are not repeated bits at all. As for independent claims 15 and 25, each requires scrambling of irregularly repeated bits, yet Kobayashi never scrambles irregularly repeated bits. Petitioner points instead to an interleaving of a single copy of each original bit with a group of parity bits, not to a scrambling of a collection of irregularly repeated bits.

In addition to these deficiencies, Petitioner's late filing of this petition warrants discretionary denial in light of the co-pending litigation in the Eastern District of Texas in which Petitioner is a defendant. Petitioner filed the present case less than a year before the scheduled trial. Under even generous estimates, the district court trial will be completed many months before a final written decision would be due in this case. Given the substantial costs that will arise due to duplication of efforts, Petitioner's unexplained and unexcused delay, and the weak merits of the petition's grounds, the Board should not institute trial.

Accordingly, institution of *inter partes* review of claims 11-17 and 19-33 of U.S. Patent No. 7,116,710 ("the '710 patent") should be denied.

## II. CLAIM CONSTRUCTION

In an *inter partes* review, a claim is given its ordinary and customary meaning in light of the specification. 37 C.F.R. §42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). Petitioner asserts that the term "repeat" should be construed to mean "generation of additional bits, where generation can include, for example, duplication or reuse of bits," in accordance with a district court construction affirmed by the Federal Circuit. Pet., 8 (citing *Cal. Inst. of Tech. v. Broadcom Ltd.*, 25 F.4th 976, 986 (Fed. Cir. 2022) ("*Broadcom* litigation")).

However, Petitioner extends this construction in an unreasonable way and mischaracterizes the Federal Circuit's construction. Petitioner first asserts that (1) the Federal Circuit held that "passing an input information bit through an AND gate when the other input is a '1' bit comprises 'repeating' the information bit"; (2) "[m]ultiplying a binary information bit by a "1" bit is equivalent to passing the information bit through an AND gate with a '1' bit", and (3) therefore, "multiplying an information bit by a "1" bit comprises 'repeating' the information bit." Pet., 14-15. The Federal Circuit never said this—its claim construction never discussed either multiplication or AND gates. *See Broadcom*, 25 F.4th at 986.

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