Paper 11 Date: May 11, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD
LG ELECTRONICS INC. and LG ELECTRONICS USA, INC., Petitioner,
v.
IMAGE PROCESSING TECHNOLOGIES, LLC, Patent Owner.
IPR2023-00104 Patent 6,959,293 B2

Before MICHAEL R. ZECHER, BARBARA A. BENOIT, and IFTIKHAR AHMED, *Administrative Patent Judges*.

BENOIT, Administrative Patent Judge.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

### I. INTRODUCTION

LG Electronics Inc. and LG Electronics USA, Inc. (collectively, "Petitioner") filed a Petition (Paper 1, "Pet.") requesting institution of *inter partes* review of claim 1 ("the challenged claim") of U.S. Patent No. 6,959,293 B2 (Ex. 1001, "the 293 patent"). Image Processing Technologies, LLC ("Patent Owner") filed a Preliminary Response (Paper 6, "Prelim. Resp."). With prior authorization (Paper 7), Petitioner filed a Preliminary Reply (Paper 8, "Reply"), limited to addressing Patent Owner's arguments for discretionary denial under 35 U.S.C. §§ 314(a) and 325(d), and Patent Owner filed a Preliminary Sur-reply on these issues (Paper 9, "Sur-reply").

After considering the Petition, Preliminary Response, Preliminary Reply, and Preliminary Sur-reply, we exercise our discretion under 35 U.S.C. § 325(d) and do not institute *inter partes* review for the reasons explained below.

### A. Real Parties in Interest

The Petition identifies LG Electronics Inc. and LG Electronics USA, Inc. as real parties in interest. Pet. 1. Patent Owner identifies only itself as real party in interest. Paper 3 (Patent Owner's Mandatory Notices), 1.

## B. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), each party identifies various judicial or administrative matters that would affect or be affected by a decision in this proceeding. Pet. 1–2; Paper 3, 1–2.

The parties identify the following district court cases: *Image Processing Technologies, LLC v. Samsung Electronics Co.*, No. 2:20-cv-00050 (E.D. Tex.), *Image Processing Technologies, LLC v. Samsung Electronics Co.*, No. 2:16-cv-00505 (E.D. Tex.), and *Image Processing* 



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*Technologies, LLC v. Canon Inc.*, No. 2:10-cv-03867 (E.D.N.Y.). Pet. 1–2; Paper 3, 1–2. Patent Owner additionally indicates that the '293 patent is involved in *Image Processing Technologies, LLC v. LG Electronics Inc.*, No. 2:22-cv-00077 (E.D. Tex.). Paper 3, 1.

The parties also each indicate that the sole claim challenged here was involved in three prior Board proceedings. Pet. 1–2; Paper 3, 1–2. Two inter partes proceedings were brought by a different petitioner—Samsung Electronics Co. v. Image Processing Technologies, LLC, IPR2017-00336 ("IPR 336") and Samsung Electronics Co. v. Image Processing Technologies, LLC, IPR2017-01189 ("IPR 1189"). In a final written decision issued May 9, 2018 in IPR 336, the Board determined that the petitioner had not demonstrated that claim 1 was unpatentable, among other determinations. Ex. 1005, 43–54, 76. In a decision denying institution issued August 18, 2017 in IPR 1189, the Board determined that the petitioner did not demonstrate a reasonable likelihood of succeeding with regard to claim 2 (which depends directly from claim 1) or any other challenged claim. Ex. 1006, 27. Additionally, the Board reversed the Examiner's rejection that claim 1 was unpatentable in Ex Parte Image Processing Technologies, LLC, Reexamination Control No. 90/014,056 ("Reexam 056"). Ex. 1007, 22;1 Ex. 2001 (reexamination certificate issued January 27, 2020 confirming patentability of claim 1).

<sup>&</sup>lt;sup>1</sup> All citations to the Board's Reexamination Decision refer to the page number inserted by Petitioner in the bottom, right-hand corner of each page of Exhibit 1007.



## C. The '293 Patent

The '293 patent describes a visual perception device, including a device for processing image signals using histogram calculation units. Ex. 1001, 1:6–10. Figure 3 of the '293 patent illustrates a histogram calculation unit, and is reproduced below with highlighting added by Petitioner (Pet. 5). Ex. 1001, 4:45–46.

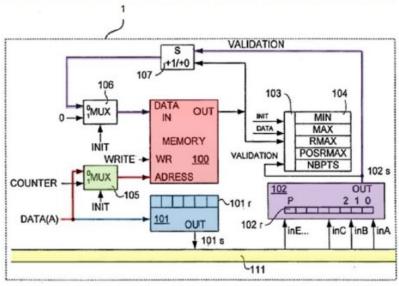


FIG. 3

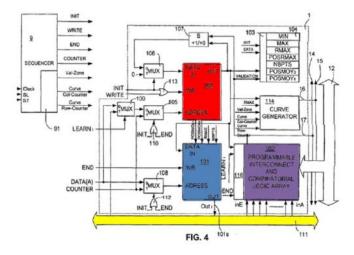
As shown in highlighted Figure 3 above, histogram calculation unit 1 includes analysis memory 100 (in red), address multiplexer 105 (in green), data input multiplexer 106, incrementation unit 107, classifier 101 (in blue), time coincidences unit 102 (in purple), and test unit 103, which is connected to analysis output registers 104. Ex. 1001, 8:37–43, 9:51–54. Output of classifier 101 (in blue) is connected to bus 111 (in yellow). *Id.* at 9:36.

Analysis output registers 104 receive and store statistical information prepared on the basis of the values of parameter A of signal DATA(A) for each frame. *Id.* at 9:51–57. In particular, after processing a complete frame, statistical information representative of this frame is produced and stored in analysis output registers 104. *Id.* at 10:1–14. This statistical information



includes minimum values (MIN) and maximum values (MAX) of the histogram, the number of points (NBPTS) of the histogram, the position (POSRMAX) of the maximum of the histogram, and the number of points (RMAX) at the maximum of the histogram. *Id.* These features are determined in parallel with the formation of the histogram by test unit 103.

Figure 4 of the '293 patent illustrates a self-adapting histogram calculation unit with anticipation and learning functionalities, and is reproduced below with highlighting added by Patent Owner (Prelim. Resp. 10). Ex. 1001, 4:47–49.



According to the '293 patent, in the self-adapting embodiment illustrated in Figure 4, the content of the memory of classifier 101 (in blue) is updated automatically. Ex. 1001, 11:14–29. To implement the self-adapting function (i.e., real-time updating of classifier 101), classifier 101 has an addressable memory whose writing is controlled by signal END, which is generated by sequencer 9. *Id.* Histogram calculation unit 1 also includes selection circuit 110 (e.g., an "OR" gate), receiving as its input signals INIT and END and whose output is connected to the selection input of address multiplexer 105. *Id.* 



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