



[54] STACKED DEVICES FOR MULTICHIP MODULES

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[75] Inventors: David B. Tuckerman, Dublin; Nicholas E. Brathwaite, Hayward; Paul Marella, Palo Alto; Kirk Flatow, San Jose, all of Calif.

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[73] Assignee: nChip, Inc., San Jose, Calif.

[21] Appl. No.: 655,338

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[22] Filed: May 24, 1996

Related U.S. Application Data

- A. Barfknecht et al., "Multichip Packaging Technology With Laser-Patterned Interconnects", IEEE Trans. Components, Hybrids, and Manufacturing Technology, vol. 12, No. 4, (1989), pp. 646-649.
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[62] Division of Ser. No. 300,575, Sep. 2, 1994, which is a continuation of Ser. No. 881,452, May 11, 1992, abandoned.

[51] Int. Cl.6 H05K 3/32

[52] U.S. Cl. 156/60; 29/831; 29/850; 156/300

[58] Field of Search 156/150, 151, 156/182, 288, 295, 300, 313, 299, 60; 29/829, 830, 831, 842, 844, 850, 876, 877

(List continued on next page.)

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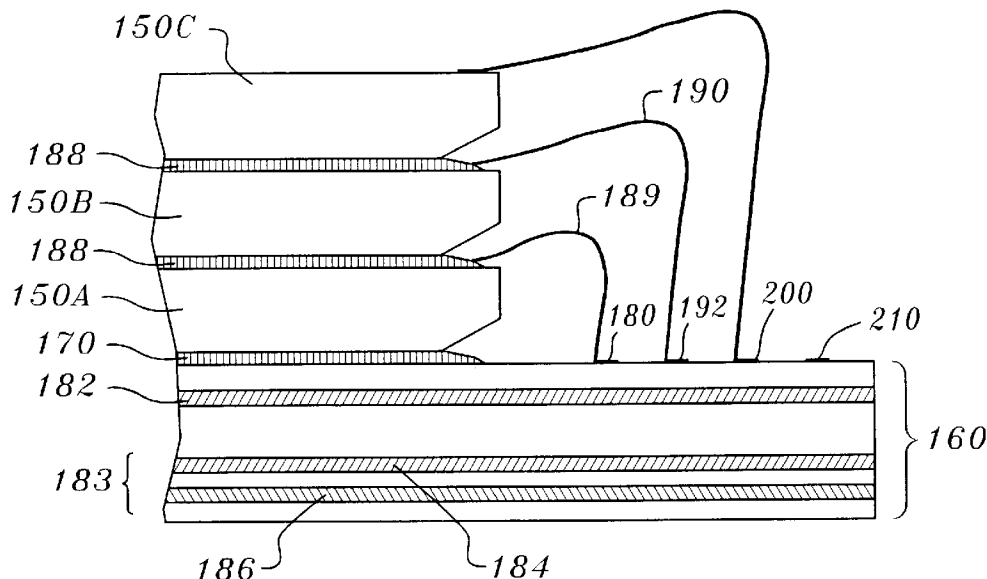
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[57] ABSTRACT

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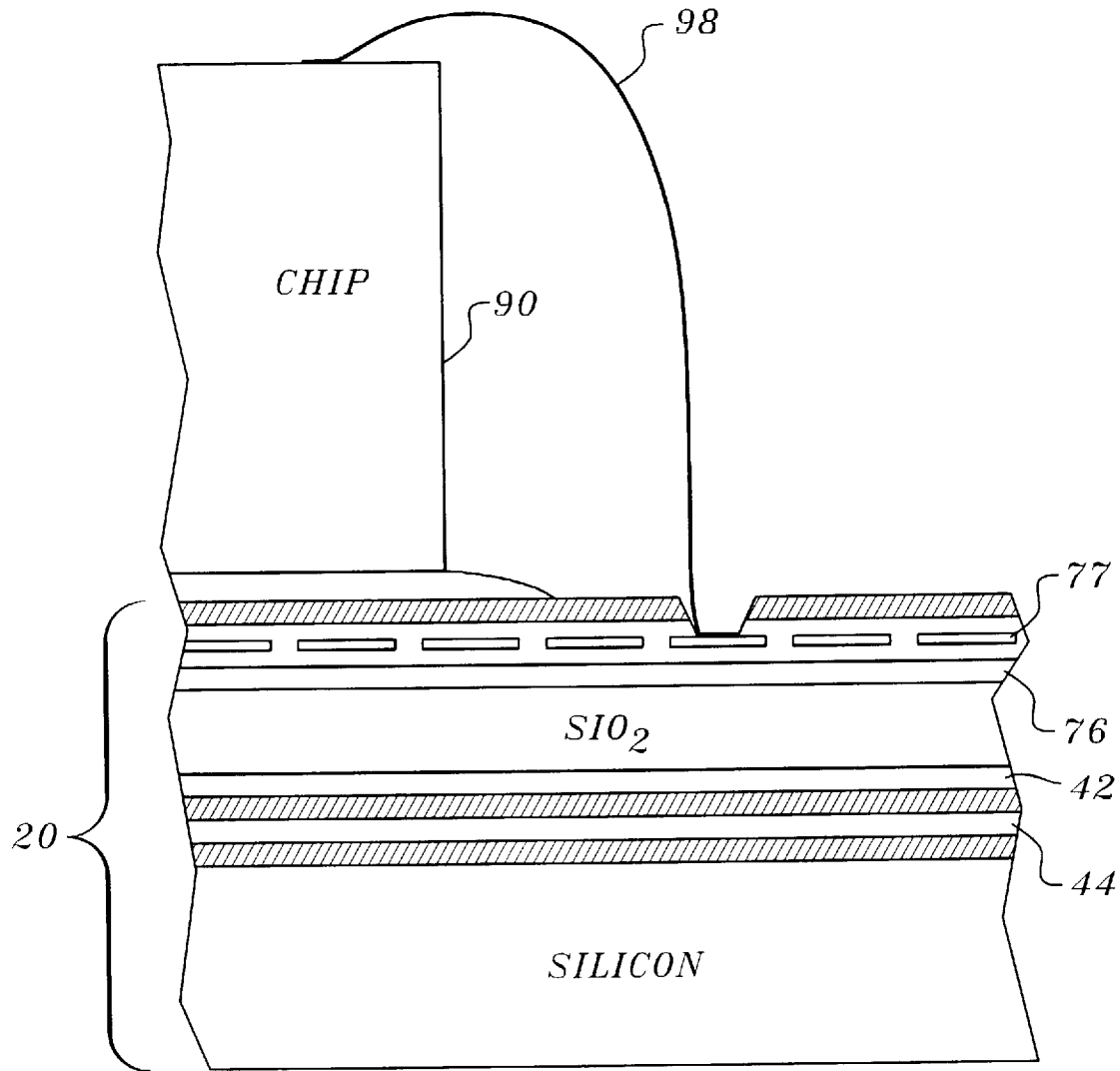
A method for fabricating a multichip module includes attaching a first integrated circuit to a silicon circuit board. Bonding pads on the first integrated circuit are wire-bonded to a first set of contacts on the circuit board. A second integrated circuit is adhesively attached onto the top of the first integrated circuit. The second integrated circuit includes a recessed bottom surface to provide an overhang over the first integrated circuit which exposes the bonding pads on the top surface of the first integrated circuit. Then bonding pads on the second integrated circuit are wire-bonded to a second set of contacts on the circuit board.

18 Claims, 8 Drawing Sheets



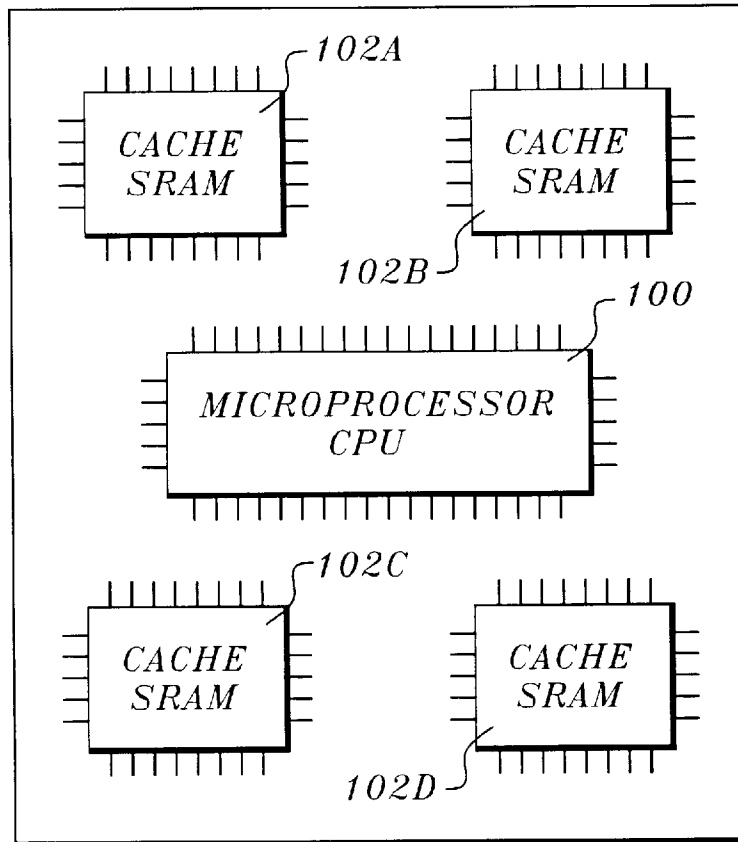
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*(PRIOR ART)*

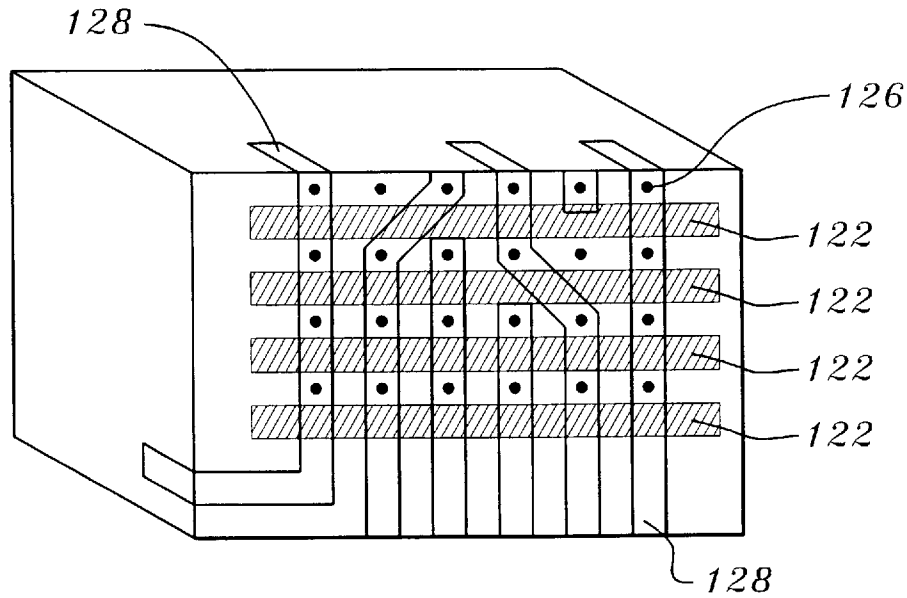
*FIG. 1.*



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*(PRIOR ART)*

*FIG. 2.*



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*(PRIOR ART)*

*FIG. 3.*

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