A CUSTOMIZABLE DSP FOR DMT–BASED ADSL MODEM

L. Kiss, E. Hanssens, K. Adriaensen, M. Huysmans, C. Gendarme,
F. Van Beylen, H. Van De Weghe

Alcatel Antwerp (Microelectronics department)
Fr. Wellesplein 1
2018 Antwerp (Belgium)
(32)32407807
hanssene@sh.bel.alcatel.be

Abstract

From Time domain to Atm domain, the complete digital signal processing required by ADSL technology has been integrated onto a single device called SACHEM. High programmability along with flexible architecture enable the device to serve for both network and line termination. Mapping on a 0.35 um standard digital CMOS technology makes SACHEM a cost effective solution as well as a low power device, consuming only 800 mW at 3.3 V.

I. Introduction

The most important feature of ADSL is that it can provide high speed digital services on existing pair copper wire, in overlay and without interfering with the traditional analogue telephone service (plain old telephone system: POTS) see Fig. 1. ADSL can offer,

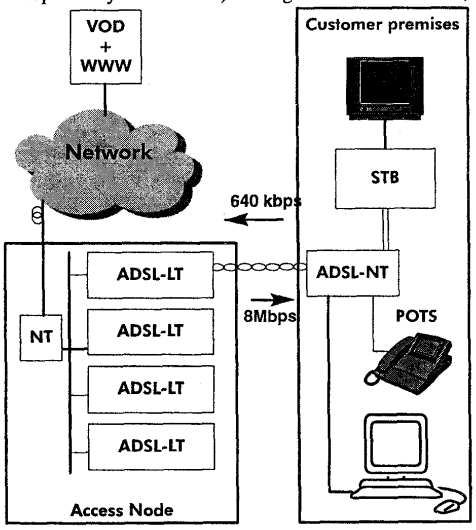

Fig. 1: ADSL network.

due to its highly efficient line coding technique, new services like high speed Internet and On–line Access, telecommuting and VOD to every residential telephone subscriber. The technology is largely independent of twisted pair characteristics, thereby enabling it to be applied universally, virtually regardless of the actual parameters of the local loop.

The modulation technique for ADSL, which has been standardized in TI.413 [1], is Discrete Multi–Tone (DMT), a special form of multicarrier modulation [2][3]. Fundamentally, DMT modulation superimposes several carrier–modulated waveforms to represent the input bit stream. The DMT transmit signal, see Fig. 2, is the sum of N independent sub–sig-

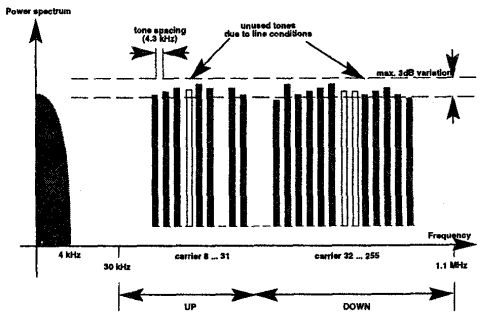

Fig. 2: DMT frequency division.

nals, each of equal bandwidth and equispaced with center frequency f_i, i=1, ... , N. Each sub–channel can be considered as a Quadrature Amplitude Modulated (QAM) signal. In a DMT modulation scheme, the number input data bits allocated on distinct sub–channels is variable. Obviously, sub–channels that encounter less attenuation and less noise will carry more bits of information.

The chip we propose reaches the highest integration level. The complete digital signal processing for ADSL DMT–based modem functionality and transport convergence functions such as (de)interleaving, Reed–Solomon (de)coding, (de)scrambling and

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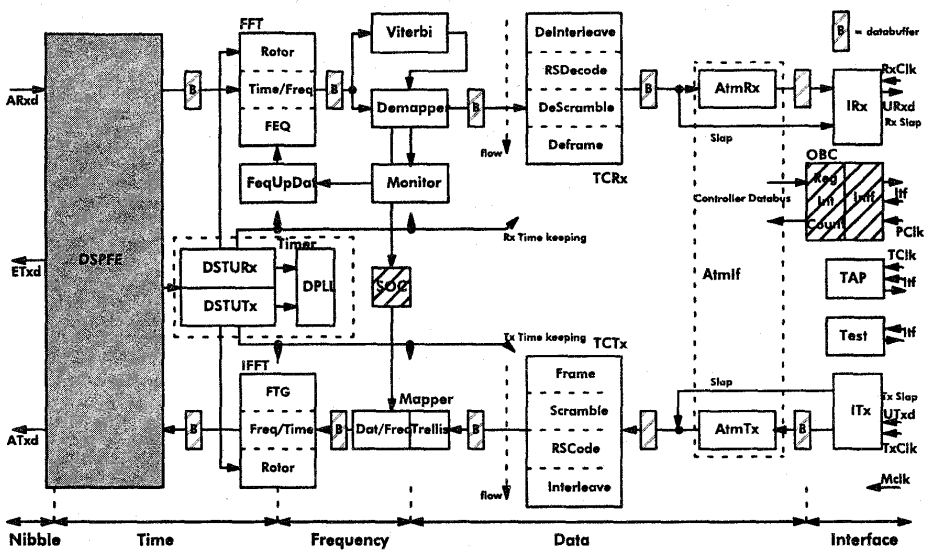

Fig. 3: SACHEM architecture.

(de)framing is integrated in the single device called SACHEM.

II. Architecture

The SACHEM is used in both central office (line termination) and remote applications (network termination), and is designed for sampling rates up to 8.8 Ms/s with DMT symbols at 4 kHz. On the other hand it can interface with ATM devices through an Utopia interface (level1 and level2) or synchronous devices through SLAP interface (Alcatel propriety). Following main functions can be distinguished in the SACHEM, see Fig. 3: Up–and downsampling, time domain equalization, time–frequency conversion and vice–versa, frequency domain equalization, symbol alignment, frequency deviation tracking, constellations (de)coding and tone ordering, channel (de)coding and ATM.

A. DSP Front End

The DSP Front End contains a transmit part which performs filtering and upsampling, a receive part which does downsampling and time domain equalization and some test functionality as bypass and transmit–receive looping, see Fig. 4.

The receive path performs decimation and time domain equalization. The decimator receives 16–bit words at 8.8 MHz from the analog Front End and reduces the rate to 552 kHz in central office application

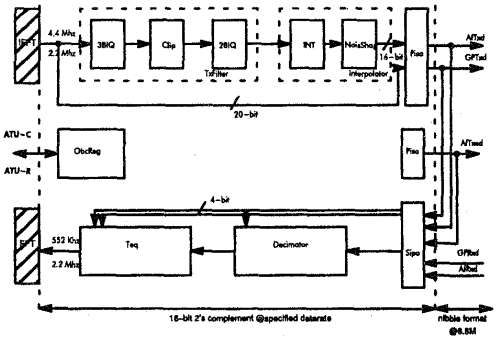

Fig. 4: Dsp Front End architecture.

and 2.2 MHz in remote application. Downsampling by a factor 16 is performed by a cascade of halfband FIR filters: two 3–tap triangular filters reducing the rate by 4, followed by a 15–tap sinx/x Hamming compensated FIR filter also reducing rate by 2 and finalized by a 59–tap sinx/x Hamming compensated FIR filter bringing rate to 552 kHz. The factor 4 downsampling is obtained by dropping the up–front triangular filters and achieving an output rate of 2.2 MHz. The time equalizer is a FIR filter with programmable coefficients, mainly intended to reduce the effect of Inter–Symbol Interference (ISI) by shortening the channel impulse response. Length is determined by the type of applica-

tion, 64–taps in central office and 32–taps in remote configuration.

The transmit direction includes sidelobe filtering, clipping, delay equalization and interpolation. The sidelobe filtering and delay equalization are implemented in a 3–stage and 2–stage biquad (2nd order FIR + IIR), thus reducing the effect of echo. Clipping is limiting the amplitude of the output signal by a FIR–type of structure and as such optimizing the dynamic range of the analog front–end. The interpolator performs an upsampling of 2, from 4.4 MHz to 8.8 MHZ, in central office application by a 7–tap triangular FIR filter. An upsampling of 4, from 2.2 MHz to 8.8 Mhz, is performed in remote application by a simple hold function. The noise shaper is reducing wordsize from 16–bit to 13–bit by a 1–order IIR and thus minimizing noise introduction by wordsize reduction.

B. FFT, Rotor, FEQ and FTG

The Fast Fourier Transformer is instantiated twice in the SACHEM. It is used as a DMT carrier demodulator in the receive direction and as modulator in the transmit direction. It is a programmable machine with instruction set, which can do all processing for one DMT symbol in less than 250 usec and is based on a dedicated pipeline multiplier–accumulator ALU. The ALU contains two 20X18 fixed point multipliers and two busses: one for data, two times 20–bits and one for coefficients, two times 18–bits. The ALU performs complex radix–2 and radix–4 decimation in time (I)FFT butterflies, special 'resolve' butterflies to combine results of real FFT's, complex times complex multiplications with 2^N scaling and complex time real multiplication.

In the receive direction the FFT, see Fig. 5, used as

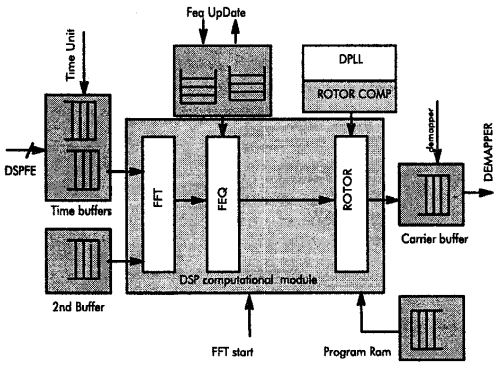

Fig. 5: Receive FFT.

DMT carrier demodulator performs following functions:

– A real time to positive frequencies, from 512 (CO) or 128 (R) time samples to 256 complex positive frequencies with a maximum computing delay of 92 usec.

– Frequency equalization (FEQ), a rotation (360 degrees maximum) to align the received carriers on the X and Y axis, is performed to reduce signal phase rotation by carrier specific channel distortion. Signal amplitude attenuation by the same distortion can be compensated by applying fine gain, between 0 and –6dB, on the FEQ computation and by doing so adjusting received vector to demapping grid. FEQ calculation is performed within 15 usec for remote and 5 usec for central office application.

– ROTOR, performed on positive frequencies, performs a linear phase correction to compensate a misalignment of the sampling clock. Actually it interpolates the sampling clock of the received data to any intermediate point, but in the frequency domain. The following formula applies: $f_i = f_i \cdot e^{j \cdot 2\pi \cdot i \cdot \Delta\Phi}$ where $i.\Delta\Phi$ is the content of an accumulator increment with $\Delta\Phi$ for each next frequency. This rotor process is performed in 2 step, a coarse adjustment followed by fine adjustment, 6 LSB's of rotor value. The computational delay is 30 usec in remote and 9 usec in central office application.

In the transmit direction the IFFT performs complementary operations:

– Fine tune gain (FTG), meant to correct gain of individual carriers, an operation taking 15 usec for 256 frequencies (R) and 30 usec for 512 frequencies (CO).

– ROTOR calculation to adjust the frequency error between local X–tal and desired transmit frequency. Computing delay of both operations, coarse and fine is 30 usec for remote mode and 60 usec for central office application.

– The IFFT performs a positive frequency to real time samples conversion: in remote mode 256 positive frequencies are processed, yielding 512 time samples within 76 usec while in central office mode 512 positive frequencies are converted to 1024 time samples within 178 usec.

C. Constellation (de)coding

Receive part mainly contains following blocks:

– Demapper which converts the FFT computed constellation points to a block of bits by use of a programming table (tone ordering). This essentially consists in identifying a point in the 2D QAM constellation plane. It is also capable of demodulating 4D Trellis encoded carriers [4][5] by the 2D subset information provided by Trellis decoder.

– The Viterbi decoder, see Fig. 6, collects data during

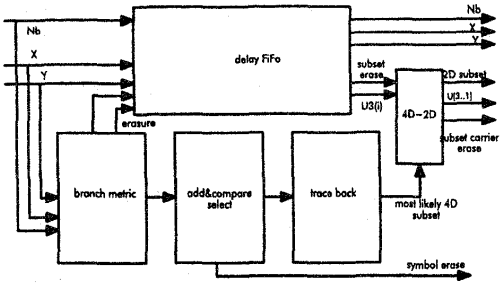

Fig. 6: Viterbi decoder.

a number of cycles and estimates the most likely 4D subset based on a long data sequence. It computes 64 branch metrics, performs 16 add–compare&selects, uses a backtrace length of 20 4D symbols and translates 4D to 2D subset information per 2 tones to provide information towards the demapping process.

– The Monitor computes error parameters that will be used for software updates of adaptive filter coefficients (FEQ, TEQ), clock phase adjustment (DPLL) and error detection (loss of signal, loss of frame). Signal detection, also a part of monitoring activities, is build around 8 configured leaky integrators whose outputs are fed to a highly programmable level detector. Error parameters obtained from linear monitoring can be used for automatic hardware updates of FEQ coefficients. This adaptive process can be inhibited for pilot tone or incase of missing signal to block incorrect coefficient updates.

The transmit block has less complexity and only contains following functions: 4D Trellis encoding and mapping of data by use of programming table (tone ordering). The Trellis encoder fetches information of a pair of tones and adds 1 redundant bit, thus creating an overhead of 1/2 bit per tone.

D. Transmission Convergence layer

The data received from the demapper is split into two paths, one dedicated to the interleaved or slow data flow and the other one for the non–interleaved or fast data flow. Except for interleaving/deinterleaving, those 2 flows are identical, from demapper to slap or utopia interface as well as from interface to mapper. For the purpose of clarity, only one flow is shown on Figure 3. The interleaving/deinterleaving is used to increase the error correction capabilities of block codes for error burst. A block code with depth D increases the burst errors capability from T–bytes to D*T bytes. SACHEM uses rectangular interleaving with depths 1,2,4,8, 16, 32 and 64.

The Reed Solomon decoder [6][7] is able to correct errored bytes by using the redundant bytes and erasure information. The error correcting capabilities of a Reed Solomon (N,M) code is limited to following equation:

$$(Ed + 2*Eu) \leq (N - M)$$

where Ed number of erased byte, Eu number of undetected error bytes, N number of RS codeword bytes and M number of data bytes. The SACHEM, configured up to 16 overhead bytes (N is even), is capable of decoding 3 codewords (N = 255) within one DMT symbol.

Two PDM descramblers are used, one for slow and one for fast, performing $d_n' = d_n \oplus d_{n-18}' \oplus d_{n-23}'$ as specified in the ADSL standard T1.413 [1].

The deframer is a highly programmable synchronization machine with a variable synchronization delay according to: (S * D) mod 272 with S being number of DMT symbols per codeword (S = 0.5, 1, 2, 4, 8, 16) and D being interleaving depth. The extracted First, A and B byte are sent towards CRC, EOC, AOC termination.

Finally the two byte streams (slow and fast) are presented to ATM byte–based processing unit which provides basic cell functions like cell synchronization, payload descrambling, idle/unassigned cell filtering and cell header detection and correction all according the ITU–T I.163 standard. Provision is also made for Bit Error Rate measurement (BER).

The transmit path is the dual of receive path and contains ATM TC layer functions, framing, PDM scrambling, Reed Solomon encoding and interleaving.

III. Design Methodology

As a result of design methodology improvement activities, a continuous process at Alcaltel Antwerp, three new basic approaches were introduced in the design flow in order to meet stringent time to market requirements: modelling (C++ and behavioral VHDL), simulation flexibility and design mapping on emulator to speed up test and software development even before any silicon was available.

Bit–true C–models of PMD layer were used to verify system performance and match versus VHDL simulation results. The simulation environment of SACHEM was build in a manner that designers were able to switch between behavioral, RTL, Verilog gate–level or mapped database (emulator) simulations without worrying about stimuli or input files. Mapping of the SACHEM on an emulator enabled us to significantly speed up simulation time with a factor of more than 100 when the emulator was driven directly by a workstation, or more than 100,000 when the emulator was driven by a test board (with simulation software

being compiled on the target on–board controller). Moreover, software development could start as soon as netlist was mapped, i.e. several weeks before first available samples.

All together, these new design methodology approaches resulted in a 3 to 6 months reduction in developpement time. As they are not specific for SACHEM design, these approaches will be part of the design flow for every new ASIC designed at Alcatel Antwerp.

IV. Results

A photograph of the SACHEM is included, see Fig. 7. The device is designed in 0.35 um digital

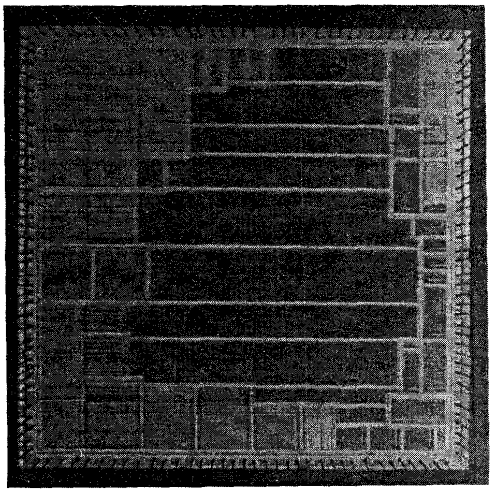

Fig. 7: Photograph of SACHEM.

CMOS technology (5 metal layers) and packaged in a 144–pins PQFP. Thanks to special attention during development, appealing power consumption and silicon area figures were obtained, especially when compared to designs of such complexity: SACHEM only consumes 800 mW in operational conditions (3.3 V, ambient temperature) while its area is well below 100 mm2.

V. Conclusion

This paper shows a high complexity design, approaching the system on chip concept, which was developed within a very short lead time and introduced new design methodology concepts such as modelling and use of emulation for parallel engineering (hardware and software).

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