TP 14.6 A 70Mb/s Variable-Rate DMT-Based Modem for VDSL

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Very high-speed digital subcriber line (VDSL) technology can deliver data at multi-Mbits/s over the unshielded, twisted pair in overlay to the plain old telephone service (POTS) and ISDN services [1,2]. Discrete multi-tone (DMT) is one candidate for the modulation of VDSL. The DMT transmit signal is the sum of independent quadrature amplitude modulated (QAM) carriers spread over a bandwidth of 11.04 MHz. Time division duplexing (TDD) is used to provide a half-duplex communication channel over a single pair [1,2]. This chip integrates the complete digital signal processing required by a TDD-DMT VDSL system and the Transport Convergence (TC) sublayer functions such as (de)interleaving, Reed-Solomon (de)coding, (de)scrambling, (de)framing and the ATM-specific TC functions (Figure 14.6.1). It can be used both at the Network Termination (NT) and the Line Termination (LT) side.

DMT modulation and demodulation is by an FFT/IFFT block. This block performs a 512 points real FFT in less than 20µs. The FFT/IFFT is decomposed in complex radix-2, radix-4 and special resolve butterflies to combine results of the real FFT [3]. The block is based on a dedicated pipelined dual ALU. ALU0 can perform radix-4, radix-2 and special resolve butterflies. ALU1 needs only perform radix-4 operations (Figure 14.6.2). ALU1 is therefore 20% less complex than ALU0. To perform a complete 512 point real FFT, input data are read from the input buffer, pass ALU1, are temporarily reorganised in a small scratch buffer, pass ALU0 and are stored in the output buffer. This process is repeated twice and the final result is available in the output buffer (Figure 14.6.2). Table 14.6.2 summarizes the configuration of both ALU for the IFFT and FFT during the 3 passes. Data and twiddle coefficients are coded as floating point with 13 bits mantissa and 4 bits exponent, avoiding the use of block floating point with intermediate scaling between the radix [4]. Using a bit-true C++ model, optimum bit length for each intermediate stage of the ALU is derived. Simulations have shown that the noise generated by the FFT/IFFT block is well under the noise level of the VDSL system in the most favorable configuration.

In the front-end receive part of the chip, a variable rate decimator is followed by a variable rate Time Equalization (TEQ) block implemented as a FIR filter with programmable coefficients. The length of the TEQ can be programmed from 1 to 32 taps depending on the application. In the transmit path, a variable rate interpolator shares the same hardware as the decimator, due to the TDD scheme.

The hardest noise encountered in VDSL system is radio-frequency interference (RFI). Its power spectral density is typically well above the received signal (Figure 14.6.3). A programmable digital RFI canceller works in the frequency domain [5]. The RFI noise can be detected on 4 predefined frequency bands for each DMT symbol. The interference of two simultaneous RFI on the neighboring carriers can be reduced. The same floating-point format as for the FFT/IFFT block is used here to cope with the data dynamics encountered in the presence of RFI. A windowing is performed on the samples in the time domain, just before the FFT. Combining this windowing with the digital RFI cancelling yields an interference reduction of 45dB on the neighboring carriers.

Symbol timing recovery uses a digital phase-locked loop (PLL). This DPLL can be programmed to be of the second order or the third order with a bandwidth ranging from 0.1Hz to 100Hz, depending on the location of the chip in the system. The phase difference between receiver and transmitter clock is measured at the Demapper block and filtered out by a proportional-integral filter and then integrated to produce a value used to perform a digital rotation on each carriers in the frequency domain in both transmit and receive paths (Figure 14.6.1).

A slave Utopia interface provides the chip with ATM cells. Scrambling, header error control (HEC) generation and Idle cell insertion can be applied in the transmit direction. In the receive direction, basic ATM cell functions like cell synchronization, payload descrambling, idle/unassigned cell filtering and cell header detection and correction are provided.

A fully programmable Reed-Solomon (RS) encoder protects against random and burst errors. The number of check bytes can be programmed from 0 to 16 Band the number of data bytes can be programmed from 2 to 255B. An interleaver protects against error bursts by spreading the errors over a number of RS code-words. It is a triangular interleaver, with parameter I ranging from 1 to 255 and parameter M ranging from 1 to 34 (Figure 14.6.4). In the receive part, a programmable RS decoder and a deinterleaver perform the opposite transform. The parameters ranges are the same as for the transmit side. Two on-chip 32kB RAMs are provided to support the full parameter range for the interleaver and deinterleaver.

For some services, a constant data delay is mandatory, even if the bit rate on the line is changing. Therefore, the parameters of the interleaver/deinterleaver and RS encoder/decoder can be modified during normal operation of the chip, without any interruption or error generation. The synchronization between transmit and receive (of two different chips) is guaranteed by counting on both ends the number of transmitted and received RS code-words [6].

All the blocks of the chip can be separately bypassed for debugging. A central block, the Timing Unit, is responsible for chip synchronization of the chip and proper sequencing of operations.

A complete bit-true C model of the chip is available. The chip processes a 70Mb/s data stream coming from or going to the Utopia interface.

A buffer-tree used for clock distribution reduces power dissipated by the clock network. The characteristics of the chip are described in Table 14.6.1. A micrograph of the chip is available in Figure 14.6.5.

Acknowledgements:
The authors thank F. De Meersman and H. Fabri for contribution to chip layout.

References:
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[3] A.V. Oppenheim, R.W. Schafer, Discrete-Time Signal Processing, Prentice-Hall, 1989.
[4] L. Kiss et al., "A Customizable DSP for DMT-based ADSL Modem", Proceedings of the 24 th IEEE European Solid-State Circuits Conference, September 22-24, 1998, The Hague, The Netherlands.
[5] P. Spruyt, S. Braet, "Solving the Issue of Radio Interference when Deploying Digital Subcriber Lines", in Broadband Access Networks, D.W. Faulkner and A.L. Harmer (Eds.), IOS Press 1997, pp. 98-105. [6] M. Peeters, P. Spruyt, "A Dynamic Interleaving Scheme for VDSL," ANSI T1E1.4/97-052.
[6] R. Peters, P.Spruyt, "A dynamic Interleaving Scheme for VDSL," ANSI T1E1, 4/97-052.

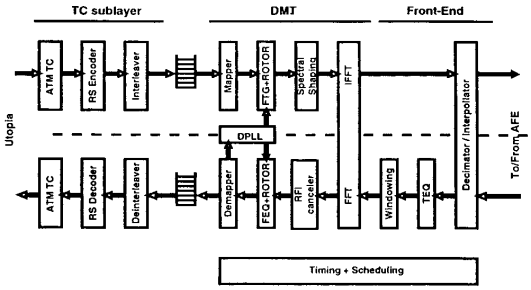


Figure 14.6.1: Chip block diagram.

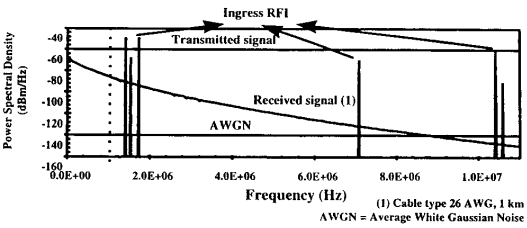


Figure 14.6.3: RFI noise characteristics.

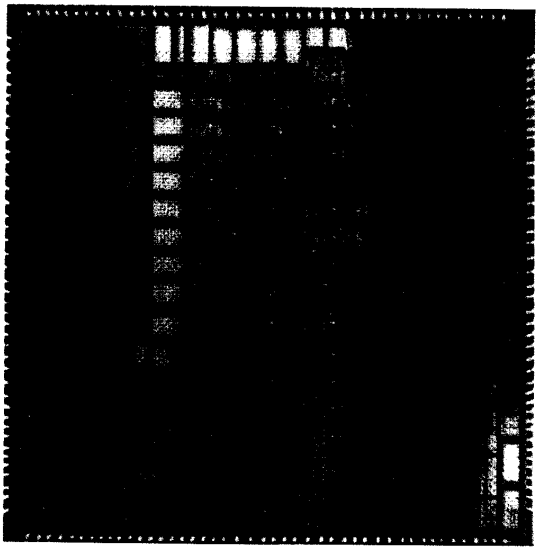
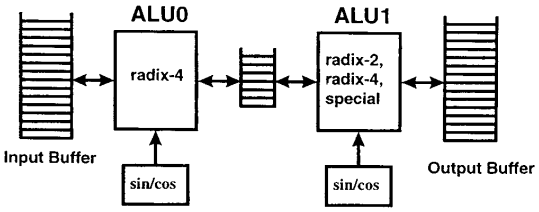


Figure 14.6.5: VDSL chip micrograph.



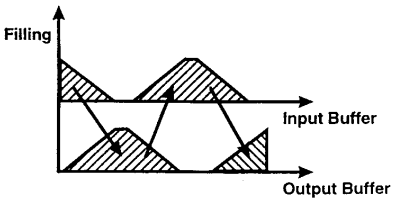


Figure 14.6.2: FFT architecture.

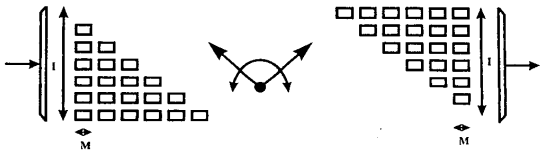


Figure 14.6.4: Interleaver.

Technology	0.35 µm 5-metal CMOS
Gate	680k
RAM	900kbit
Frequency	44.16 MHz
Area	150 mm^2
Package	PQFP-208
Transistors	9.0M
Power dissipation	2.7 W at 3.3 V

Table 14.6.1: Chip characteristics.

FFT	ALU1	ALU0
pass 1	bypass	radix-2
pass 2	radix-4	radix-4
pass 3	radix-4	special butterfly

IFFT	ALU1	ALU0
pass 1	bypass	special butterfly
pass 2	radix-4	radix-4
pass 3	radix-4	radix-4

Table 14.6.2: FFT and IFFT ALU usage.