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Fadavi-Ardekani et al.

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(54) **MULTI-SESSION ASYMMETRIC DIGITAL SUBSCRIBER LINE BUFFERING AND SCHEDULING APPARATUS AND METHOD**

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(52) **U.S. Cl.** **370/395.5**; 370/466; 370/480; 375/222

(58) **Field of Search** 370/230, 235, 370/235.1, 395.1, 412, 428, 429, 395.5, 480, 503, 505, 511, 512, 513, 514, 516; 375/222

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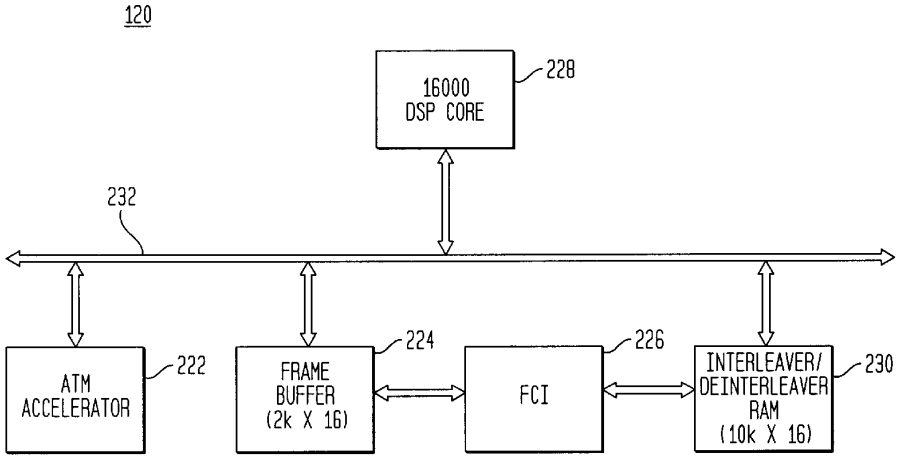
(57) **ABSTRACT**

A transceiver for an asymmetric communication system is provided that implements a buffering and scheduling scheme that utilizes a virtual clock signal to synchronize processing of asynchronous frame data for multiple ADSL sessions. In every virtual clock cycle, the transceiver first sequentially performs transmit-processes for each active ADSL line and then sequentially performs receive-processes for each active ADSL line. An Asynchronous Transfer Mode (ATM) Accelerator provides the network interface to multiple ATM channels and communicates frame data to a Frame Buffer (FB). The FB may be used in a ping-pang fashion for the communication of data between the ATM accelerator and a Framer/Coder/Interleaver (FCI), which performs its namesake, among other, functions. The FCI also interfaces a Digital Signal Processing (DSP) core through an Interleave/De-Interleave Memory (IDIM). The DSP core generates the virtual clock signal, which schedules operation of the ATM accelerator and the FCI. IDIM holds DMT frames of data and may also be utilized in a ping-pang fashion. Memory is shared by multiple ADSL sessions and by the transmit and receive processes within an individual session.

26 Claims, 2 Drawing Sheets



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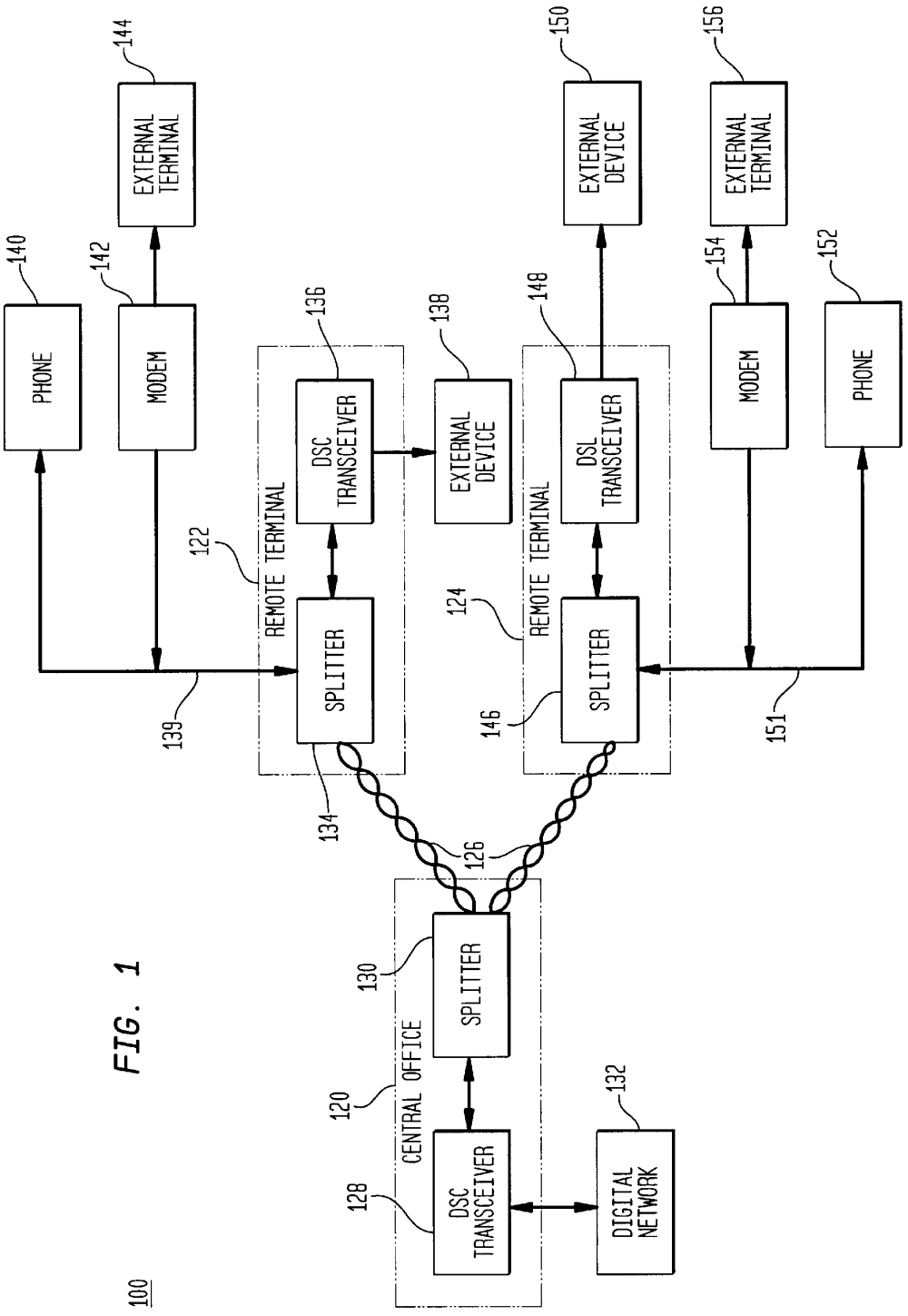

FIG. 1

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FIG. 2

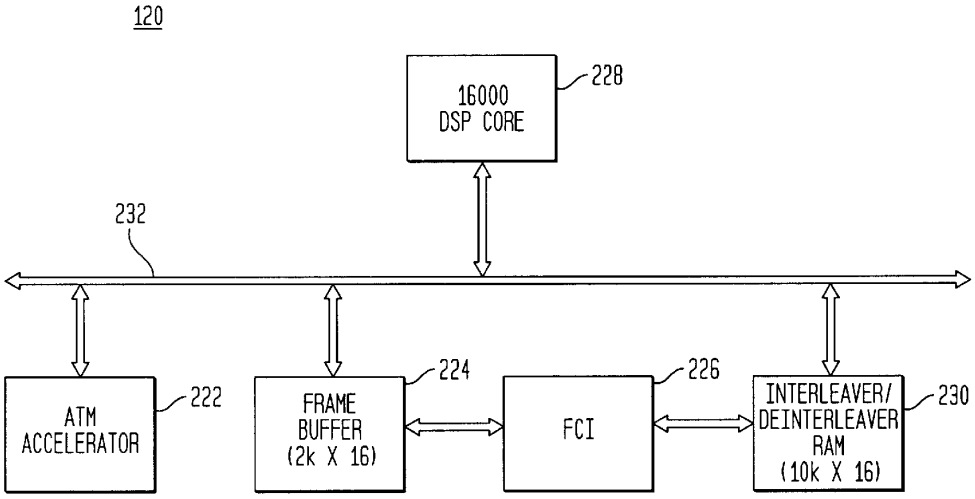
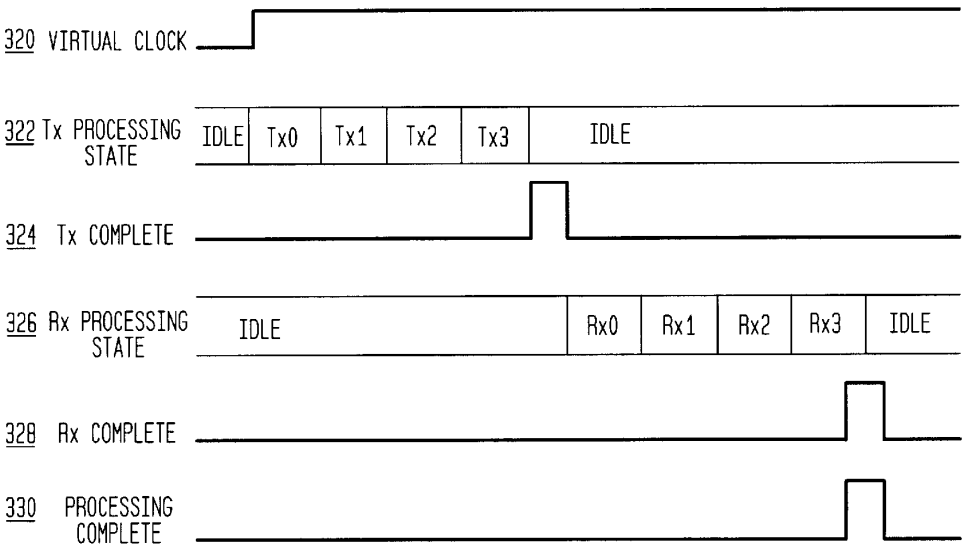


FIG. 3



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MULTI-SESSION ASYMMETRIC DIGITAL SUBSCRIBER LINE BUFFERING AND SCHEDULING APPARATUS AND METHOD

FIELD OF THE INVENTION

The invention relates generally to broadband communications, and more particularly to the transmission of broadband signals using twisted-pair cable.

BACKGROUND

High-speed data communications paths are desirable for Internet access and are essential for high data rate interactive services such as video on demand. Since fiber optic cable, the preferred transmission media for such services, is not readily available in the transmission link between a network node and a user premise and is prohibitively expensive to install, it is desirable to utilize the existing Plain Old Telephone Service (POTS) infrastructure. However, current POTS wiring connections consist of copper twisted-pair media which was designed for low frequency, voice-band (0–3400 Hz) analog telephony, and does not readily support the data rates or bandwidth required for high data rate interactive services. Conventional POTS analog transmission is limited to a data rate of about 56 Kbps, which represents only a small portion of the amount of information that can be transmitted over twisted-pair media.

DSL (Digital Subscriber Line) provides a method of communicating high-bandwidth data over twisted-pair media. In addition, some forms of DSL service (e.g., ADSL) include a subdivision of the DSL bandwidth so that some bandwidth is used to provide POTS service simultaneously with data transmission. Thus, DSL enables high data rate interactive services without requiring the installation of fiber optic cable.

Asymmetrical Digital Subscriber Line (ADSL (ANSI T 1.413-1998)) is specifically designed to exploit the asymmetric nature of most multimedia communication, in which large amounts of information flow toward an end user (i.e., downstream) and only a small amount of information (e.g., interactive control information) is returned by the end user to a central office (i.e., upstream). ADSL is "asymmetric" in that most of its two-way (duplex) bandwidth is utilized to transmit downstream and only a small portion is utilized for upstream transmission. Using ADSL, approximately 6–8 Mbps of data can be sent downstream and approximately 512 Kbps can be sent upstream. Other variations of DSL (i.e., xDSL) include High bit rate DSL (HDSL) and Very high bit rate DSL (VDSL).

Many DSL technologies require that a signal splitter be installed at a remote end user location to split POTS service from the digital data transmission. However, the line split for an end user can be managed remotely from a central office using G.Lite (a/k/a DSL Lite, splitterless ADSL, and Universal ADSL), which is essentially a slower form of ADSL. Equipment installation costs are saved using G.Lite (ITU-T standard G-992.2), which provides a data rate of approximately 1.5 Mbps downstream and approximately 512 Kbps upstream.

In a conventional ADSL communication system, an ADSL transceiver at each end of a twisted-pair (a remote end user premise and a central office) connects to the twisted-pair circuit, creating information channels—a high speed downstream channel, a medium speed upstream channel, and depending on implementation, a POTS or an Integrated Services Digital Network (ISDN) channel. Each channel can be sub-multiplexed to form multiple, lower rate channels utilizing one of several modulation technologies. One such modulation technology, Discrete MultiTone (DMT), is a multi-carrier technique that divides the available bandwidth of twisted-pair media connections into mini-subchannels or bins. In the ADSL standard, DMT may be used to generate up to 250 separate 4.3125 Khz subchannels from 26 Khz to 1.1 Mhz for downstream transmission and up to 26 subchannels from 26 Khz to 138 Khz for upstream transmission. Other modulation technologies used with ADSL include Carrierless Amplitude Modulation (CAP) and Multiple Virtual Line (MVL).

At the central office in a typical ADSL system, a Digital Subscriber Line Access Multiplexer (DSLAM) multiplexes/de-multiplexes a unique set of data for each of multiple ADSL lines, concentrating the ADSL lines into a single terminating device for connection onto the backbone network interconnecting central offices. An ADSL transceiver associated with each ADSL line is in communication with the DSLAM. For the unique data stream of each ADSL line, the ADSL transceiver provides data to (and receives data from) several channels with the data grouped into frames that include both payload data bytes and overhead data bytes. Data from each channel is placed in different positions in a frame depending on whether the data is interleaved or non-interleaved. In general, for transmission, a frame is assembled from the payload data of the channels with overhead bytes appended as appropriate. In particular, a cyclic redundancy check (CRC), scramble, interleave (if selected), and forward error correction (FEC) are performed on the frame data prior to its transmission. The frames in turn are grouped together into a "superframe" which includes 68 data frames plus an additional synchronization frame, which delineates the superframe boundary. A CRC is performed on all the data in a superframe and transmitted in the overhead bytes of the first frame of the next superframe. The frame data is converted into a set of complex symbols, each of which represents a number of frame bits as defined by a bit allocation table. These complex symbols are subsequently converted into an analog signal that is transmitted on a twisted-pair. Conversely, when receiving an analog signal from a twisted-pair, an ADSL transceiver must convert the analog signal into complex digital symbols, convert the complex symbols into a receive frame, and de-interleave, FEC, CRC, and de-scramble the received frame to recover payload data.

In order to provide service to multiple remote end user premises, the central office of an ADSL communication system needs to support multiple ADSL lines, each line having a session or active period of data transfer. In addition, the central office must manage asynchronous downstream and upstream data streams for each ADSL session since, the recurrence of frames containing data for/from an individual remote end user is not necessarily periodic. In a conventional ADSL communication system, the central office has an ADSL transceiver for each remote end user served by the system. Such a system is excessively duplicative in terms of transceivers and memory in each transceiver, and thus more costly than necessary to provide the desired functionality.

SUMMARY OF THE INVENTION

The invention provides an Asymmetric Digital Subscriber Line (ADSL) transceiver that manages multiple asynchronous ADSL sessions, synchronizing the digital signal processing tasks for the sessions with a buffering and scheduling scheme such that the various transceiver components operate seamlessly (i.e., in a semi-synchronous fashion).

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Utilizing this buffering and scheduling methodology, reductions in the design sizes of various transceiver components and the data flow complexity of the transceiver may be achieved.

A central office transceiver (i.e., headend processor) according to the invention includes various functional elements and memories coupled together with digital signal processing tasks synchronized by a virtual clock signal. An Asynchronous Transfer Mode (ATM) Accelerator provides the network interface to multiple ATM channels for multiple asynchronous ADSL sessions. The ATM accelerator transfers frame data to a Frame Buffer (FB) as controlled by a Digital Signal Processing (DSP) core. The FB provides a dual access memory that is used in a ping-pang fashion, based on the logic level of the virtual clock, for the communication of data between the ATM accelerator and a Framer/Coder/Interleaver (FCI). The FCI performs various processing tasks on the frame data and also interfaces the DSP core through an Interleave/De-interleave Memory (IDIM), which holds DMT frames of data and may also be utilized in a ping-pang fashion. The DSP core generates the virtual clock signal, which is approximately 4 Khz and coincides with the ADSL Discrete MultiTone (DMT) symbol rate. The DSP core controls operation of the ATM accelerator and the FCI and performs various processing tasks such as moving data to/from the FB and the IDIM.

According to the buffering and scheduling scheme of the invention, after every transition of the virtual clock signal (i.e., in every virtual clock cycle), the transceiver first steps through ADSL lines, performing FCI transmit-processes for each active ADSL line and generating a control signal after completing all transmit-processes. The FCI then again steps through ADSL lines, processing receive-processes for all active ADSL lines and generating control signals indicating completion of receive processes and completion of all processing.

In every virtual clock cycle, the DSP core provides the FCI with data by reading Receive (RX) data frames to and loading Transmit (TX) data frames from the FB after processing. The FB is divided into segments for each individual ADSL session with the same memory space used for both RX data and TX data. The FCI and ATM accelerator first perform reading processes and then loading processes, reading RX data first before loading the TX data into the FB. In this way, the same buffer can be used for both RX data and TX data, thereby permitting the FB memory to be half the size of that in a conventional ADSL transceiver arrangement. The DSP core also loads RX data frames and reads TX data frames to/from the IDIM, which may be used in a ping-pang fashion by the FCI and DSP core.

Numerous other advantages and features of the present invention will become readily apparent from the following detailed description of the invention and the embodiments thereof, from the claims and from the accompanying drawings in which details of the invention are fully and completely disclosed as a part of this specification.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference may be had to the following Detailed Description of exemplary embodiments thereof, considered in conjunction with the accompanying drawings, in which:

FIG. **1** illustrates, in block diagram form, an Asymmetric Digital Subscriber Line (ADSL) system/in accordance with the invention;

FIG. **2** illustrates, in block diagram form, an ADSL transceiver for a central office in accordance with the invention;

FIG. **3** illustrates, an exemplary processing sequencing for a case when four Transmit and Receive lines are enabled;

In the detailed description below, like reference numerals are used to describe the same, similar or corresponding elements in FIGS. **1–3**.

DETAILED DESCRIPTION

A headend transceiver (i.e., central office side processor) is provided for processing Asymmetric Digital Subscriber Line (ADSL) data. The provided ADSL transceiver implements a buffering and scheduling scheme for synchronizing the digital signal processing tasks for multiple asynchronous ADSL lines. As a result, the various components of the ADSL transceiver are able to operate seamlessly (i.e., in a semi-synchronous fashion) and the design sizes of various transceiver components and the data flow complexity of the transceiver are reduced. It should be noted, however, that the ADSL transceiver of the invention may alternatively incorporate other variations of DSL (i.e., xDSL), such as High bit-rate DSL (HDSL) and Very high bit-rate DSL (VDSL).

Asymmetric Digital Subscriber Line Communication System

FIG. **1** illustrates, in block diagram form, an Asymmetric Digital Subscriber Line (ADSL) system in accordance with the invention. The ADSL system **100** includes a central office **120** and remote end user terminals 122–124, which are connected together copper twisted-pair media forming a telephone line **126**. The central office **120** includes an ADSL transceiver according to the invention **128** and a splitter **130**. Central office ADSL transceiver **128** is bi-directionally coupled to the splitter **130** and is additionally bi-directionally coupled externally to a digital network **132**.

A first remote end user terminal **122** includes splitter **134** and conventional ADSL transceiver **136**. ADSL transceiver **136** is bi-directionally coupled to splitter **134** and is additionally coupled to external device **138**. The splitter **134** is bi-directionally coupled via a Plain Old Telephone Service (POTS) channel **139** to a telephone **140** and is additionally coupled to a modem **142**. The modem **142** is further coupled to an external terminal **144**. The second remote end user terminal **124** is similarly arranged. The second remote end user terminal **124** includes a splitter **146** and a conventional ADSL transceiver **148**. The ADSL transceiver **148** is bi-directionally coupled to the splitter **146** and is additionally coupled to an external device **150**. The splitter **146** is bi-directionally coupled via a POTS channel **151** to a telephone **152** and additionally coupled to a modem **154**, which is further coupled to an external terminal **156**.

The exemplary digital communication system **100** allows high-speed data communication between a variety of remote end users having computers, telephones, fax machines, modems, television sets, and any number of other communication devices. Digital network **132** is used to transmit information for a variety of high data rate interactive services, each of which may have a different transmission format and frequency. An exemplary digital communication system employing G.lite is similar to FIG. **1**, with splitters **130**, **134** and **146** merely replaced by a hardware device providing a direct correction to ADSL transceivers **128**, **136**, and **148** respectively.

Central Office ADSL Transceiver

FIG. **2** illustrates a central office ADSL transceiver **120** according to the invention. The transceiver implements a

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