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# United States Patent [19]

## Garde

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[54] **CLOCKING SCHEME FOR DIGITAL SIGNAL PROCESSOR SYSTEM**

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[73] Assignee: **Analog Devices, Inc.**, Norwood, Mass.

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[51] **Int. Cl.$^6$** ....................................................... **G06F 1/04**
[52] **U.S. Cl.** .............................................................. **713/600**
[58] **Field of Search** .................................... 395/553, 555, 395/556, 559; 713/500, 501, 600; 709/400, 248

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[57] **ABSTRACT**

A digital signal processing system includes a cluster of processors and a host. A host can access each of the processors through an external bus system that interconnects the host with each of the processors. An external port of each of the processors operates at one of a local clock frequency and host clock frequency, the local clock frequency and host clock frequency being asynchronous with one another. The host operates at the host clock frequency. Upon a host access of one of the processors, the clock frequency of operation of the external parallel port of each processor automatically is controlled to operate at the host clock frequency. In an embodiment, each processor also includes a core processor that operates at a core clock frequency that is a multiple of the local clock frequency, asynchronous with the host clock frequency. Thus, the speed of operation of the core processor and that of the external parallel port can be optimized independently.

**12 Claims, 6 Drawing Sheets**

## FIG. 1



LCLK   HCLK   LCLK   HCLK

P2 — PROC.   PROC. — P1

HCLK   100

— 102   — 104

MEM.   HOST

CLK

— 108

ANALOG SWITCH   — 106   110

LCLK   HCLK   P3   P4   BUFFERS — HCLK'

PROC.   PROC.   HCLK's TO EACH DESTINATION

LCLK   HCLK   LCLK   HCLK   — 112

BUFFERS — LCLK'

LCLK's TO EACH DESTINATION

## FIG. 2



P1

LCLK

PCLK

MUX   MCLK

HCLK   124
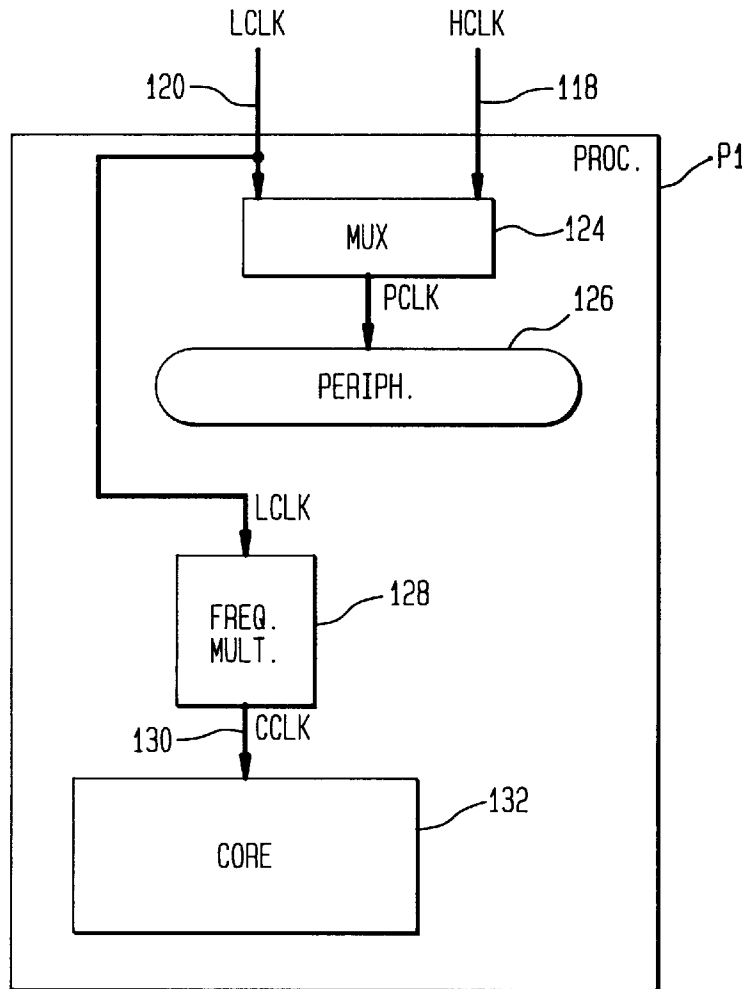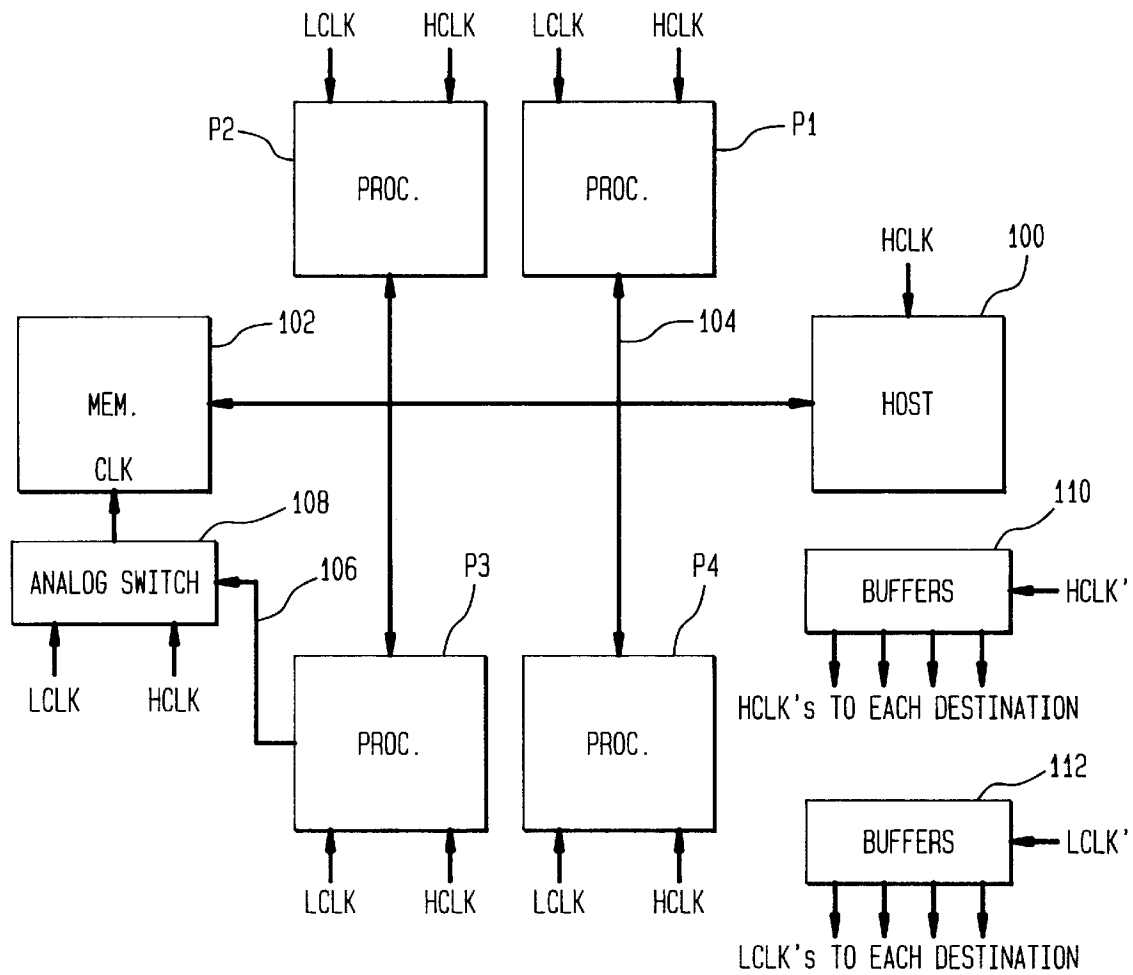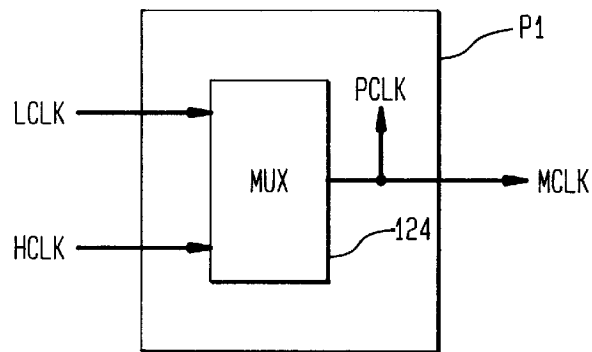
*FIG. 3*

# FIG. 4

## FIG. 5

# DOCKET ALARM
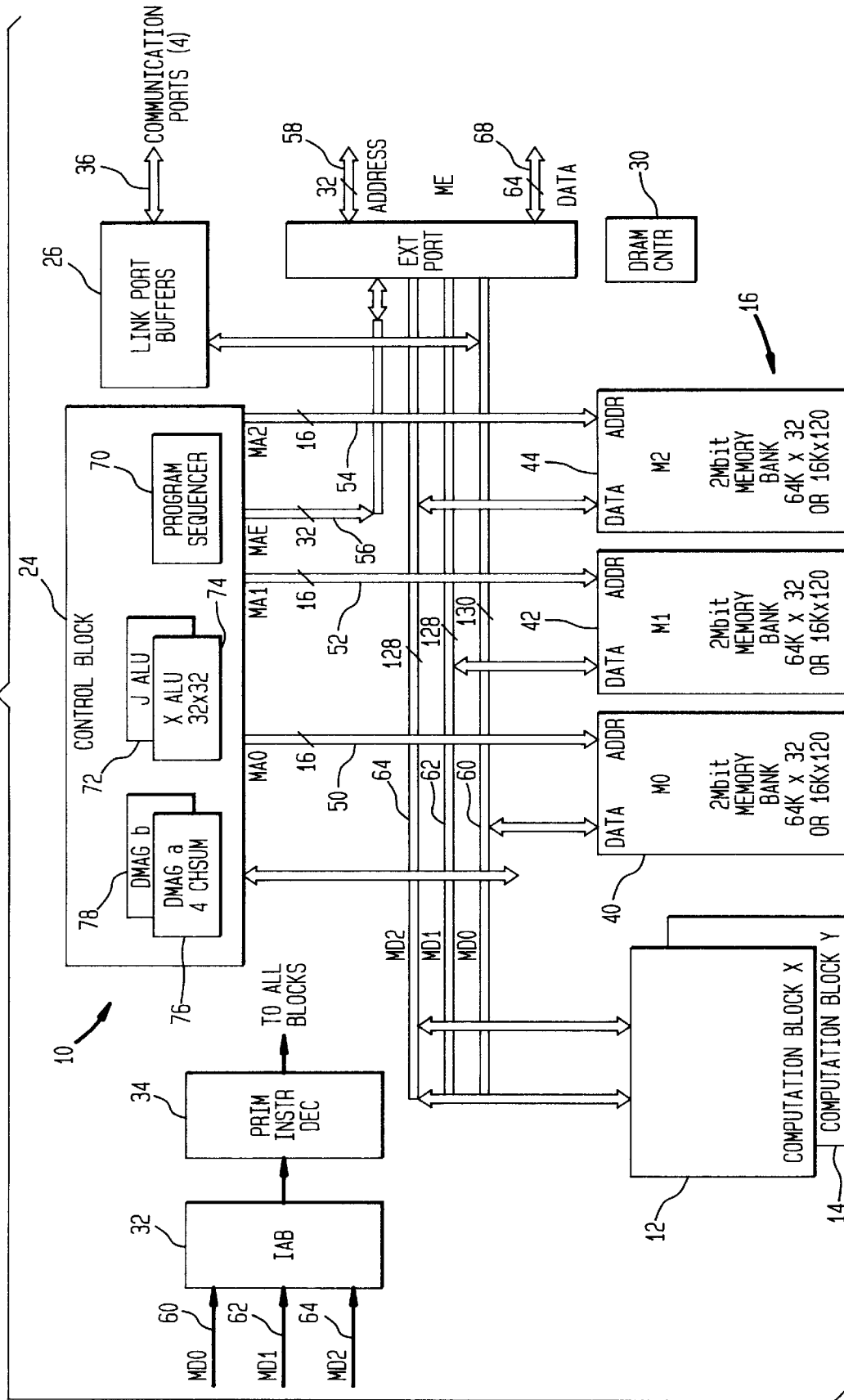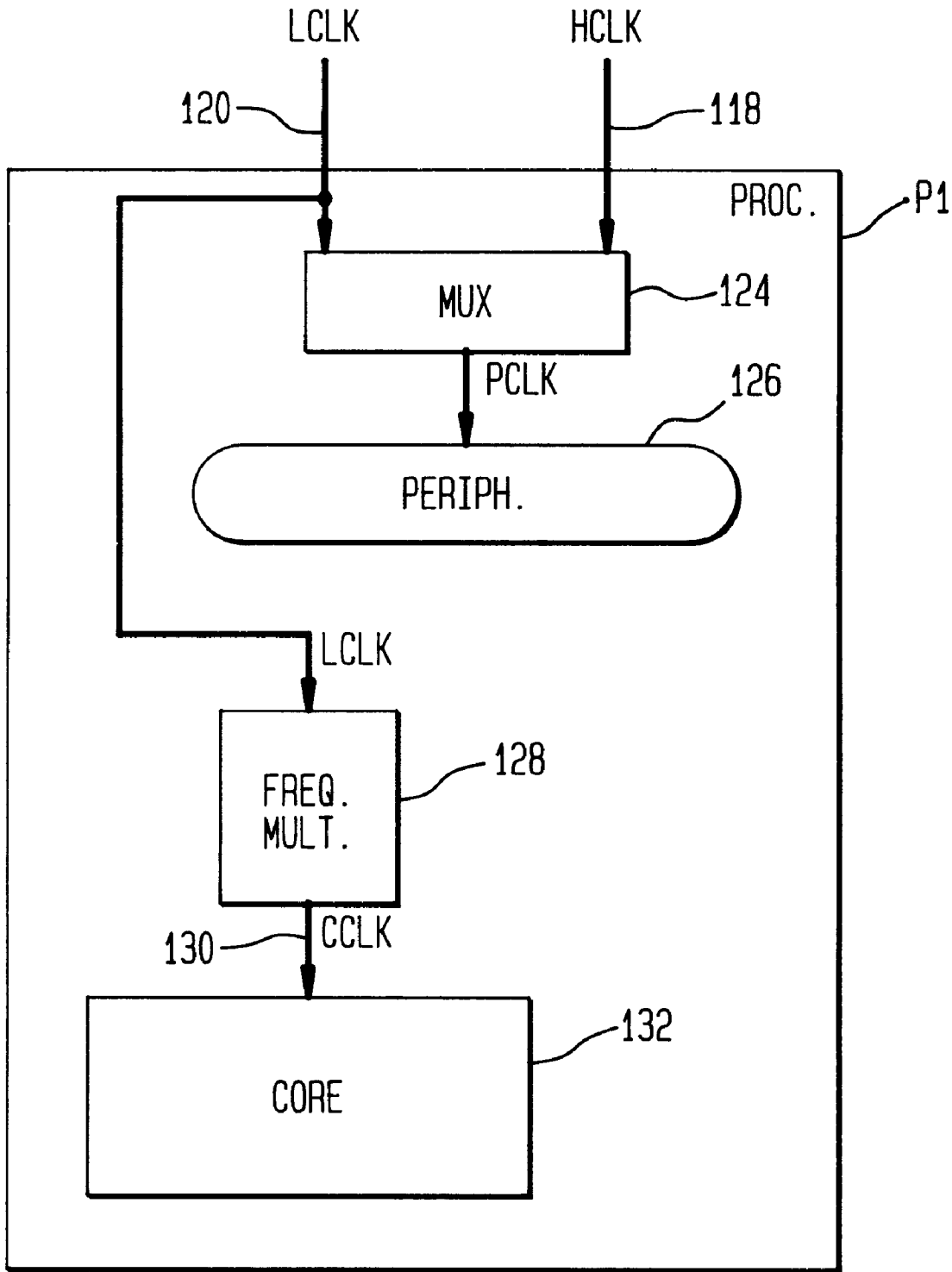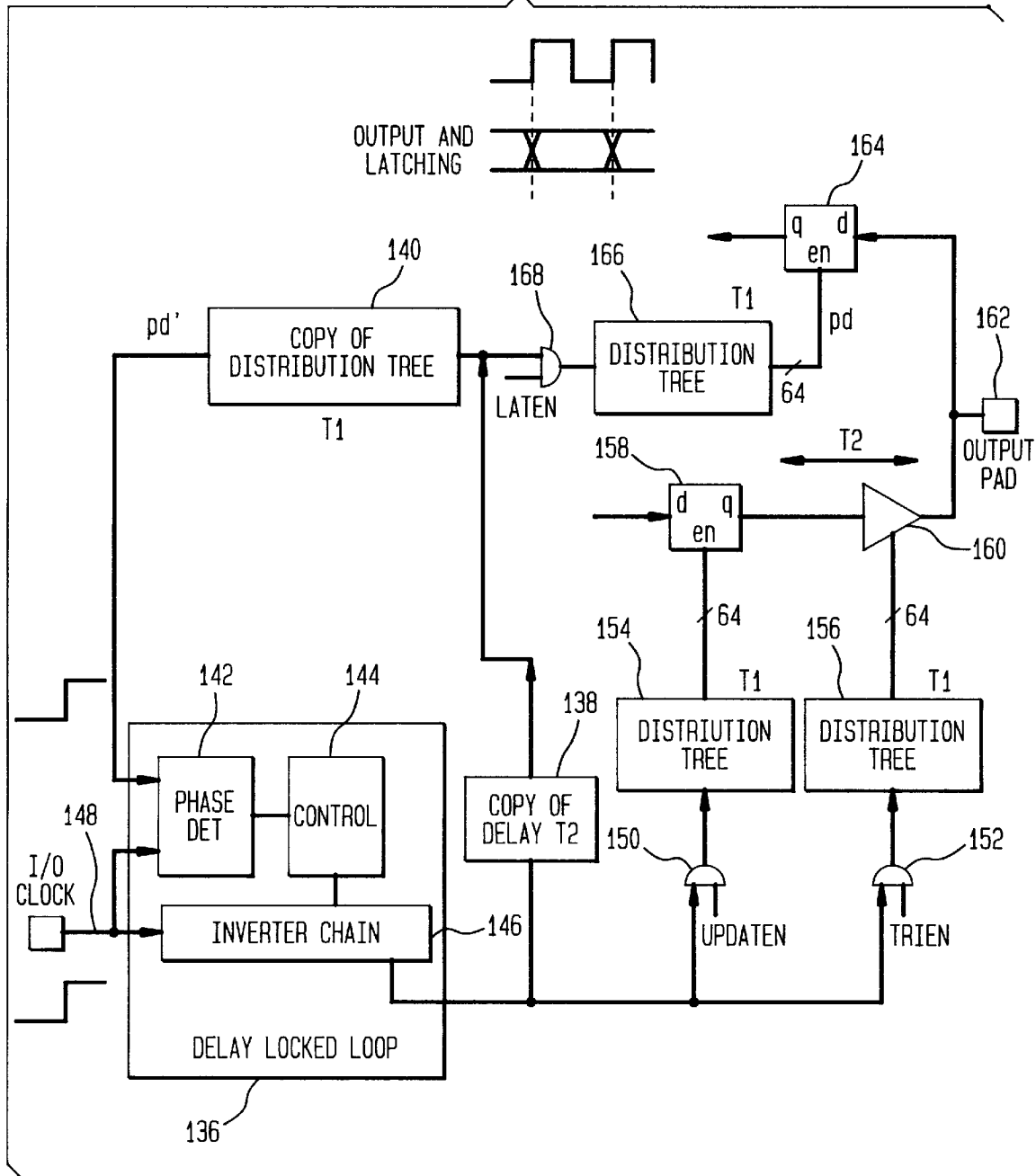
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