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[54] **METHOD AND APPARATUS FOR A UNIFIED PARALLEL PROCESSING ARCHITECTURE**

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[51] **Int. Cl.**[6] **G06F 3/60**

[52] **U.S. Cl.** **395/800;** 395/200; 395/425; 364/DIG. 1; 364/229; 364/243

[58] **Field of Search** 395/200, 800, 425

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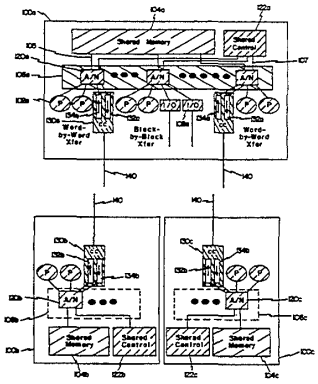
[57] **ABSTRACT**

A unified parallel processing architecture connects together an extendible number of clusters of multiple numbers of processors to create a high performance parallel processing computer system. Multiple processors are grouped together into four or more physically separable clusters, each cluster having a common cluster shared memory that is symmetrically accessible by all of the processors in that cluster; however, only some of the clusters are adjacently interconnected. Clusters are adjacently interconnected to form a floating shared memory if certain memory access conditions relating to relative memory latency and relative data locality can create an effective shared memory parallel programming environment. A shared memory model can be used with programs that can be executed in the cluster shared memory of a single cluster, or in the floating shared memory that is defined across an extended shared memory space comprised of the cluster shared memories of any set of adjacently interconnected clusters. A distributed memory model can be used with any programs that are to be executed in the cluster shared memories of any non-adjacently interconnected clusters. The adjacent interconnection of multiple clusters of processors to a create a floating shared memory effectively combines all three type of memory models, pure shared memory, extended shared memory and distributed shared memory, into a unified parallel processing architecture.

24 Claims, 12 Drawing Sheets



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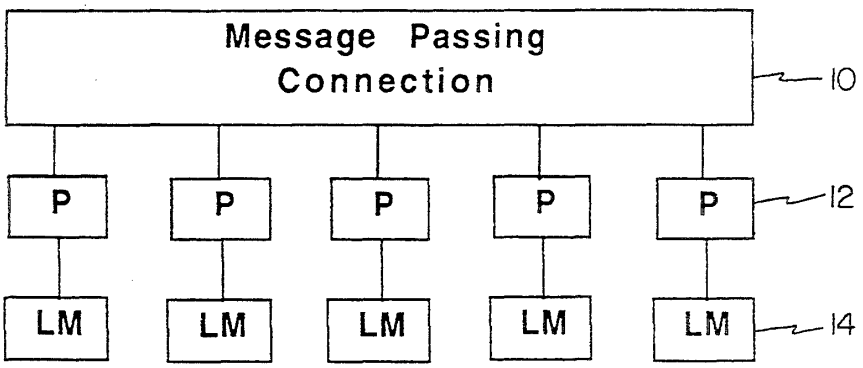
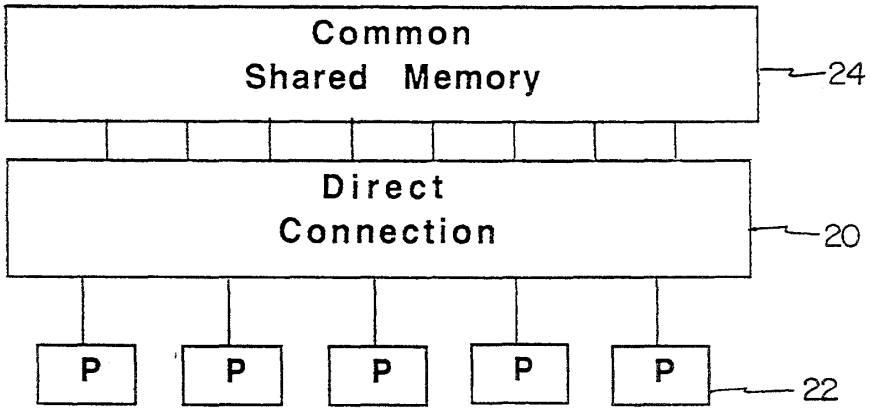


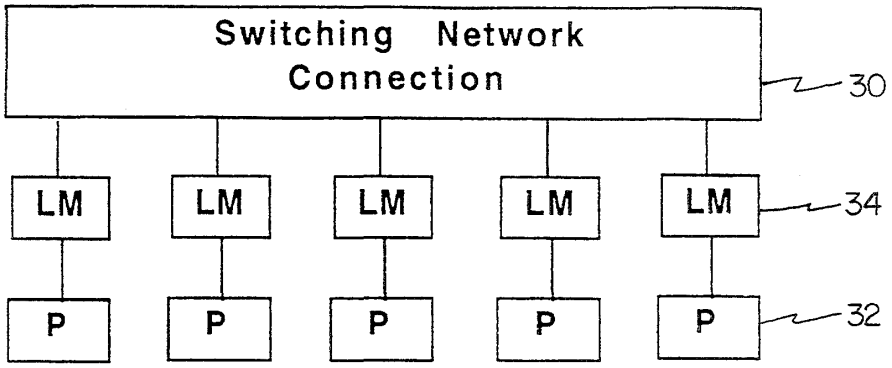
PRIOR ART
DISTRIBUTED MEMORY MODEL

Fig. 1a



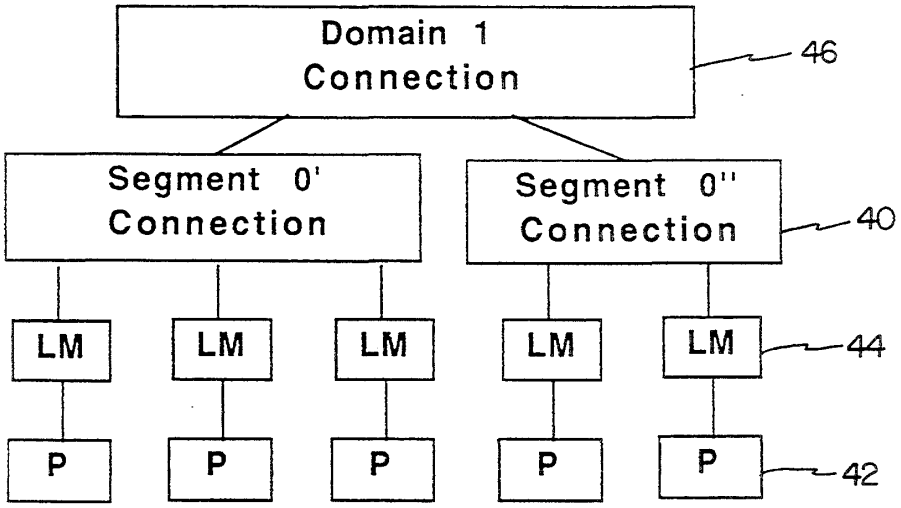
PRIOR ART
SHARED MEMORY MODEL

Fig. 1b



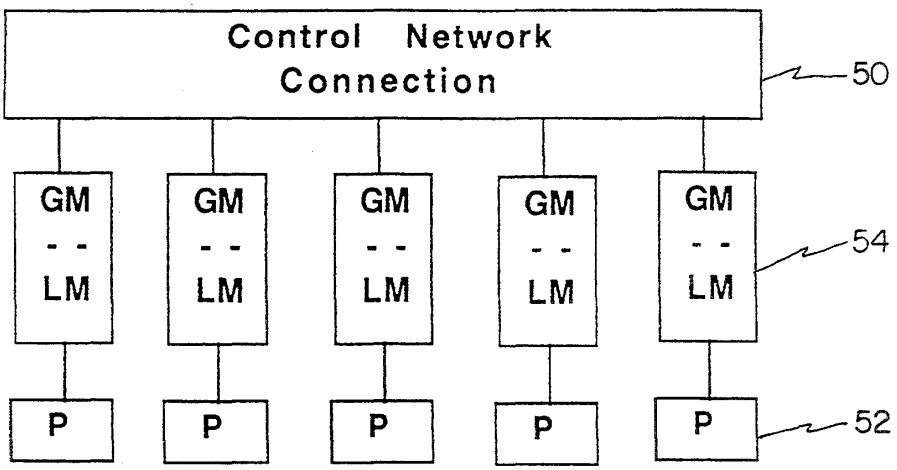
PRIOR ART
EXTENDED SHARED MEMORY
SWITCHING NETWORK MODEL

Fig. 2a



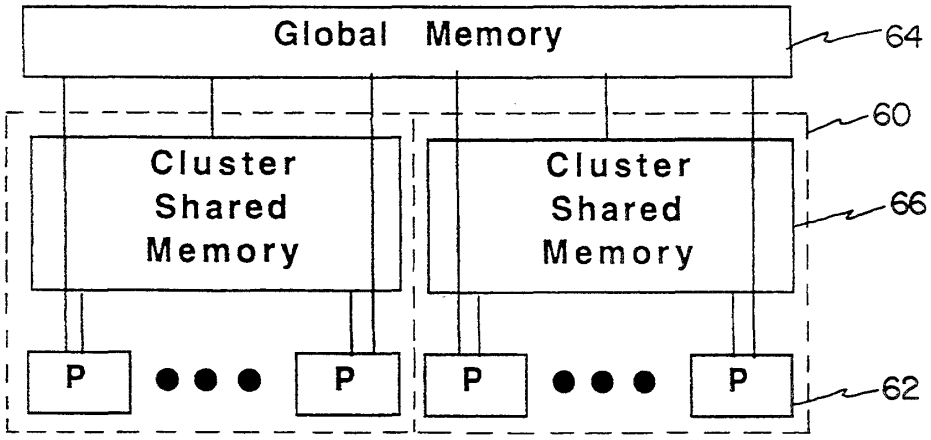
PRIOR ART
EXTENDED SHARED MEMORY
HEIRARCHICAL RING MODEL

Fig. 2b



PRIOR ART
EXTENDED SHARED MEMORY
RECONFIGURABLE MODEL

Fig. 2c



PRIOR ART
EXTENDED SHARED MEMORY
CLUSTER/GLOBAL MEMORY INTERCONNECT

Fig. 2d

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