



## 2.2MHz, 2A Buck Converters with an Integrated High-Side Switch

### General Description

The MAX5088/MAX5089 high-frequency, DC-DC converters with an integrated n-channel power MOSFET provide up to 2A of load current. The MAX5088 includes an internal power MOSFET to enable the design of a nonsynchronous buck topology power supply. The MAX5089 is for the design of a synchronous buck topology power supply. These devices operate from a 4.5V to 5.5V or 5.5V to 23V input voltage and a 200kHz to 2.2MHz resistor-programmable switching frequency. The voltage-mode architecture with a peak switch current-limit scheme provides stable operation up to a 2.2MHz switching frequency. The MAX5088 includes a clock output for driving a second DC-DC converter 180° out-of-phase and a power-on-reset (RESET) output. The MAX5089 includes a power-good output and a synchronous rectifier driver to drive an external low-side MOSFET in the buck converter configuration for high efficiency.

The MAX5088/MAX5089 protect against overcurrent conditions by utilizing a peak current limit as well as overtemperature shutdown providing a very reliable and compact power source for point-of-load regulation applications. Additional features include synchronization, internal digital soft-start, and an enable input. The MAX5088/MAX5089 are available in a thermally enhanced, space-saving 16-pin TQFN (5mm x 5mm) package and operate over the -40°C to +125°C temperature range.

### Applications

xDSL Modem Power Supply  
Automotive Radio Power Supply  
Servers and Networks  
IP Phones/WLAN Access Points

### Selector Guide

PART	CONFIGURATION	FEATURES
MAX5088ATE	Nonsynchronous Buck	RESET Output, Clock Output
MAX5089ATE	Synchronous Buck	PGOOD Output, Synchronous FET Driver

Pin Configurations continued at end of data sheet.



Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).

### Features

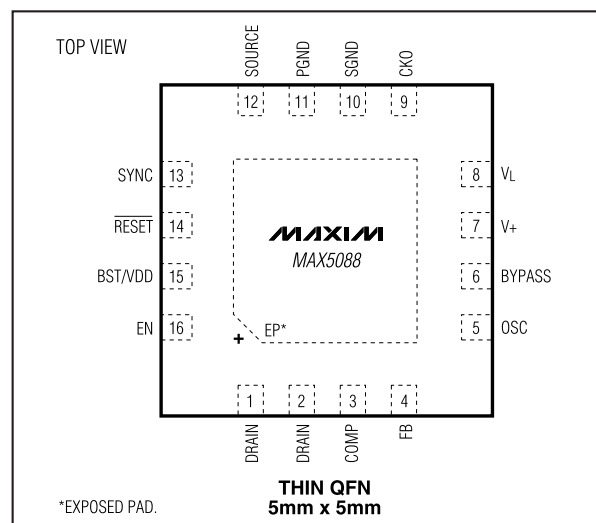
- ◆ 4.5V to 5.5V or 5.5V to 23V Input Voltage Range
- ◆ Output Voltage Adjustable Down to 0.6V
- ◆ 2A Output Current
- ◆ Synchronous Rectifier Driver Output (MAX5089) for Higher Efficiency
- ◆ Resistor-Programmable Switching Frequency from 200kHz to 2.2MHz
- ◆ External Synchronization and Enable (On/Off) Inputs
- ◆ Clock Output for Driving Second Converter 180° Out-Of-Phase (MAX5089)
- ◆ Integrated 150mΩ High-Side n-Channel Power MOSFET
- ◆ Power-On Reset Output (MAX5088)/Power-Good Output (MAX5089)
- ◆ Short-Circuit Protection
- ◆ Thermal-Shutdown Protection
- ◆ Thermally Enhanced 16-Pin TQFN Package Dissipates 2.7W

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5088ATE+	-40°C to +125°C	16 TQFN	T1655-2
MAX5089ATE+	-40°C to +125°C	16 TQFN	T1655-2

+Denotes lead-free package.

### Pin Configurations



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## ABSOLUTE MAXIMUM RATINGS

V+ to PGND .....-0.3V to +25V  
 BST/VDD, DRAIN to SGND .....-0.3V to +30V  
 SGND to PGND .....-0.3V to +0.3V  
 BST/VDD to SOURCE .....-0.3V to +6V  
 SOURCE to SGND .....-0.6V to +25V  
 SOURCE or DRAIN Maximum Peak Current .....5A for 1ms  
 VL to SGND .....-0.3V to the lower of +6V and (V+ + 0.3V)  
 SYNC, EN, DL, CKO, OSC, COMP,  
 FB to SGND .....-0.3V to (VL + 0.3V)  
 BYPASS, CKO, OSC, COMP, FB, EN, SYNC, RESET,  
 PGOOD Maximum Input Current .....±50mA

RESET, PGOOD to SGND .....-0.3V to +6V  
 BYPASS to SGND .....-0.3V to +2.2V  
 VL and BYPASS Short-Circuit Duration to SGND .....Continuous  
 Continuous Power Dissipation\* (TA = +70°C)  
 16-Pin TQFN (derate 33mW/°C above +70°C) .....2666mW  
 Package Thermal Resistance (junction to case) .....1.7°C/W  
 Operating Temperature Range .....-40°C to +125°C  
 Junction Temperature Range .....-65°C to +150°C  
 Storage Temperature Range .....-65°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C

\*As per JEDEC51 Standard (multilayer board).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V+ = VL = 5V or V+ = 5.5V to 23V, VEN = 5V, TA = TJ = -40°C to +125°C, unless otherwise noted. Circuits of Figures 5 and 6. Typical values are at TA = TJ = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SYSTEM SPECIFICATIONS</b>						
Input Voltage Range	V+		5.5		23.0	V
		V+ = VL	4.5		5.5	V
V+ Operating Supply Current	IQ	V+ = 12V, VFB = 0.8V ROSC = 10kΩ, no switching		1.8	2.5	mA
V+ Standby Supply Current	ISTBY	V+ = 12V, VEN = 0V, PGOOD (MAX5089), RESET, CKO unconnected (MAX5088), ROSC = 10kΩ		1	1.4	mA
Efficiency	η	Nonsynchronous (MAX5088), fsw = 1.25MHz, V+ = 12V, IOUT = 1.5A, VOUT = 3.3V		79		%
		Synchronous (MAX5089), fsw = 300kHz, V+ = 12V, IOUT = 1.5A, VOUT = 3.3V		90		
<b>VL REGULATOR (VL)/BYPASS OUTPUT (BYPASS)</b>						
VL Undervoltage Lockout	VUVLO	VL falling		4.1	4.3	V
VL Undervoltage Lockout Hysteresis	VHYST			137		mV
VL Output Voltage	VL	V+ = 5.5V to 23V, IVL = 0 to 40mA	5.0	5.2	5.5	V
BYPASS Output Voltage	VBYPASS	V+ = VL = 5.2V	1.98	2	2.02	V
BYPASS Load Regulation	ΔVBYPASS	IBYPASS steps from 0 to 50μA, V+ = VL = 5.2V	0	1.2	10	mV

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_+ = V_L = 5V$  or  $V_+ = 5.5V$  to  $23V$ ,  $V_{EN} = 5V$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Circuits of Figures 5 and 6. Typical values are at  $T_A = T_J = +25^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>SOFT-START</b>							
Digital Soft-Start Period		Internal 6-bit DAC		4096		Clock periods	
Soft-Start Steps				64		Steps	
<b>ERROR AMPLIFIER (FB and COMP)</b>							
FB to COMP Transconductance	gm		1.20	1.8	2.75	mS	
FB Input Bias Current	I <sub>FB</sub>				250	nA	
FB Input Voltage Set Point	V <sub>FB</sub>		0.5940	0.601	0.6095	V	
COMP Sink-and-Source Current Capability	I <sub>COMP</sub>		100	150		μA	
<b>INTERNAL MOSFETS</b>							
On-Resistance n-Channel Power MOSFET	R <sub>ON</sub>	$V_+ = V_L = 5.2V$ , I <sub>SINK</sub> = 100mA		0.150	0.302	Ω	
Leakage Current	I <sub>LEAK</sub>	$V_{EN} = 0V$ , $V_{DRAIN} = 23V$ , SOURCE = PGND			20	μA	
Minimum Output Current	I <sub>OUT</sub>	$V_{OUT} = 3.3V$ , $V_+ = 12V$ (Note 2)		2		A	
Current Limit	I <sub>LIMIT</sub>		2.2	2.8	3.5	A	
On-Resistance Internal Low-Side Switch	R <sub>ONLSW</sub>	I <sub>SWITCH</sub> = 50mA, $V_+ = V_L = 5.2V$		20	38	Ω	
<b>SYNCHRONOUS RECTIFIER DRIVER (DL) (MAX5089 Only)</b>							
On-Resistance nMOS	R <sub>ONDLN</sub>	I <sub>SINK</sub> = 0.1A		1	6.7	Ω	
On-Resistance pMOS	R <sub>ONDLP</sub>	I <sub>SOURCE</sub> = 0.1A		1.9	11.1	Ω	
Peak Sink Current	I <sub>IDL_SINK</sub>			1		A	
Peak Source Current	I <sub>IDL_SOURCE</sub>			0.75		A	
<b>OSCILLATOR (OSC)/SYNCHRONIZATION (SYNC)/CLOCK OUTPUT (CKO) (MAX5088 Only)</b>							
Clock Output-High Level	V <sub>CKOH</sub>	$V_L = 5.2V$ , I <sub>SOURCE</sub> = 5mA	3.54			V	
Clock Output-Low Level	V <sub>CKOL</sub>	$V_L = 5.2V$ , I <sub>SINK</sub> = 5mA			0.4	V	
Switching Frequency	f <sub>sw</sub>	$V_+ = V_L = 5.2V$	R <sub>OSC</sub> = 5.62kΩ	1900	2100	2400	kHz
			R <sub>OSC</sub> = 41.2kΩ	275	312	350	
			R <sub>OSC</sub> = 10kΩ	1130	1250	1380	
Minimum Controllable On-Time	t <sub>ON_MIN</sub>			120		ns	
Maximum Duty Cycle	D <sub>MAX</sub>	f <sub>sw</sub> = 2.2MHz	MAX5088	82	87.5	%	
			MAX5089	82	87.5		

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_+ = V_L = 5V$  or  $V_+ = 5.5V$  to  $23V$ ,  $V_{EN} = 5V$ ,  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Circuits of Figures 5 and 6. Typical values are at  $T_A = T_J = +25^\circ C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Frequency Range (Note 3)	$f_{SYNC}$		200		2200	kHz
Sync Input to SOURCE Rising-Edge Phase Delay (Note 4)	SYNC <sub>PHASE</sub>	$R_{OSC} = 10k\Omega$ , $f_{SYNC} = 1.2MHz$		65		degrees
Clock Output Phase Delay With Respect to SOURCE Waveform (Note 5)	CKO <sub>PHASE</sub>	$R_{OSC} = 10k\Omega$ , SYNC = GND (MAX5088 only)		115		degrees
SYNC High Threshold	$V_{SYNCH}$		2.0			V
SYNC Low Threshold	$V_{SYNCL}$				0.8	V
Minimum SYNC High Pulse Width	$t_{SYNC\_H}$			100		ns
<b>EN, RESET (MAX5088)/PGOOD (MAX5089)</b>						
EN Threshold	$V_{IH}$		2.0			V
	$V_{IL}$				0.8	
EN Input Bias Current	$I_{EN}$				250	nA
RESET Threshold (Note 6)	$V_{TH}$	$V_{FB} = V_{OUT}$	90	92.5	95	% $V_{OUT}$
PGOOD Threshold (Note 6)	$V_{TH}$	$V_{FB} = V_{OUT}$	90	92.5	95	% $V_{OUT}$
FB to RESET or FB to PGOOD Propagation Delay	$t_{FD}$			3		$\mu s$
RESET Active Timeout Period	$t_{RP}$		140	200	254	ms
RESET, PGOOD Output Voltage	$V_{OL}$	$I_{SINK} = 3mA$			0.4	V
RESET, PGOOD Output Leakage Current	$I_{LEAK}$	$V_+ = V_L = 5.2V$ , $V_{RESET}$ or $V_{PGOOD} = 6V$ , $V_{FB} = 0.8V$			2	$\mu A$
<b>THERMAL SHUTDOWN</b>						
Thermal Shutdown	$T_{SHDN}$	Temperature rising		+170		$^\circ C$
Thermal-Shutdown Hysteresis				25		$^\circ C$

**Note 1:** 100% tested at  $+125^\circ C$ . Limits over temperature are guaranteed by design.

**Note 2:** Output current may be limited by the power dissipation of the package. See the *Power Dissipation* section in the *Applications Information* section.

**Note 3:** SYNC input frequency is equal to the switching frequency.

**Note 4:** From the SYNC rising edge to SOURCE rising edge.

**Note 5:** From the rising edge of the SOURCE waveform to the rising edge of the CKO waveform.

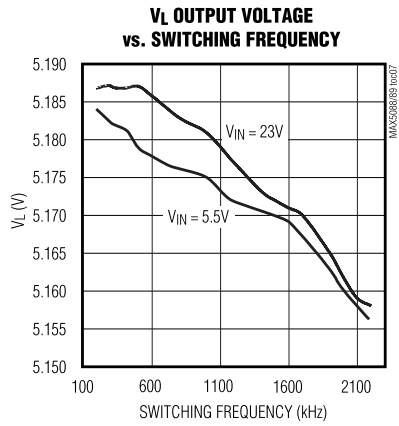
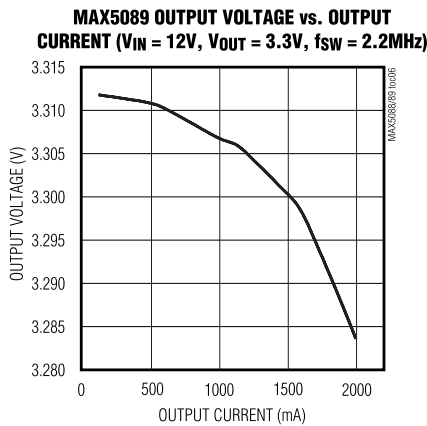
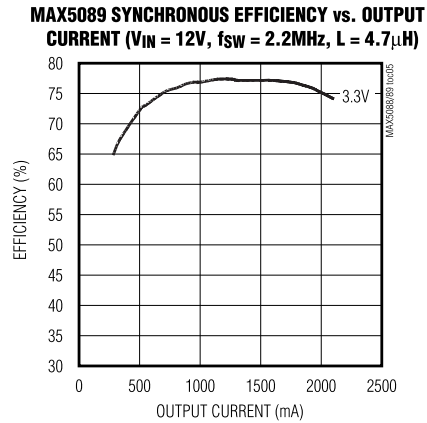
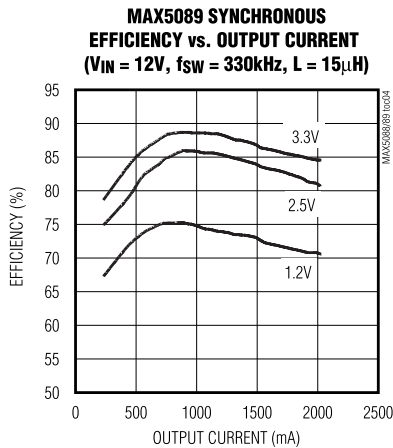
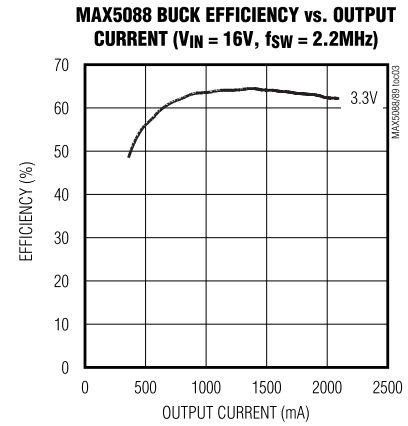
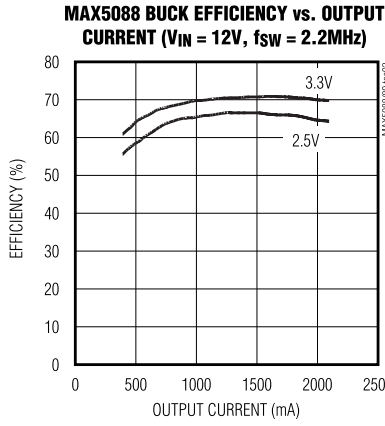
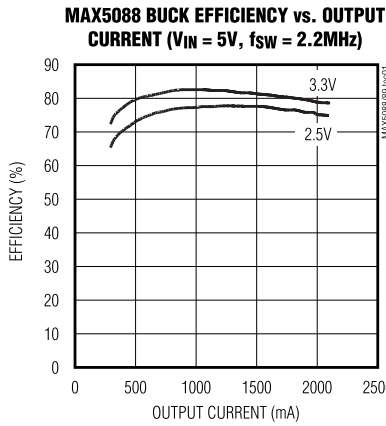
**Note 6:** RESET goes high 200ms after  $V_{OUT}$  crosses this threshold, PGOOD goes high after  $V_{OUT}$  crosses this threshold.

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## Typical Operating Characteristics

( $V_+ = V_L = 5.2V$ ,  $T_A = +25^\circ C$ , Figures 5 and 6, unless otherwise noted.)

MAX5088/MAX5089



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