Passive Cancellation of Common-Mode Electromagnetic Interference in Switching Power Converters

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Abstract

It is well known that common-mode (CM) conducted electromagnetic interference (EMI) is caused by the common-mode current flowing through the parasitic capacitance of transistors, diodes, and transformers to ground in the power circuit. Because of the potential for interference with other systems as well as governmental regulations, it is necessary to attenuate this noise. Ordinarily this must be accomplished by using a magnetic choke on the input power lines, which can result in large penalties to the overall size, weight, and cost of the completed system.

In order to lessen the requirement for this magnetic choke, there has been in recent years a desire to introduce noise cancellation techniques to the area of EMI. This text introduces a method of canceling the common-mode EMI by using a compensating transformer winding and a capacitor. Compared with active cancellation techniques, it is much simpler and requires no additional transistors and gate-drive circuitry since it merely adds a small copper winding and a small capacitor. By using this technique the size of the EMI filter can be reduced, especially for applications requiring high currents.

In this thesis a survey of CM noise reduction techniques is presented, encompassing conventional and active cancellation techniques. The new method for passive noise cancellation is presented, which is then applied to families of isolated DC/DC converters, non-isolated DC/DC converters, and DC/AC inverters and motor drives. The method, results, and ramifications of this technique are presented in order of appearance.

Acknowledgement

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Finally, I must thank my parents, Alan and Vivian Cochrane, for their love and support in my various endeavors throughout the years.

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Chapter 1. A Brief Overview of EMI

Before we look at the main topic of this thesis text, it is necessary to present some basic background information. This chapter briefly summarizes some of the most important topics of the field of EMI as they relate to this particular subject. Starting with the fundamental definitions, we will then look at some of the regulations pertaining to this subject before looking at the causes of noise.

1.1. What is EMI?

1.1.1. The Basics

What is EMI? Simply put, EMI, or electromagnetic interference, is undesirable noise that interferes with the normal operation of electronics. Michel Mardiguian puts it the following:

> "Generally, electromagnetic interference occurs when an electrical disturbance from either a natural phenomenon (e.g., electrostatic discharge [ESD], lightning, and so on) or an electrical or electronic equipment causes an undesired response in another equipment."[1]

Specifically, we can categorize EMI into four different groups:

1. Conducted emissions
2. Radiated emissions
3. Conducted susceptibility
4. Radiated susceptibility

The first two groups deal with the undesirable emanations from a particular piece of equipment, and the second two groups deal with a piece of equipment's ability to reject interference from external sources of noise. In this thesis I will be focusing on the first type of EMI: conducted emissions.

In practice this interference can have various degrees of manifestation ranging from nuisance, such as interference with a portable radio when walking under a power line, to catastrophic, such

[1] Mardiguian, pg 1

as an electronic communications device interfering with a aircraft navigation equipment[2]. Ott gives a diagram shown in Figure 1 that illustrates some of the myriad ways that EMI can be propagated.

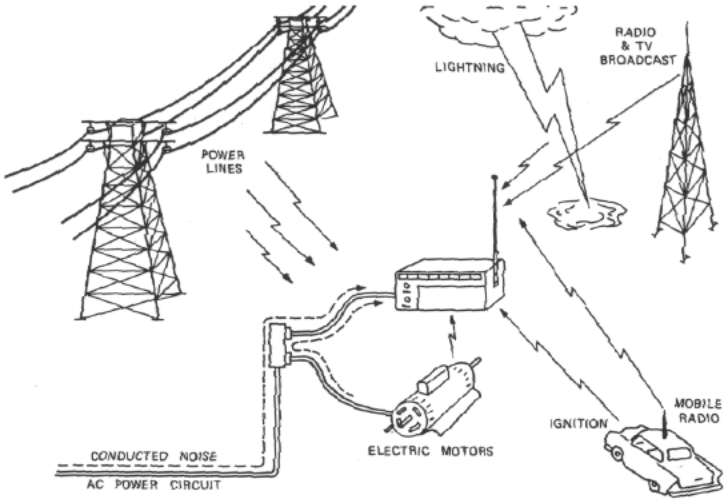

Figure 1: Examples of Conducted and Radiated EMI Propagation[3]

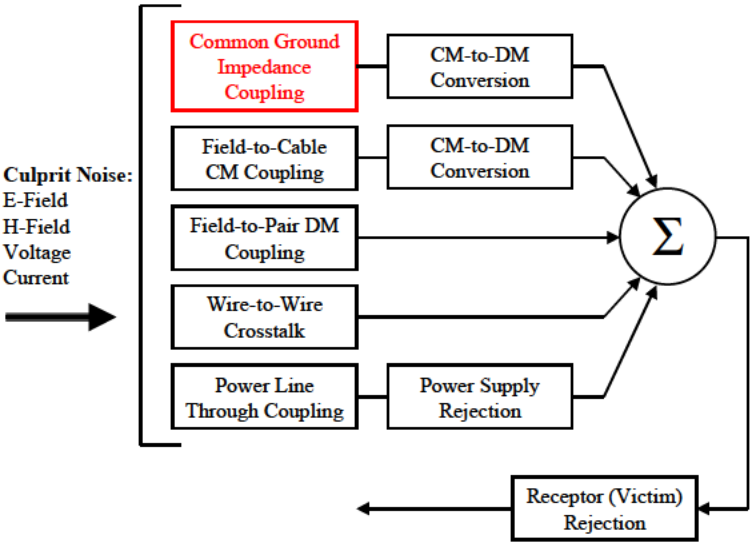

Figure 2: Flow Chart of Source to Victim Coupling Paths[4]

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[2] *CAA News*, referenced in bibliography, specifies several instances of cell phones triggering various system malfunctions in commercial aircraft.

[3] Ott, pg. 3

Figure 2 is a simple flow chart showing how the noise sources are coupled into a noise victim; this can be the system itself or some other nearby susceptible equipment. The particular method of coupling that this thesis will focus on eliminating is the highlighted box "Common Ground Impedance Coupling".

As electronic equipment has increased in popularity we have been seeing a great deal of interest in incorporating switch-mode power converters to reduce the size, weight, and cost of said equipment. In order to increase the performance and/or the efficiency of these power converters the switching frequency has been increasing with concomitant increases in the levels of EMI. Techniques of reducing this EMI by cheap and simple means should therefore be of great interest to persons involved in the design of switch-mode power conversion equipment.

1.1.2. Standards

Because of the difference in motivation between protecting the designer's product against susceptibility to other products emissions and protecting other products from emissions from the designer's product, various government bodies have instituted standards which set specific limits on the quantities of radiated and conducted noise emissions in order for a product to be sold within that country. In the United States these regulatory bodies are the Federal Communications Commission (FCC) and the Department of Defense (DOD). In Europe all standards are set by the European Economic Consortium (EEC). There is also an international body called the International Special Committee on Radio Interference (CISPR), a committee of the International Electrontechnical Commission (IEC), which has no regulatory authority but which sets standards that can then be adopted by individual nations in order to facilitate international trade. Table 1 summarizes these various standards.

Table 1: List of Common EMI Regulations

Standard	Description
FCC Part 15, Subpart J	FCC General standard for digital electronics
EN55011	EU standard for industrial, scientific, and medical equipment
EN55013	EU standard for broadcast receivers
EN55014	EU standard for motor and thermal appliances, and electrical tools
EN55015	EU standard for electrical lighting
EN55022	EU standard for information technology (IT) equipment
CISPR Publication 22	CISPR standards for digital electronics
MIL-STD-461E	DOD standards for electrical equipment

[4] Mardiguian, pg. 16

While all of the aforementioned standards include both conducted and radiated specifications as well as regulations concerning electromagnetic compatibility, only the conducted noise interference specifications will be discussed in this thesis in the interest of reducing extraneous noise. Figure 3 and Figure 4 (The EN standards follow CISPR specifications) compare the limits of each of these standards. The non-military specifications differentiate between types of electronic equipment; a Class A device is intended for use in commercial or industrial environments while a Class B device is intended for consumer applications[5]. Typically no military equipment is intended for use in consumer applications, so the military specification differentiates between equipment based on input voltage and adds special rules if the equipment is to be used in an electromagnetically sensitive environment such as that in a submarine or spacecraft.

The most important difference between all of these specifications is the frequency band that they cover. The CISPR and the EU regulations specify a bandwidth of 150 kHz-30 MHz, while the FCC is more lax in calling for a starting frequency of 450 kHz. MIL-STD-461E is much stricter on the low frequency side (10 kHz), although the high side of the specification only goes to 10 MHz. What this translates into is that the corner frequency of the input EMI filter will have to be lowered for the stricter standards, which can mean a considerable increase in the size and cost of the compliant system. Naturally this also increases the motivation for eliminating the EMI by techniques other than filtering.

[5] Ott, pg 8

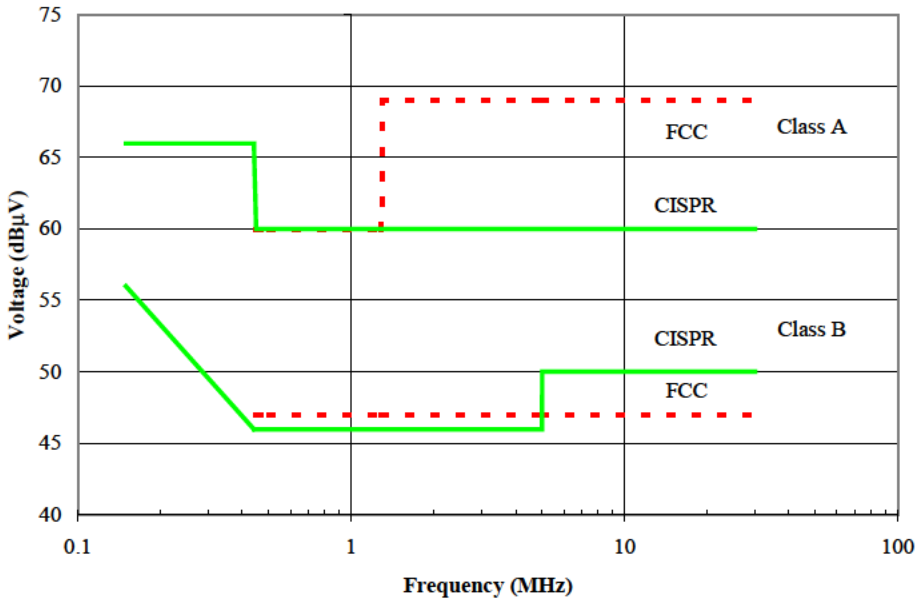

Figure 3: Comparison of Conducted Emissions Limits for FCC Part 15, Subpart J and CISPR, Publication 22[6]

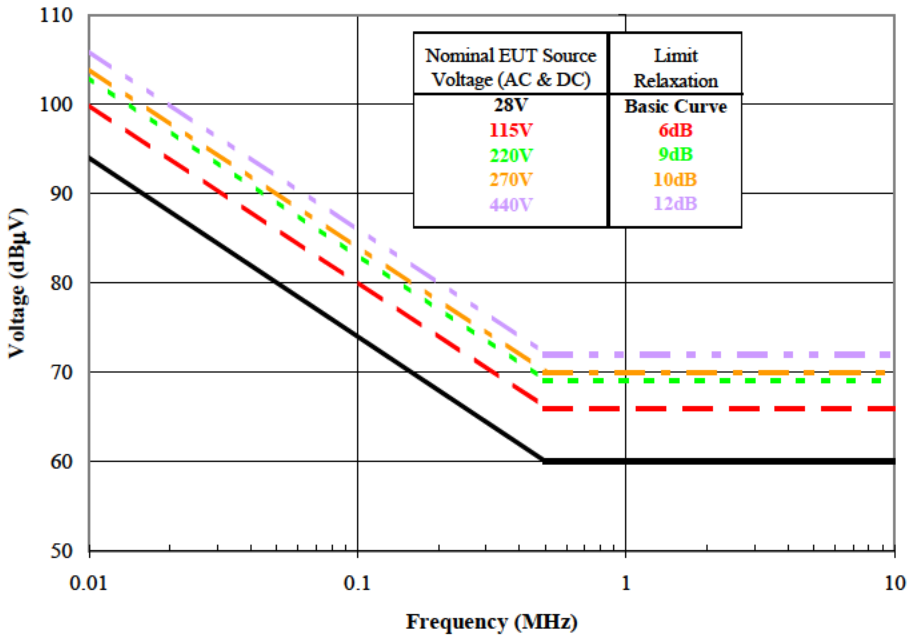

Figure 4: MIL-STD-461E Conducted EMI Limits, CE102[7]

[6] Ibid., pg. 15

[7] MIL-STD-461E, pg. 38

1.1.3. Testing

Each regulatory body has a specific standard of performing EMI tests. Figure 5 shows the conducted emission test setup for MIL-STD-461E by means of example. The equipment under test (EUT) is placed on a copper ground plane that is electrically isolated from the surrounding area. Power leads to the EUT have a Line Impedance Stabilization Network (LISN) placed in series to provide a common power line impedance over the frequency of interest. The LISN also serves as the measurement point for the conducted mode testing, as shown in the MIL-STD-461E, CE102 measurement setup in Figure 6.

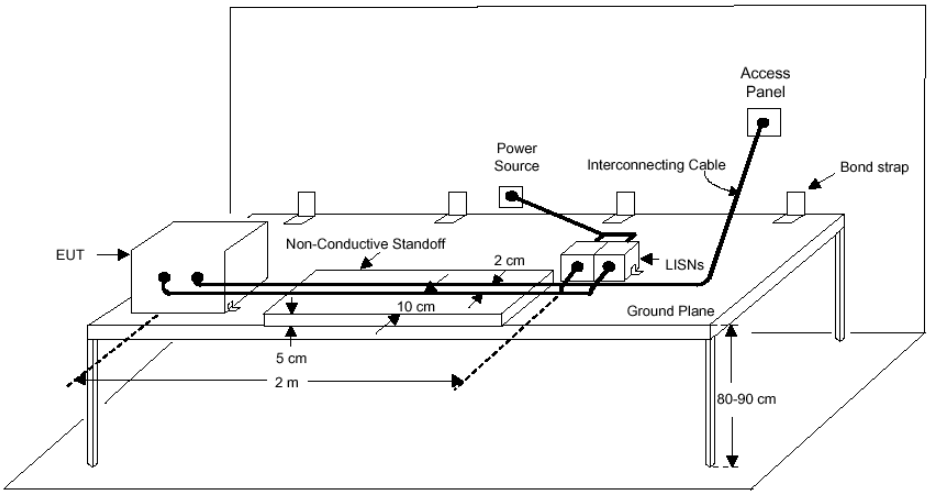

Figure 5: MIL-STD-461E Conducted Emissions Test Setup[8]

[8] MIL-STD-461E, pg. 19

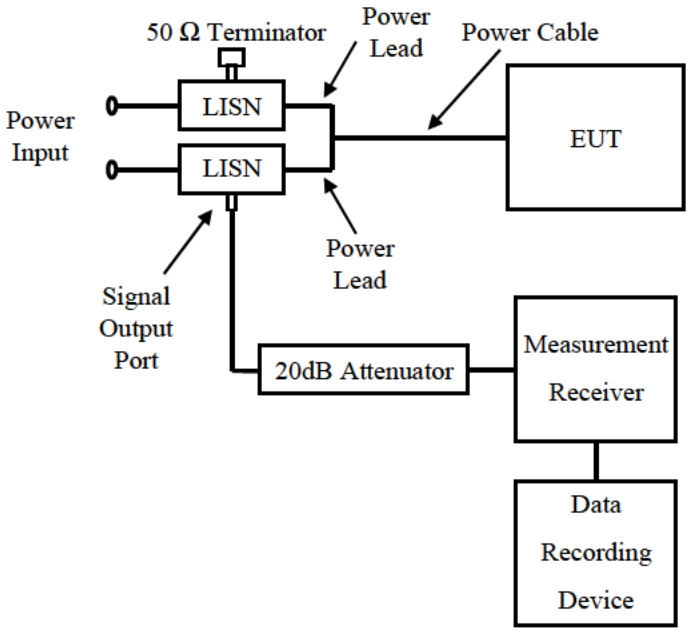

Figure 6: MIL-STD-461E, CE102 Measurement Setup[9]

As stated before, the purpose of the LISN is to provide a common 50 Ω line impedance for comparing test results. However, this 50 Ω impedance is only specified of the frequencies to be tested for noise. This means that for practical purposes, different LISNs must be used for different regulations testing. Figure 7 give the schematics of the LISNs used for FCC and MIL-STD-461E testing. Figure 8 compares their impedances. It is obvious that the typical LISN will give good results for the FCC test that starts at 450 kHz, but the system designer should be aware of the limitations of the -461E LISN. The 10 kHz—500 kHz portion of the CE102 test will have a much lower impedance than the higher frequencies. This can possibly create issues with an input filter (See Section 2.1) designed for the larger line impedance. Of course, these problems will be magnified if the wrong LISN is used, since the typical LISN drops to slightly less than 1 Ω at low frequency versus 5 Ω for the –461E LISN.

[9] Ibid., pg. 40

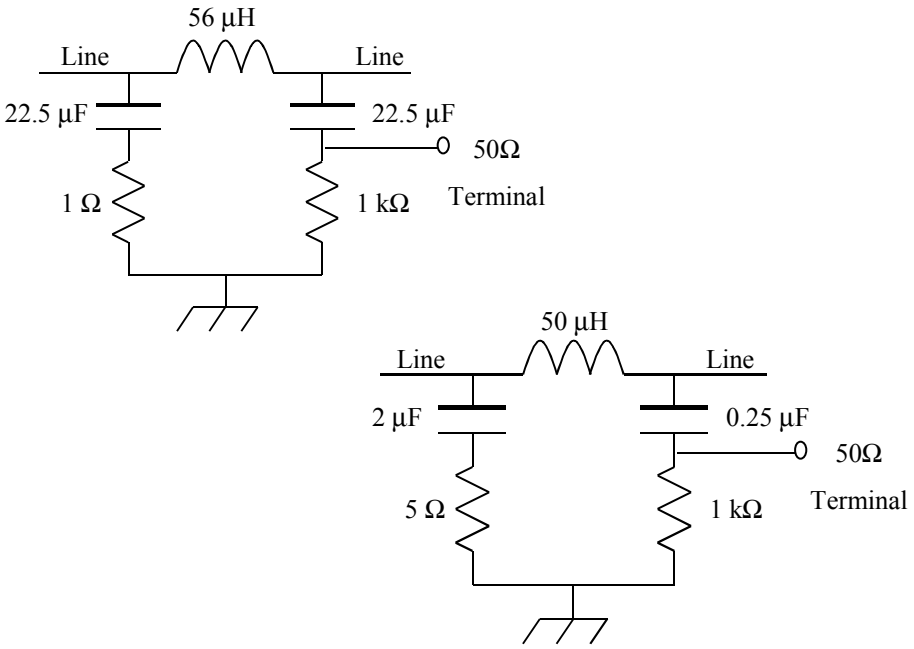

Figure 7: Typical and MIL-STD-461E LISN[10]

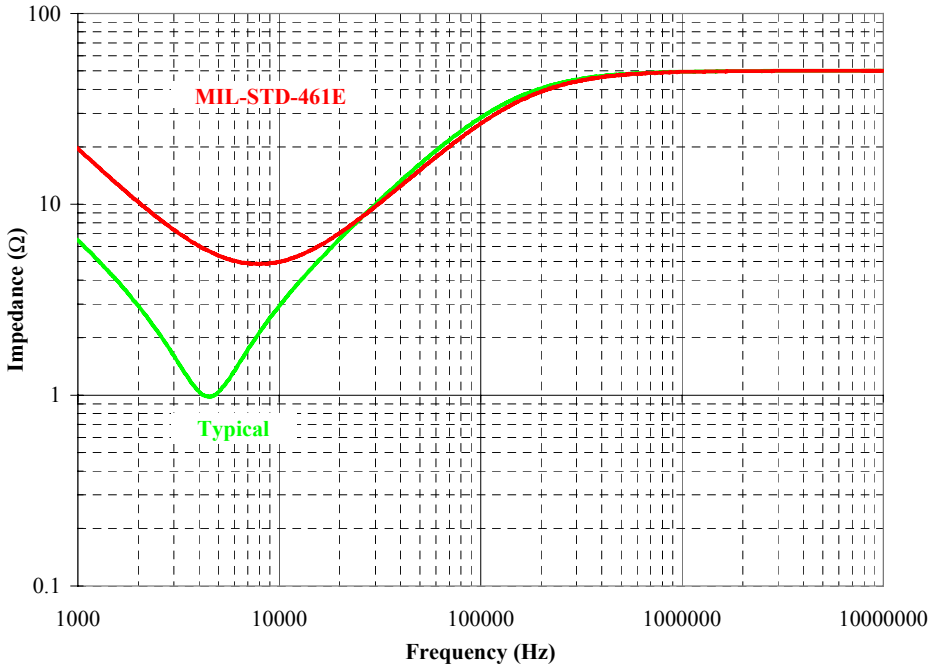

Figure 8: LISN Impedance Comparison

[10] Ozenbaugh, pg. 23

1.2. Sources and Traps

1.2.1. Active Components

Any power electronics switch will be a noise source due to parasitics in the device packaging. There will be a parasitic inductance L_P from the package leads, and there will be a parasitic capacitance C_P due to the thermal management (heat sink) used to protect the device. Figure 9 illustrates this.

The parasitic L_P causes high frequency ringing in the voltage waveform across the switch due to $L_P {}^{di}/_{dt}$. This has the effect of both increasing the stress on the switch as well as serving as a source of DM noise current from the interaction of the high frequency voltage components with the Miller capacitances of the switch.

The voltage waveform that develops between the device and ground will interact with the parasitic C_P to create CM noise currents that will flow into the ground plane. This parasitic is the focus of this thesis. Naturally if the heat sink can be floated the noise will be eliminated, but this raises safety issues and in any event may not be possible due to mechanical considerations.

In addition to the packaging parasitics, there will also be noise sources related to the device physics. Effects such as diode reverse-recovery can create additional high-frequency noise as well as increased switching stresses. These high-frequency effects, are outside the bounds of this thesis, however, and will not be discussed in detail.

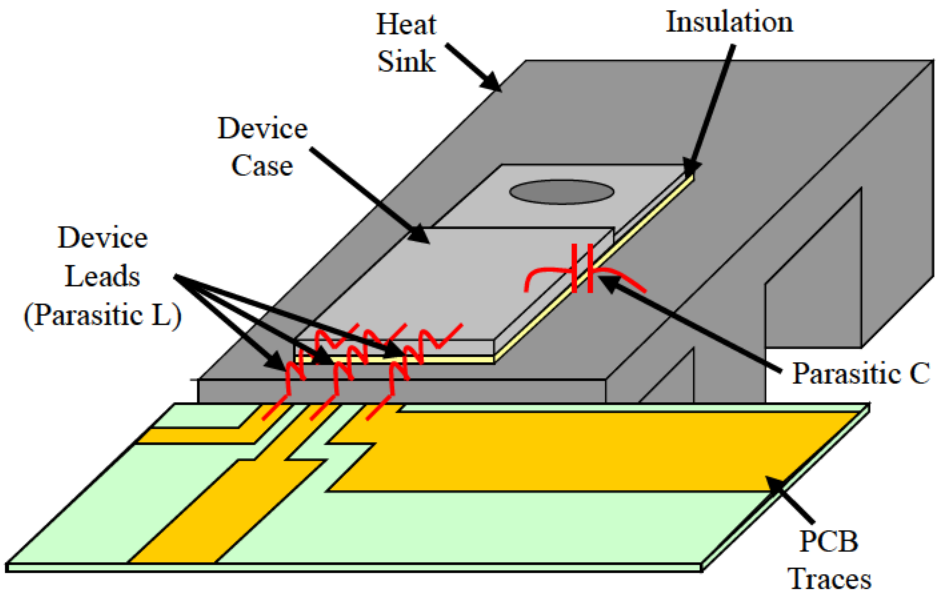

Figure 9: Packaging Parasitics for Active Device

1.2.2. Passive Components

Perhaps the chief source of CM EMI, apart from the active components described above, is the isolation transformer. More specifically, it is the cross-coupling capacitance between the windings that serves as a path for CM noise to flow through the system. Figure 10 shows a simple two-winding transformer with the following major parasitic components: leakage inductance L_k, interwinding capacitance C_R, and cross-coupling capacitance C_T. This capacitance can be minimized by separating the windings (increasing the leakage flux) or by using a Faraday shield in the construction of the transformer. The Faraday shield is simply an isolated section of aluminum or copper foil that is wrapped between the primary and secondary windings and then connected to ground.

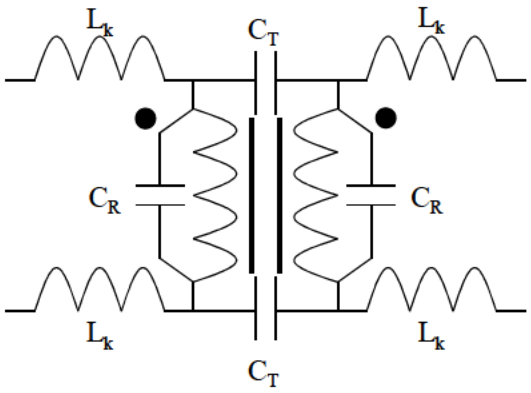

Figure 10: Transformer with Lumped Reactive Parasitics

Another important source of common-mode noise is the winding to frame capacitance in an electric machine. This capacitance can be quite significant for large machines, and will result in large leakage currents flowing back into the utility interface and/or interfering with the motor current control and ground-fault interrupt breakers. In addition to the possible external interference, there has also been some discussion related to reduced reliability of motor roller bearings due to the electrical breakdown of the of the lubricating film by common-mode noise currents.[11]

Of course, there are also the parasitics present in any resistor, capacitor, or inductor that will serve to limit the upper operating frequency of the element. A capacitor is limited by the inductance of its leads while the inductor is limited by its interwinding capacitance. Inductors have the additional problem of stray magnetic fields causing radiated noise. These fields are caused by leakage flux that is not contained in the core. Resistors will have stray inductance and/or capacitance depending on the method of manufacture (wirewound, film, or composition).[12]

1.2.3. Layout

Control of the radiated EMI is normally emphasized in the layout. However, one must also be aware of all the coupling capacitances between cables, buses, and the mechanical assemblies that provide a potential path to the ground plane. For example, the parasitic capacitance between the transistor and its heat sink may not be an issue if the capacitive coupling between the heat sink

[11] A detailed description of this phenomenon is given by Busse, referenced in bibliography.

[12] Ott, pg. 146

and the chassis is minimized. This may not be possible if the heat sink requires forced-air cooling, because the coupling between the heat sink and a nearby fan may by quite significant.

Chapter 2. Existing EMI Reduction Techniques

In the following chapter several means of dealing with common-mode noise are presented, starting with conventional CM EMI reduction techniques then moving into some previously proposed active noise cancellation methods. The final part of the chapter presents the principles of the proposed new method of passive cancellation.

2.1. Conventional Methods

One way to reduce EMI is to reduce the $^{dv}/_{dt}$ and $^{di}/_{dt}$ of the switches. This can be accomplished by changing the gate drive circuitry of the switches or by incorporating snubbers into the topology. These techniques have the advantage of reducing the noise created, but there is the very important downside of increased power dissipation in the switches that may require additional derating (larger devices) and in any event may reduce system efficiency below what can be tolerated. Snubbers are typically also dissipative themselves and will therefore noticeably reduce the overall efficiency as well as increase the system size and complexity. As the rated power of the system is increased the penalty of these options become increasingly intolerable.

When other methods of reducing conducted noise have been exhausted, the brute-force method is to use a line filter at the utility interface of the system. In practice the incorporation of these filters are practically unavoidable if EMI regulations are to be complied with. Normally these filters are composed solely of passive components in a low-pass filter configuration. Figure 11 shows a typical topology along with the equivalent CM and DM circuits. The design of the filter is accomplished by means of a noise separator[13] to isolate the CM and DM noise spectrum and then designing the filter using the individual equivalent circuits[14].The differential capacitors C_X act to short circuit differential noise currents, while the line-to-ground capacitors C_Y short circuit the common-mode noise currents. The CM choke L_{CM} is created by winding two identical coils in the same direction on a single magnetic core. If a tight magnetic coupling is maintained between the two coils the leakage inductance is minimized and there will be little differential impedance seen at line frequencies. The CM choke therefore presents a high impedance to only the common-

[13] See Ting Guo

[14] Fu-Yuan Shih develops the design methodology in detail. Note that this technique is only applicable to the topology presented in the paper and in Figure 11. A more generalized approach can be found Richard Ozenbaugh's book *EMI Filter Design*.

mode noise currents, which allows the filter as a whole to minimize interference with the desired power line frequency. The downside to this is that the filter inductors must carry the full power current, which results in components that are large and expensive.

In conclusion to this section, EMI filters are a very effective method of attenuating conducted emissions but this can be a very expensive solution to the noise problem. It will therefore be greatly beneficial to look for other ways in which conducted interference can be cheaply reduced, therefore reducing the size and cost of the filter.

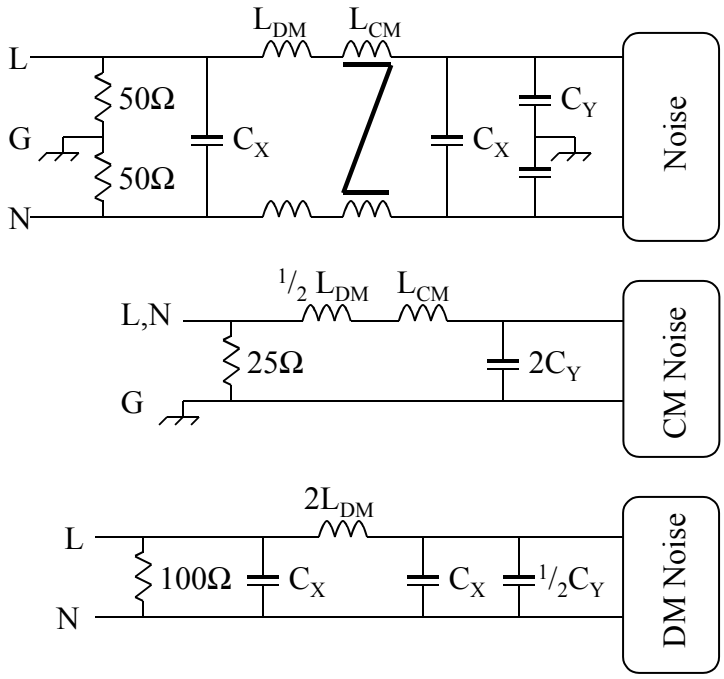

Figure 11: Typical EMI Line Filter Topology Incorporating CM and DM Components[15]

2.2. Active Cancellation

Recently there have been a number of articles dealing with methods of active common-mode cancellation. The principle behind the first group of these techniques is to vary the modulation scheme so that the circuit remains balanced at all times. All of the techniques in this first group have been proposed by A. Julian and others at the University of Wisconsin-Madison. For the three-phase voltage-source-inverter (VSI) in Figure 12 the CM voltage is given by $V_{CM} = \frac{V_1 + V_2 + V_3}{3}$, therefore the object of the modulation scheme should be to maintain

[15] Shih, pg 171.

$V_1 + V_2 + V_3 = 0$ at all times. Normally this requires that additional switches must be added to the circuit. For the case of the VSI in Figure 12 this modulation strategy requires that a fourth phase leg must be incorporated into the topology, although this leg can be derated with respect to the other phase legs so long as a balanced load is present. The modulation scheme can then achieve zero common-mode voltage by ensuring that two top switches and two bottom switches are on at all times, so that $V_1 + V_2 + V_3 + V_4 = 0$. In practice this will result in approximately 20 dBV[16] of reduction in the voltage across the ground conductor compared to the original three-phase VSI. The drawback to this scheme, other than the need for additional switches and gate drives, is that current ripple is increased and output DM waveform shaping is deteriorated.[17]

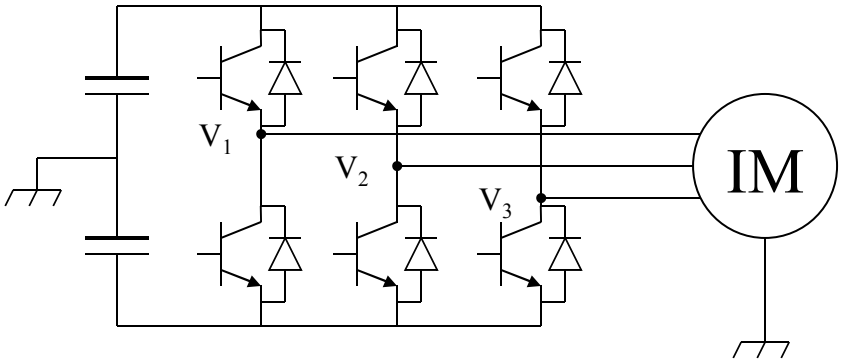

Figure 12: Typical Three-Phase Voltage Source Inverter

[16] A. Julian, pg. 986

[17] P. Ide, pg. 202

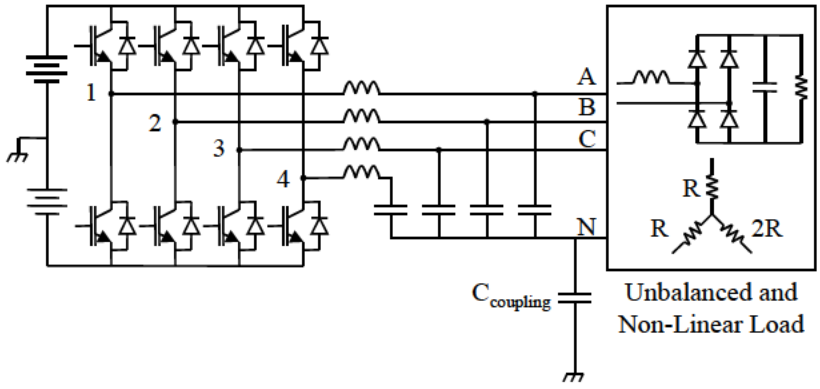

Figure 13: 3-Phase 4-Leg VSI with Active CM Filter[18]

Zhihong Ye recently proposed a method for reducing the common-mode emissions of a three-phase, 4 leg inverter. The fourth leg is normally used in this application to mitigate the magnitude of the neutral wire current due to unbalanced and/or non-linear loads that can occur in applications such as shipboard avionics support. In this case the modification involved the addition of a series capacitor to the neutral leg and the modification of the *o* channel control design (The *d* and *q* channels are independent of the *o* channel and can remain unchanged). This topology change and control methodology has the advantage of being able to reduce both CM high-frequency components and the low frequency components that are present for unbalanced and non-linear loads. The disadvantages to this technique is that it reduces the maximum modulation index from M = 1 to M = 0.866, requiring a higher DC bus voltage for the same output voltage. It also doubles the magnitude of the DM current ripple, which will require a larger DM filter to meet the ripple specifications of the inverter design.

[18] Z. Ye, pg. 1

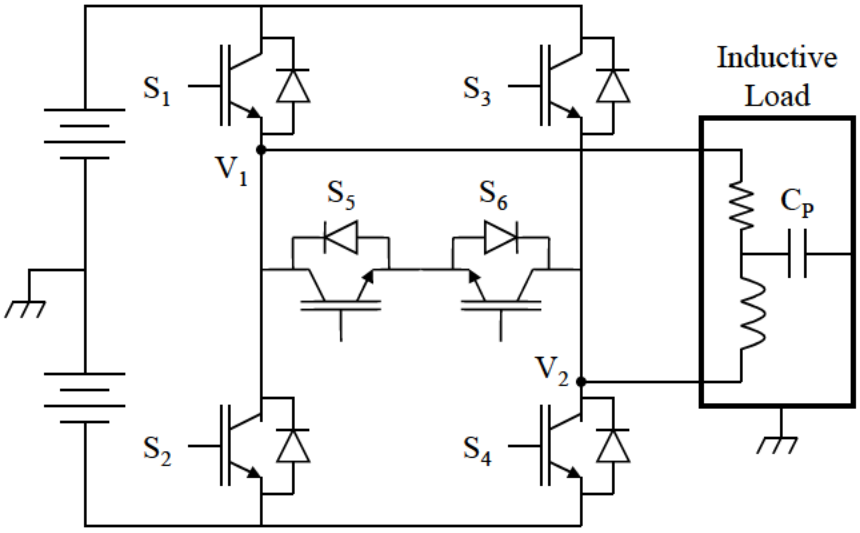

Figure 14: Single-Phase Inverter with Active CM Voltage Cancellation[19]

The single-phase inverter in Figure 14 achieves common-mode cancellation by the addition of the switches S_5 and S_6 to form a bi-directional device. Since the common-mode voltage is applied to the parasitic capacitance C_P during the zero switching states when the diodes in the phase legs (S_1 through S_4) freewheel. In this modified topology, S_5 and S_6 are turned on during the freewheeling period drive this common-mode voltage to zero (In practice this is roughly 20 dBμV measured across a LISN). The voltage rating of the added switches is the same as those in the phase legs, but the required current rating is approximately ½.

Figure 15 is an example of a buck converter topology that has been balanced to realize common-mode noise cancellation by using a split-winding inductor and an additional switch in addition to a bipolar source. The control scheme remains identical to the unmodified topology, and the net change in MOSFET costs is reduced since the voltage rating of the individual switches is halved[20]. The main difficulty is the need for a bipolar supply as this may require modifications to the overall power conversion system.

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[19] A. Rao, pg. 1

[20] A. Rockhill notes in his paper that the cost of a 500V MOSFET is approximately one-third of a 1000V device.

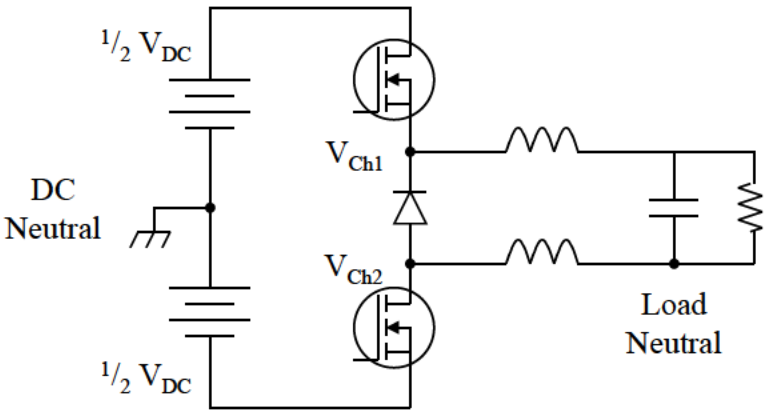

Figure 15: Balanced Buck Converter Topology[21]

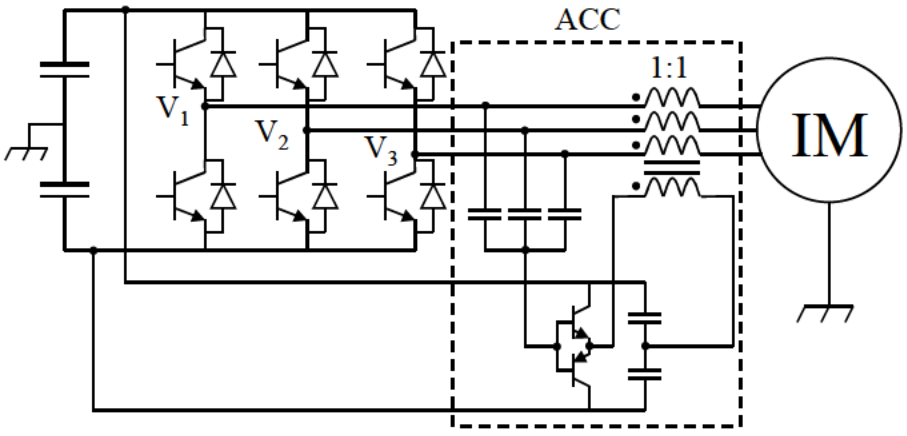

Figure 16: Auxiliary Active Circuit for CM Voltage Cancellation[22]

[21] A. Rockhill, pg. 940

[22] S. Ogasawara, "An Active Circuit for Cancellation…"pg. 836

The final example of active noise cancellation is the active common-noise canceler (ACC) proposed by S. Ogasawara in Figure 16. This technique as proposed only mitigates the CM noise applied to the motor load to increase motor reliability and reduce the electric shock hazard caused by excess ground current. Although not expressly worked out, it would not be difficult to extend this auxiliary circuit to the line filter choke to eliminate the CM voltage seen at the LISN.

The operation of the ACC is as follows: The three capacitors on the inverter output serve to detect a CM voltage, which is then passed through the push-pull amplifier and applied across the CM transformer (choke with added winding) to cancel the original CM voltage. The two capacitors across the amplifier prevent a DC current from flowing in the added winding of the transformer. Experimental results show a reduction of approximately 15 dBμV.[23] The drawback of this method, apart from the need for a CM choke that can handle the rated current of the inverter, is the power dissipation in the linear amplifier. This is given by the equation $P_D = \frac{V_{DC}^2}{64 \cdot L_M \cdot f_{SW}}$ [24], where V_{DC} is the DC link voltage, L_M is the magnetizing inductance of the CM choke, and f_{SW} is the switching frequency of the inverter. It is clear that one has a tradeoff between either a large choke or large transistors.

2.3. Passive Cancellation

Passive noise cancellation techniques are not typically considered, because the general perception is that an active technique will always be more flexible and yield better performance. This may be a true statement in many areas of electronics, but there are still cases where a passive solution can yield simpler, cheaper, and better results than an active solution.

A search of the existing literature yields a few papers dealing with passive cancellation; the one that is discussed here is proposed[25] by S. Ogasawara, which involves a CM choke that has an added winding whose terminals are shorted by a resistor. If an appropriate value of resistance is chosen then the magnitude of the motor leakage current can be reduced by a factor of $^1/_4$ to $^1/_3$. The addition of this circuit can also reduce the required size of the CM choke by approximately $^1/_3$.

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[23] Ibid. pg. 838

[24] Ibid. pg. 837

[25] S. Ogasawara, "Modeling and Damping of High-Frequency Currents…"

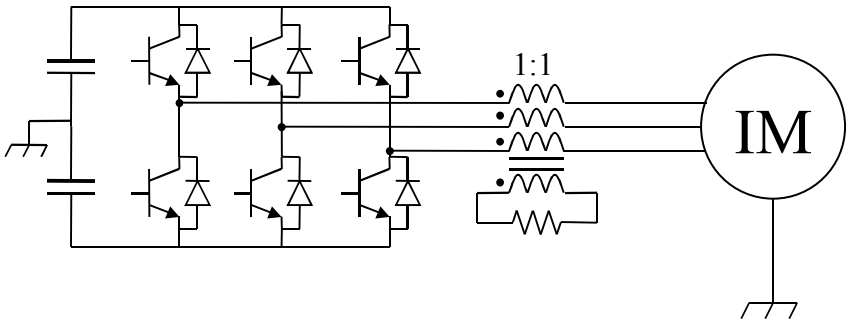

Figure 17: CM Transformer for Damping of Noise Currents[26]

2.4. Remarks

There are a number of limitations to the presented methods of noise cancellation. With the active techniques there is first and foremost the added cost of additional power switching modules and their associated gate drives and control circuits. Furthermore other design considerations may preclude the choice of an EMI-friendly modulation scheme. The passive technique presented immediately above demands the full current rating of the converter since it is based on the CM choke. While this technique may be useful if a choke is already present, it is unlikely to be looked upon favorably in a clean-sheet design, especially so given the relatively small reduction in noise currents.

Because of this it would be of some usefulness to have another option. This would be something small and simple that can be easily incorporated into an existing product or design and still allows the designer full freedom to use any desired method of control for the main power circuitry. This also means that the noise cancellation circuitry should be in shunt with the primary power flow to ensure a small size. It is with these motivations in mind that the new passive cancellation technique is presented and applied in the remaining part of this thesis.

[26] Ibid. pg. 1109

Chapter 3. Proposed Passive Cancellation in Isolated DC/DC Converters

In the following chapter we will look at how common-mode cancellation can be applied to some common isolated power converter topologies. This will be broken up into two sections dealing with buck-derived converters and buck-boost-derived converters. Boost-derived converters will not be discussed since they are not commonly used, although this should not be taken to say that the techniques discussed herein are not applicable to those topologies.

3.1. Introduction to the Proposed Technique

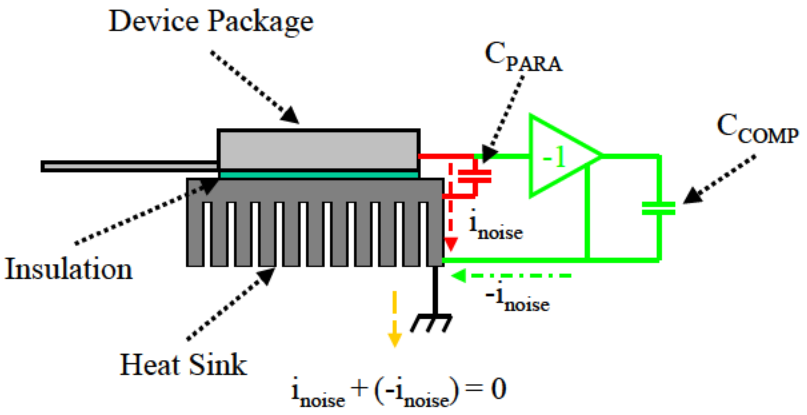

Figure 18: Proposed Method of CM Noise Cancellation

Figure 18 shows the essential concept behind the new method of common-mode noise cancellation. The device $^{dv}/_{dt}$ across the parasitic capacitance between the package and the heat sink causes a noise current to flow into the ground plane, as described in the previous chapter. Noise cancellation compensates for this noise current by sensing the device $^{dv}/_{dt}$, reversing it, and then applying it across a compensating capacitor. This causes a new current of equal magnitude and phase shifted by 180° to that of the noise current to flow into the ground plane. These two currents then sum to zero by Kirschoff's Current Law and the common-mode noise voltage across

the 50 Ω LISN resistor will be greatly attenuated. Note that this differs from the previously described methods in that it targets the noise currents rather than the overall CM voltage.

This effect can also be explained in terms of energy transfer. What happens is that the noise compensator demands energy at precisely the instant that the noise source pushes energy into the ground plane. Obviously this means that timing is critical for this to work, which means that the practical compensation circuit must contain circuitry with minimal propagation delay.

The other critical parameters that must be taken into account are the required voltage and current ratings. The voltage rating comes from the voltage seen across the switching device, and the current rating comes from the magnitude of canceling current that the noise compensator must push into the ground plane. These two parameters eliminate digital and signal-level analog devices from use in the noise compensator. While voltage sensors can reduce the voltage seen by the compensator, there are at present no cheap integrated analog or digital solutions that can push the required amounts of peak current that the noise compensator requires.

While common op-amps and digital electronics will not work for this application, magnetics can fill the job with very little difficulty. In the remaining portion of this thesis this will be explained further, but under most circumstances a small transformer using a cheap ferrite core will realize excellent results. This solution has the advantage of needing no control or auxiliary power circuitry, which yields a very simple and compact method of eliminating noise that is completely independent of the operation of the rest of the power conversion system.

3.2. Buck Derived Converters

3.2.1. Half-Bridge DC/DC

3.2.1.1. General Description

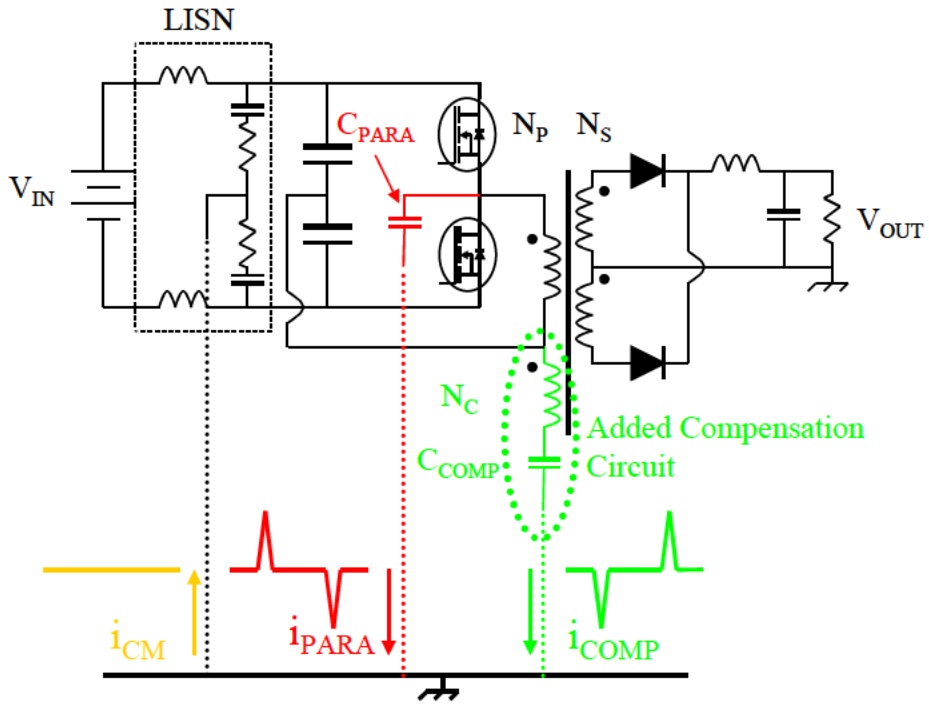

Figure 19: Half-Bridge Isolated DC/DC Topology Incorporating Passive Cancellation

Figure 19 shows how the well known half-bridge isolated topology can be modified to incorporate common-mode cancellation. Shown here is a ground plane into which are injected the parasitic $^{dv}/_{dt}$ currents (in red) from the switching elements, and the anti-noise currents (in green) injected by the added compensation circuit. In an ideal situation these two currents will then sum to zero, resulting in a much reduced common-mode current flowing into the LISN resistors. By utilizing the existing power transformer in the circuit, an additional winding N_C can be incorporated into the winding structure. Since N_C only needs to carry the anti-noise current created by C_{COMP}, it can use much smaller wire than that used by the main primary and secondary windings N_P and N_S. In practice this will be #30 AWG wire or larger depending on the mechanical considerations of the particular design. The other added component is the compensation capacitor C_{COMP}. This is used to generate the anti-noise current that will cancel out the parasitic noise current generated by C_{PARA}. The value of C_{COMP} is determined by the size of

C_{PARA} and the turns ratio N_P:N_C. If this ratio is 1:1 then C_{COMP} should be set equal to C_{PARA}; otherwise it should be sized such that $i_{COMP} = C_{PARA} \cdot {}^{dV}/_{dt}$.

3.2.1.2. Construction of Prototype

In order to test this compensation technique, a simple prototype was constructed with the parameters of Table 2. The overhead view of the completed prototype can be seen in Figure 19. The transistor C_{PARA} was measured to be 70 pF using a HP4194 impedance analyzer on the Cs-Rs setting by taking a mean value between 100 kHz and 1 MHz.

Table 2: Design Details of Half-Bridge Prototype

Input Voltage	100 V_{DC}
Output Voltage	3.3 V
Output Current (max)	10 A
Frequency	110 kHz
Turns Ratio (Pri:Com:Sec)	5:5:1
Bridge MOSFET	IRFP350
Bridge Diodes	31DF2
Output Rectifier Diodes	30CPQ050
Controller	UC2526A
Driver	IR2110
Output Inductor	65 µH
Output Capacitors	68 µF
Input Capacitors	47 µF

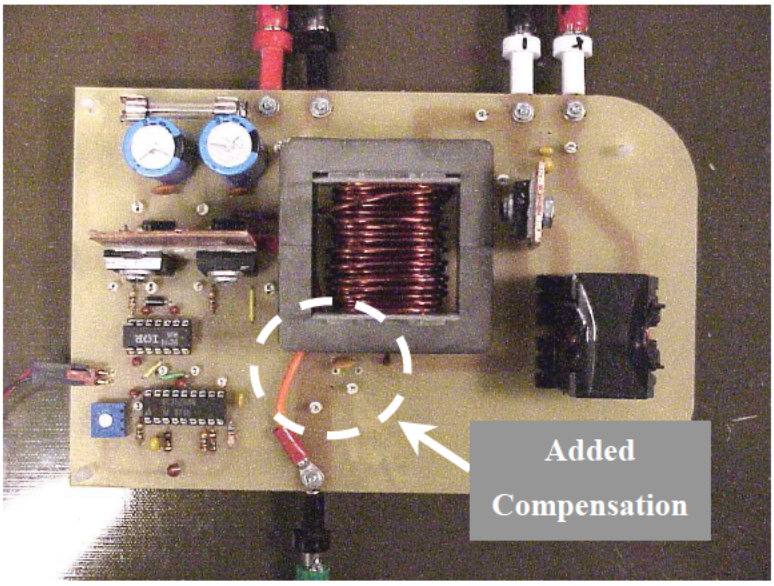

Figure 20: Half-Bridge Prototype

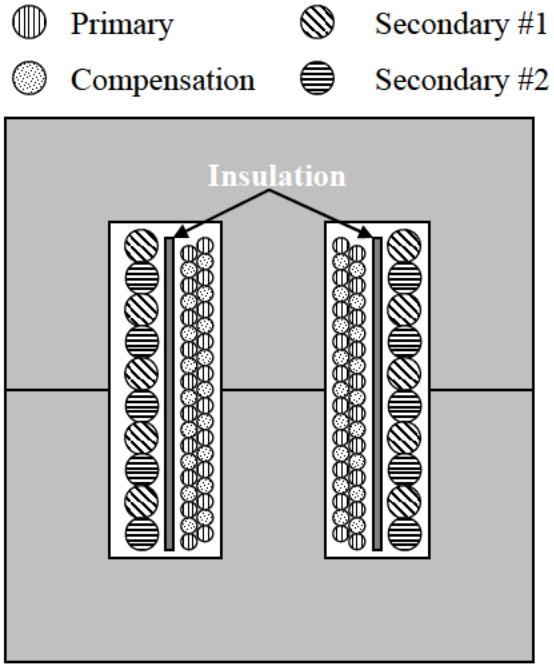

Figure 21: Winding Structure of Half-Bridge Transformer with Compensation Winding

3.2.1.3. Experimental Test Results

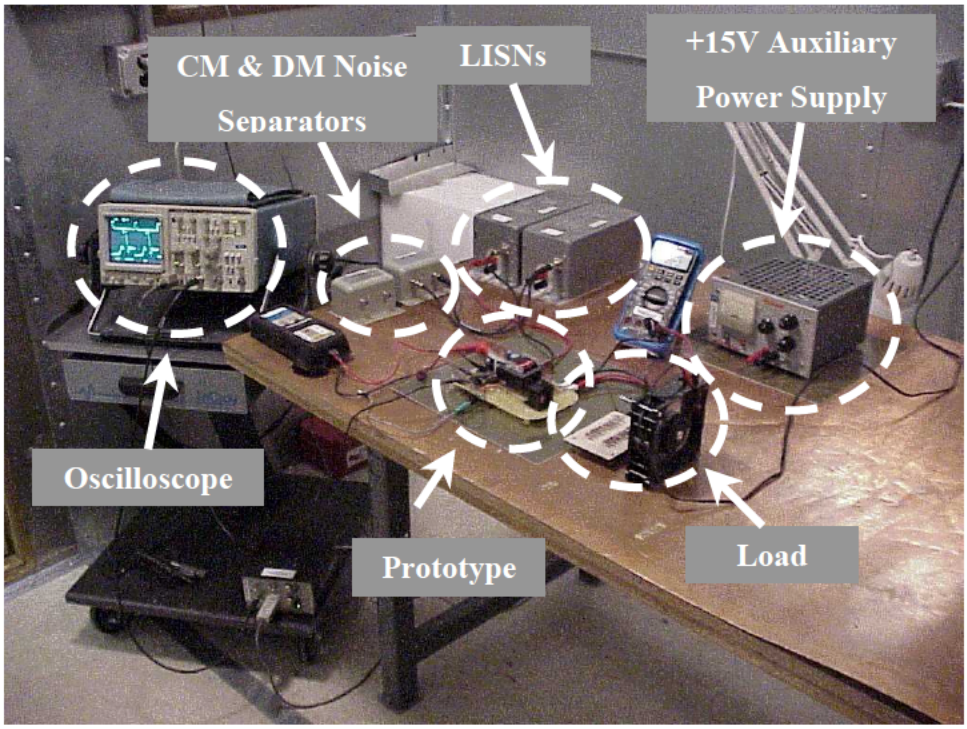

Figure 22: Test-Setup inside EMI Chamber for Half-Bridge Experiment

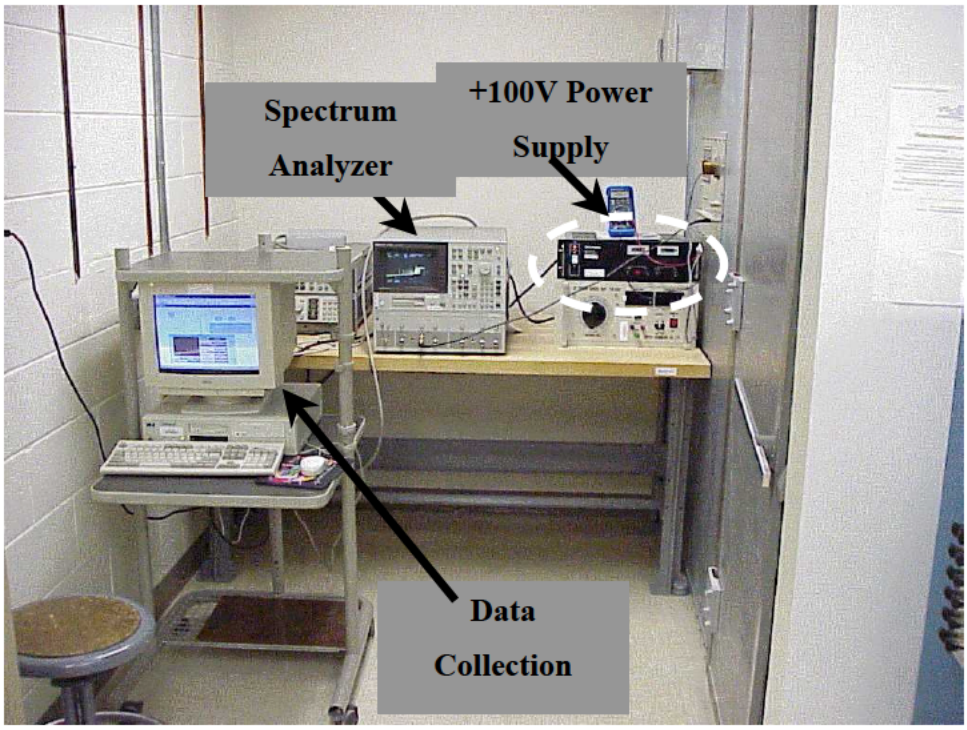

Figure 23: Test-Setup outside EMI Chamber for Half-Bridge Experiment

All EMI experiments were done using the test setup in Figure 22 and Figure 23. The circuit itself was placed on a piece of PCB FR-4 material and the circuit ground connection was connected to the ground plane. The auxiliary supply for the control circuits was similarly placed on a piece of PCB to minimize the noise that would couple from it into the ground plane and interfere with the measurement. The main DC power supply was placed outside and connected to the circuit (via the LISNs shown in the photograph) through an access hole in the wall of the EMI chamber. The load consisted of 30 1W-30Ω resistors in parallel.

Time domain information was collected using a LeCroy LC574AM digital oscilloscope (Not shown in picture), while the Tektronics 2445 analog oscilloscope shown in Figure 22 was used for routine troubleshooting. Both oscilloscopes were turned off for EMI measurements. A PC running an evaluation version of HP-VEE 5.01 was used to collect data from the spectrum analyzer. Table 3 shows the settings used for the spectrum analyzer in all tests.

Table 3: Test Settings for HP4195A in Half-Bridge Experiments

Resolution Bandwidth (RBW)	1kHz
Start Frequency	10kHz
End Frequency	10MHz
Attenuation on Input	50dBm
Video Filter	Off
IF Range	Normal

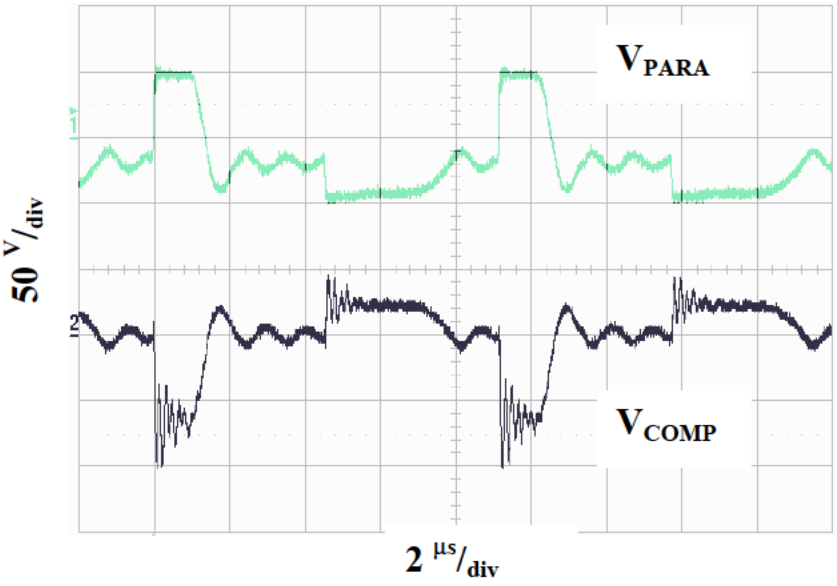

Figure 24: Half-Bridge CM Voltage Waveforms

Figure 24 show the voltage from the lower MOSFET drain to ground (V_{PARA}) and the voltage from the compensating winding to ground (V_{COMP}). The leakage inductance in the transformer causes some high-frequency ringing, but you can clearly see that the switching $^{dv}/_{dt}$ is accurately replicated by the compensating winding. The effect of the ringing will be to increase the high-frequency portion of the CM EMI, but HF noise is not as difficult to filter as the existing LF noise.

Once the circuit was verified to be operating properly a baseline measurement was taken of the CM noise spectrum. A compensating capacitance of 56 pF was then added to the circuit to see the effect of the noise cancellation technique. This value was chosen because it was the closest standard value 1000 V capacitor freely available in the lab. Unfortunately this had little to no effect, as seen in Figure 25, and the reasons for this became clear once some additional testing was performed. The compensation technique worked quite well when I added a lot of capacitance to the original C_{PARA} (Figure 26), and the resulting spectrum was very similar to the original baseline. This seemed to indicate that the original C_{PARA} was not contributing the bulk of the common-mode EMI, but rather the transformer cross-coupling capacitance was causing additional noise to couple into the ground plane through the compensating winding. When the transformer was reexamined on the HP4194 impedance analyzer, the cross-coupling capacitance was found to be on the order of 150pF, which was much greater than the measured 70pF for the MOSFET.

Based on these results the transformer was then rewound, but this time a layer of black electrical tape was inserted between the primary and secondary windings while still interleaving the primary and compensating windings. The significantly reduced the cross-coupling capacitance without interfering with the operation of the circuit. Once the first transformer was replaced with this one, several tests were run in which the heat sink was left ungrounded so that there was no parasitic capacitance from the device itself. By doing this it was then easy to see how significant the transformer EMI was, and it was also relatively simply to test the effectiveness of the canceling winding for different magnitudes of C_{PARA} by inserting a capacitor into the circuit in place of the MOSFET C_{PARA}. The results of these tests can be seen below in Figure 27, Figure 28, and Table 4.

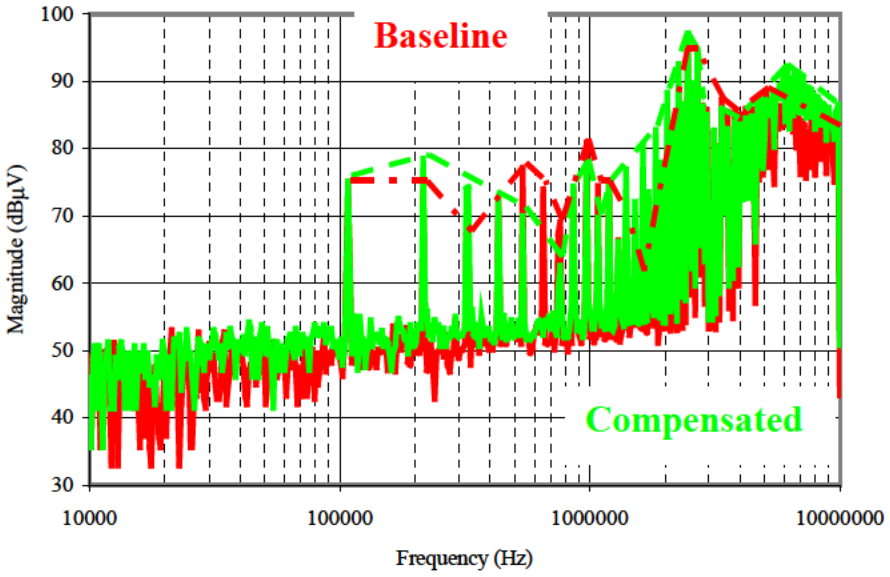

Figure 25: Half-Bridge CM Baseline and 56pF Compensation (Poor Transformer)

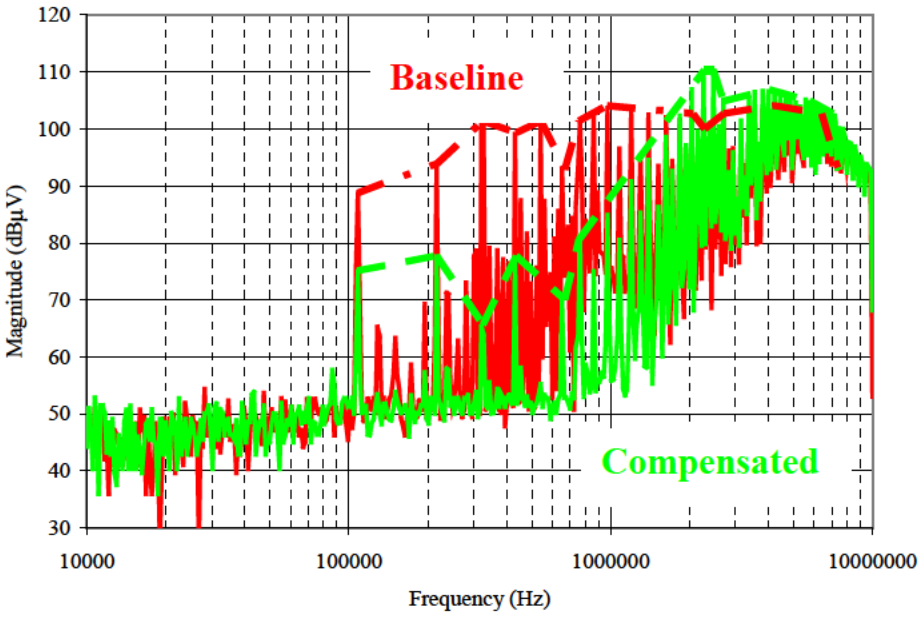

Figure 26: Half-Bridge CM Comparison with 750pF of Added C_{PARA} (Poor Transformer)

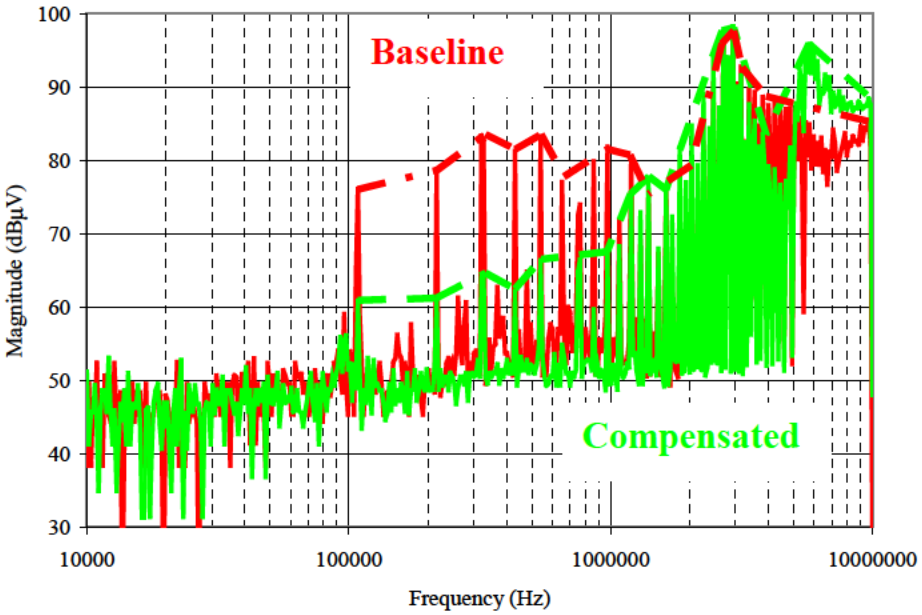

Figure 27: Half Bridge Results with C_{PARA} = 56pF (Good Transformer)

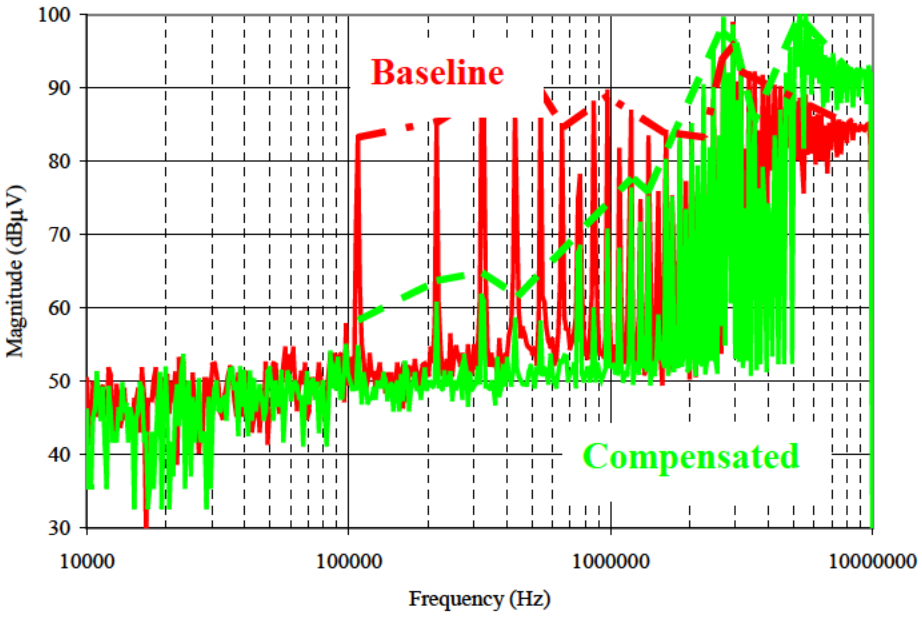

Figure 28: Half Bridge Results with C_{PARA} = 112pF (Good Transformer)

Table 4: Comparison for Selected Switching Harmonics (Heat Sink Ungrounded)

	Baseline	*56pF*			*112pF*		
N	*No Added Capacitance*	*No Compensation*	*With Compensation*	*dBµV Reduction*	*No Compensation*	*With Compensation*	*dBµV Reduction*
1	62	76	61	15	83	55	28
2	63	79	61	18	85	61	24
3	67	83	64	19	90	62	28
4	64	81	62	19	87	58	29
5	68	83	66	17	90	58	32
6	58	77	55	22	85	53	32
7	64	74	66	8	78	68	10
8	55	80	60	20	88	60	28
9	69	82	68	14	89	71	18
10	67	72	68	4	82	68	14

For the final tests, the heat sink was grounded as in the original and 56pF of compensation capacitance was added to equal the measured 70pF of C_{PARA}. The results of these tests can be seen in Figure 29, Figure 30, and Table 5. It can be seen from these results that the compensation technique can eliminate the effect of the MOSFET C_{PARA}, but the motivation for this will depend a great deal on how dominant this parasitic is in contributing to the EMI spectrum. We can also see from Figure 30 that the differential-mode EMI is unaffected—so this is not a case of shifting the EMI from one place to another. Of course, the ringing caused by the compensating winding will increase the high-frequency CM EMI, but from the standpoint of EMI filter design this penalty does not greatly impact the savings gained from reducing the low-frequency harmonics. Using additional capacitors the compensating capacitance could be more precisely tuned to the value of C_{PARA} so that the improvement would be closer to the level in the 56pF column of Table 4. My view, however, was that the additional time spent would be of little usefulness from the standpoint of proving this technique. The end result of these experiments is that this technique is very feasible for practical applications and can realize noticeable improvement in the EMI spectrum for very little cost.

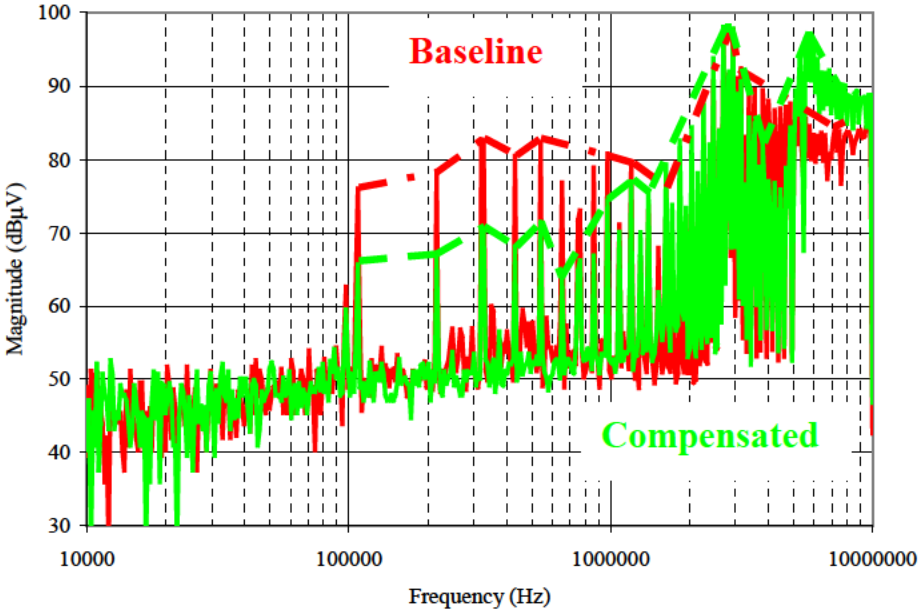

Figure 29: Final Half-Bridge CM Results

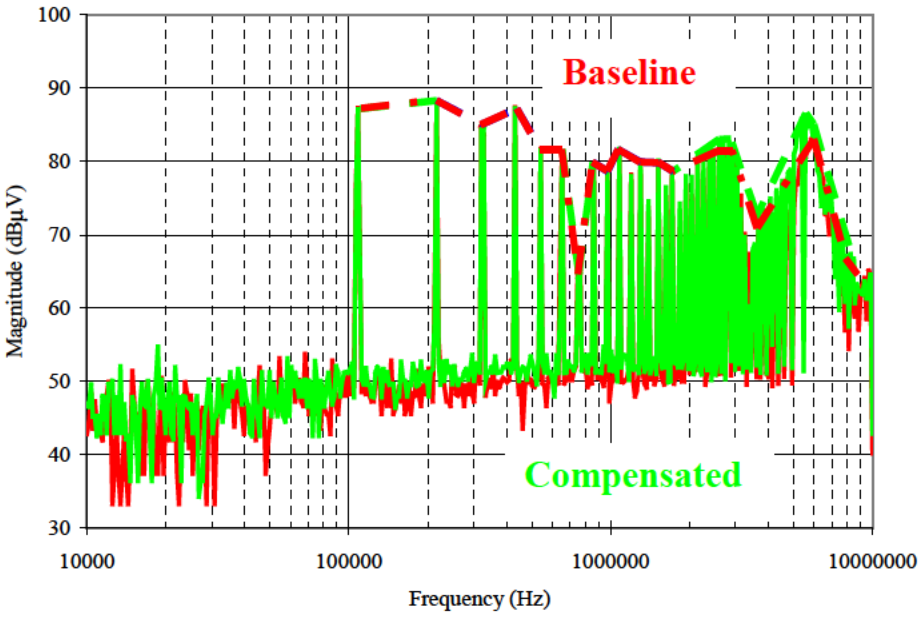

Figure 30: Final Half-Bridge DM Results

Table 5: Final Half-Bridge Switching Harmonic Comparison

N	*Baseline*	*56pF Compensation*	*dBµV Reduction*
1	76	65	11
2	78	69	9
3	83	71	12
4	80	68	12
5	82	71	11
6	77	64	13
7	73	66	7
8	79	69	10
9	81	74	7
10	79	77	2

3.2.2. Single-Switch Forward Converter

3.2.2.1. General Description

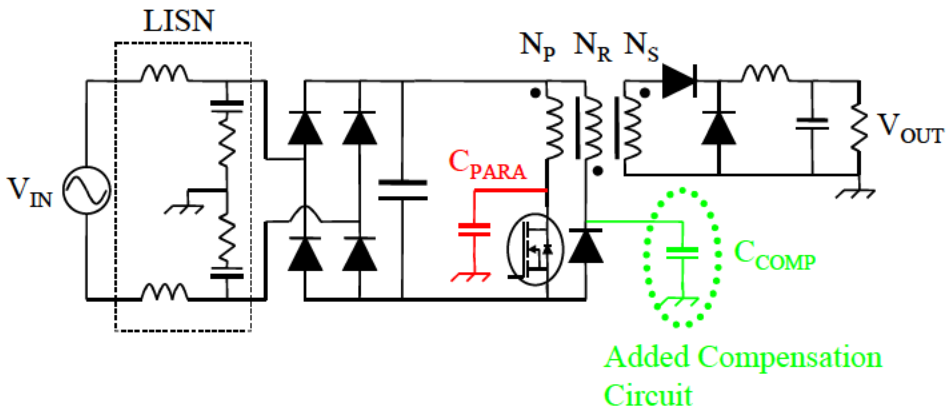

Figure 31: Off-Line Forward Converter Incorporating Passive CM Cancellation

The single-switch forward converter shown above in Figure 31 can also be easily modified to incorporate passive CM noise cancellation. For this topology, the reset winding serves as the mechanism for sensing and reversing the switching $^{dv}/_{dt}$, and therefore the only thing necessary to do is to add the compensating capacitance from the reset diode cathode to ground.

3.2.2.2. Experimental Test Results

Table 6 gives the essential design details for an open-loop control 100 W prototype that was constructed to test this concept. Figure 32 illustrates how the FET CM voltage is seen by the compensating capacitor for the experimental prototype. As with the half-bridge converter discussed in the previous section, transformer leakage inductance creates a certain amount of high frequency ringing which will cause some degradation in the high-frequency cancellation, but as before the motivation behind this technique is to reduce the low-frequency portion of the spectrum to reduce the size of the input line filter.

Table 6: Design Details of Forward Converter Prototype

Input Voltage	120 V_{AC}
Output Voltage	12 V
Output Current (max)	8 A
Frequency	110 kHz
Turns Ratio (Pri:Com:Sec)	2:2:1
MOSFET	BUK456-200A
Reset Diode	BYV29-500
Rectifier Diodes	30DF2
Output Diodes	18TQ050
Controller	UC3823BN
Output Inductor	20 µH
Output Capacitors	22 µF
Input Capacitor	1000 µF

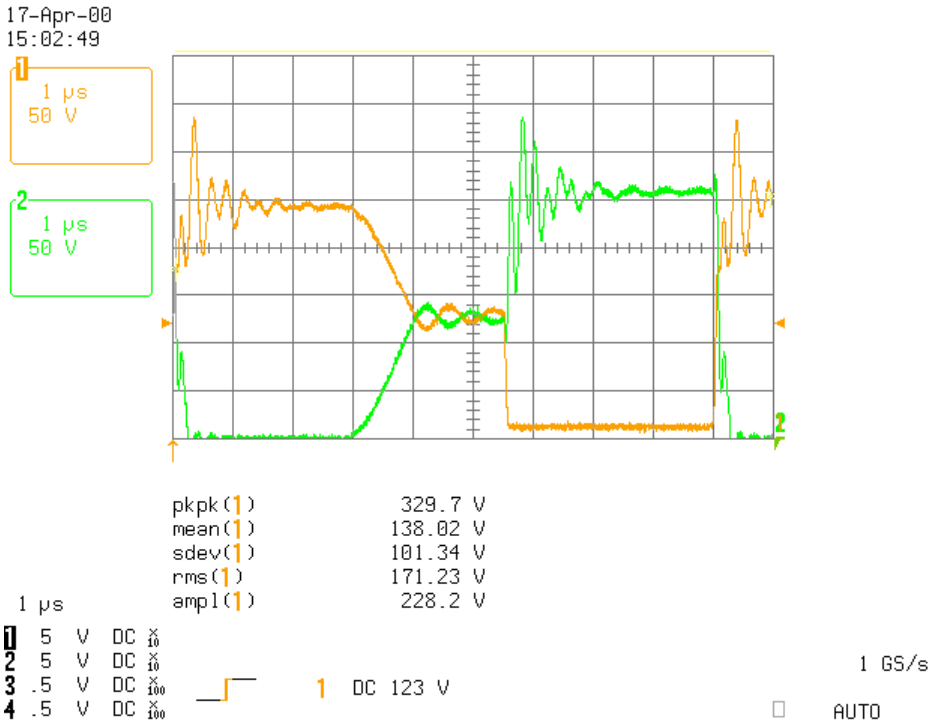

Figure 32: Forward Converter FET and Diode Waveforms

Table 7 shows the settings for the HP4195A spectrum analyzer used for these tests. Note that the start and stop frequencies differ from the half-bridge tests. This does not change the results, but was done because at the time the author was using the CISPR specifications as a guideline. With the half-bridge prototype the author was being supported by funds from the Office of Naval Research, and therefore it was thought prudent to use MIL-STD-461E guidelines instead. Apart from that detail, all other aspects of the test setup are the same as in the above section, and therefore will not be reiterated.

Table 7: Test Settings for HP4195A in Forward Converter Experiments

Resolution Bandwidth (RBW)	10kHz
Start Frequency	100kHz
End Frequency	30MHz
Attenuation on Input	50dBm
Video Filter	Off
IF Range	Normal

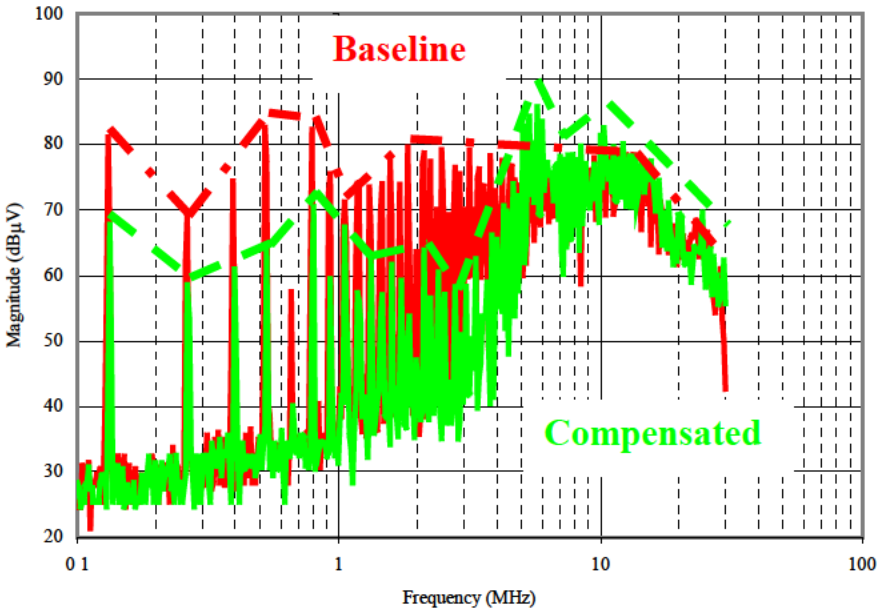

Figure 33: Experimental CM Noise Comparison for Forward Converter

Figure 33 shows the results of noise cancellation for the forward converter experiment. By adding 86 pF of compensating capacitance, the first harmonic was reduced by ~15 dBµV. Noise cancellation remains between 10 and 15 dBµV up to approximately 500 kHz, where high-frequency ringing from the transformer leakage inductance begins to make negatively affect the results. Above 10 MHz the two spectrums are approximately the same, indicating that the transformer and the compensating capacitor are no longer operating effectively.

3.3. Buck-Boost Derived Converters

3.3.1. Flyback Converter

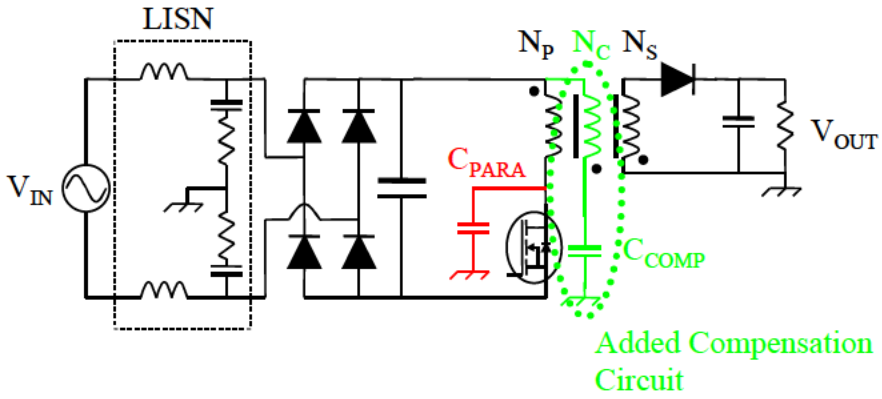

Figure 34: Isolated Flyback Topology Incorporating Passive CM Cancellation

As with buck derived converters, buck-boost derived isolated topologies such as the flyback can also be modified to incorporate passive CM noise cancellation. The method of doing this is very similar to that of the forward converter, and is shown in Figure 34. Of course, since the flyback converter does not use a reset winding, the compensation winding N_C must be added to the main power transformer. Since the N_C winding uses small gauge wire, then it would be a fairly cheap addition to the transformer as N_C can be interwound with the primary winding N_P for a 1:1 turns ratio.

To demonstrate the operation of this circuit simulated results using the Saber simulation package will be shown. While these results will naturally not be as convincing as experimental data, the amount of time necessary to build prototypes for each of the examples given in this text would be quite large. Therefore a certain number of these topologies will use simulations incorporating many of the parasitic elements seen in a prototype in order to demonstrate the feasibility of the noise cancellation concept for the particular topology.

The Saber model of the flyback converter is shown below in Figure 35. It includes the commercial LISN model and a mathematical block that separates the CM and DM noise voltages. The diodes used are all piece-wise linear models with a V_{DD} of 1 V. The input capacitor was considered to be of electrolytic type, and therefore has sufficient ESL for a resonant frequency of ~150 kHz and an ESR of 0.01 Ω. The output capacitor is modeled as several electrolytics in parallel with a high-frequency ceramic, and therefore has an ESL of 2 nH and a ESR of 0.001 Ω for the capacitance value of 200 μF. The MOSFET is modeled as an ideal switch with turn-on time of 50 ns and turn-off of 100 ns, with an anti-parallel diode with the same characteristics as the others. Also included is a packaging inductance value of 5 nH and a C_{PARA} equal to 50 pF.

The model of the transformer takes into account leakage inductance, resonant frequency, and cross-coupling capacitance. The turns ratio is 10:10:1 (primary:compensation:secondary). Leakage inductance was considered to be 1% of the magnetizing inductance of 100 μH. I decided to set the resonant frequency of the transformer at 700 kHz, and accordingly made the bypass capacitance to be 500pF. Cross-coupling capacitance is a difficult thing to model correctly due to the inherently distributed nature of the capacitance, but I decided to model this a four capacitances of equal value (10 pF), distributed in such a way as to allow noise currents to pass between all three winding.

It should be noted that the input voltage source is DC rather than 60 Hz AC. This is because and AC source would require significantly more time for the converter to reach steady-state, and would require special options to properly handle when taking the FFT of the LISN noise voltages. Since the noise that this source would contribute would only affect the very low frequency portion of the CM and DM noise spectrums, I believed this to be a justifiable abstraction for the model.

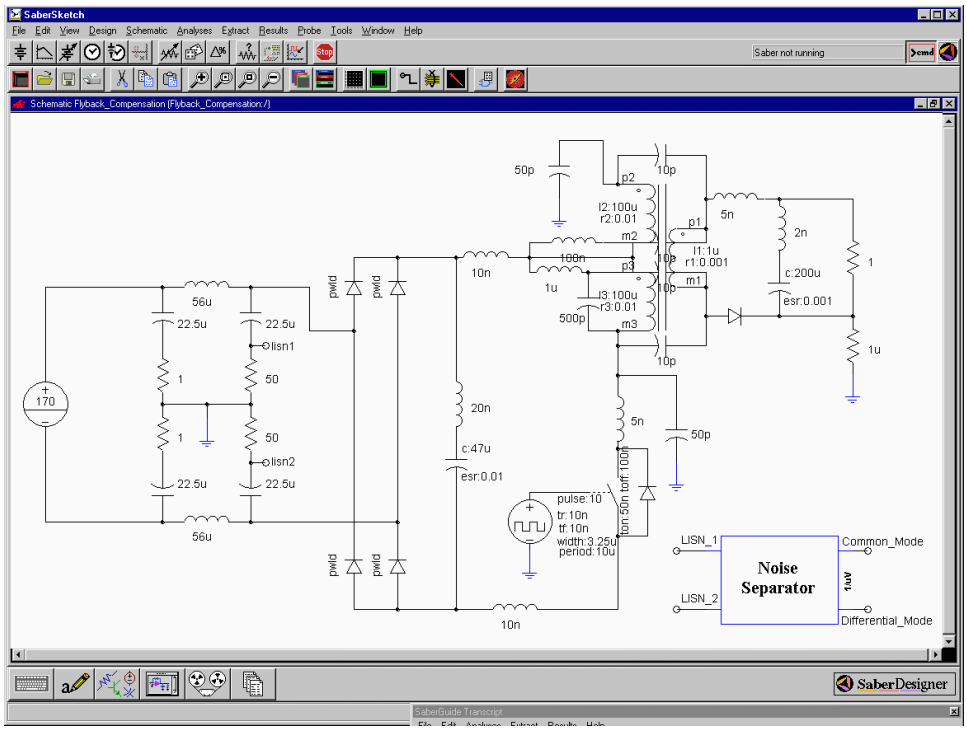

Figure 35: Saber Model for Noise Compensated Flyback Converter

The results of the simulation are shown below in Figure 36 through Figure 39. Figure 36 shows the parasitic and compensating voltages, while Figure 37 shows the corresponding currents. Also shown in Figure 37 is the sum of the LISN currents, which demonstrates the level of cancellation. In the simulations, the effect of leakage inductance is not manifested as severely as in the experimental results. This is due not only to the reduced complexity of the model, but also with the method of simulation. Since a discrete time step is used, the results will tend to be less accurate for higher frequencies because of the effect of the Nyquist sampling criterion.

Figure 38 compares the CM noise spectrums and Figure 39 compares the DM noise spectrums of the compensated and uncompensated converter models. These results were achieved by using the FFT analysis option of Saber, and using the following options: fixed transient time step of 0.1 µs, transient data from 285 µs-295 µs, 1024 points, and a Rectangular window. The simulation predicts approximately 20 dBµV of reduction for the low frequencies, reducing to 5-10 dBµV at the high frequencies. As before, the DM noise spectrum is unchanged from before.

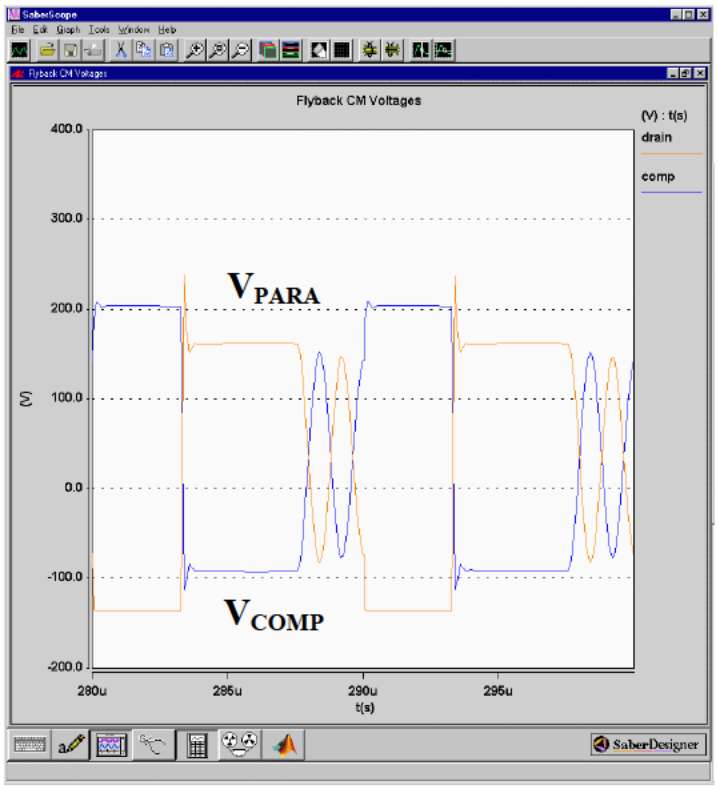

Figure 36: Simulated Parasitic and Compensating Voltages for Flyback Converter

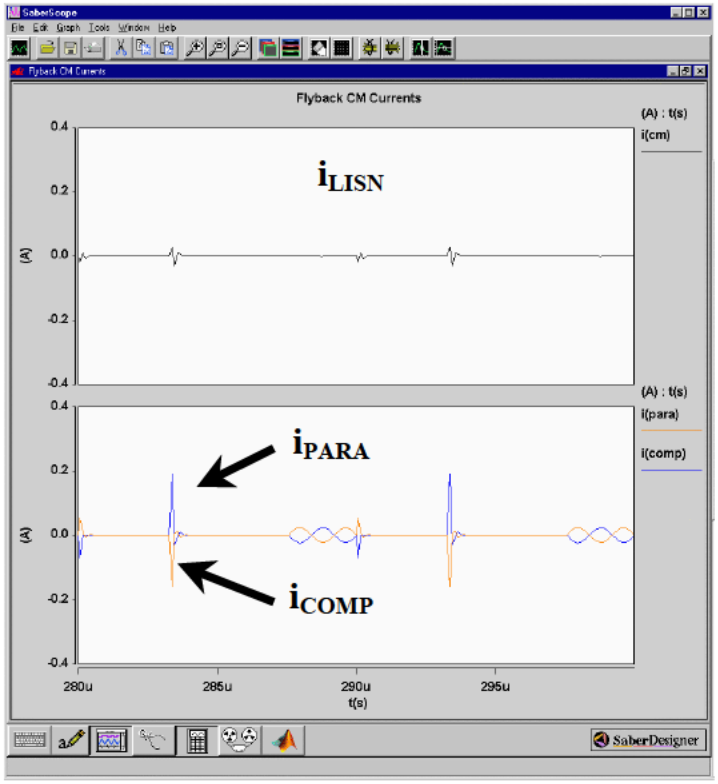

Figure 37: Simulated Parasitic and Compensating Currents in Flyback Converter

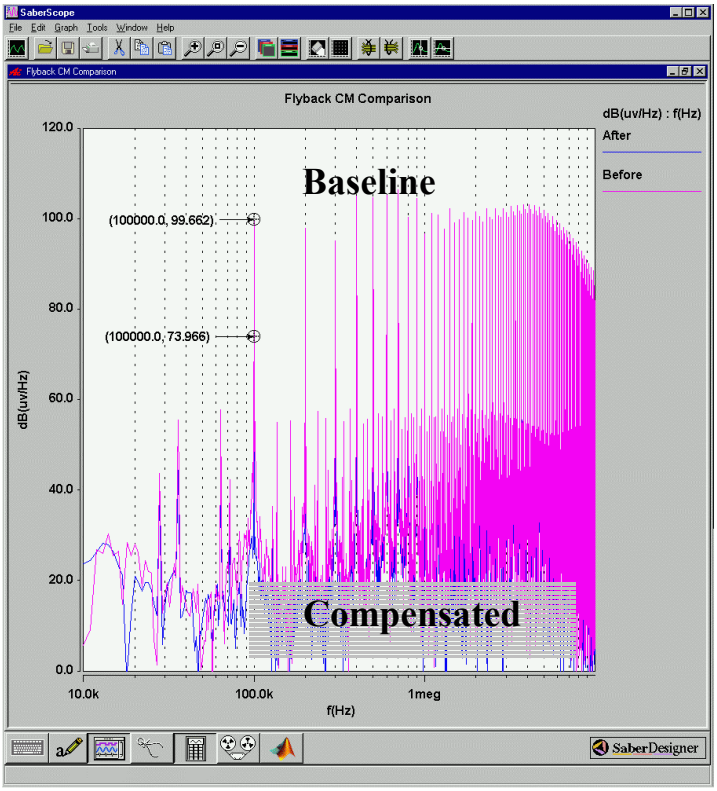

Figure 38: Simulated CM Spectrum Comparison for Flyback Converter

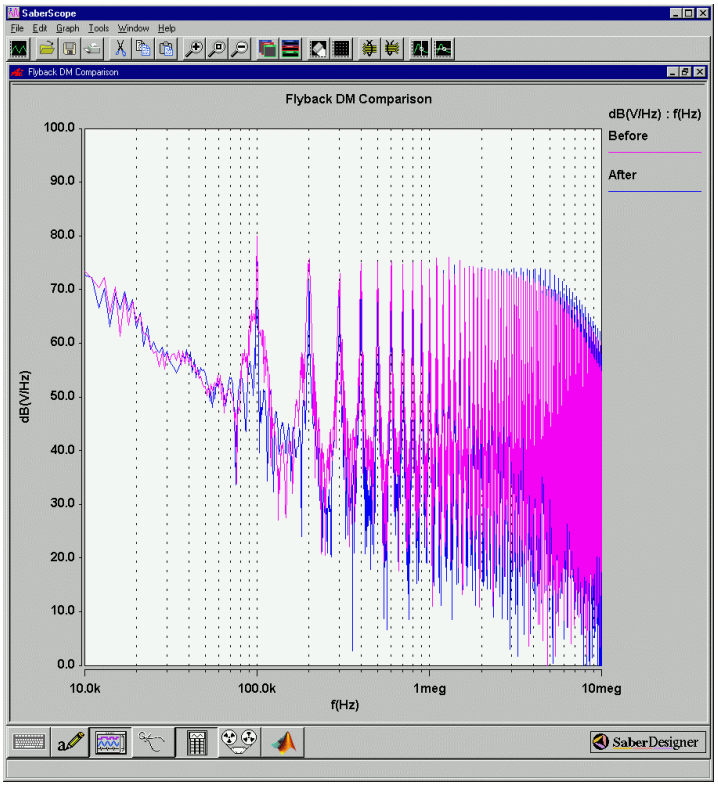

Figure 39: Simulated DM Spectrum Comparison for Flyback Converter (Unchanged)

3.4. Remarks

We have seen in this chapter how passive CM noise cancellation can be applied to conventional power converter topologies with success. Isolated topologies are perhaps the easiest and cheapest topologies to incorporate passive noise cancellation, since the compensation winding can be added to an existing transformer structure. In the case of the single-switch forward converter, adding noise cancellation is very trivial and there is little reason to not include it as a general design rule. The issues with regards to incorporation are as follows: ensure tight coupling between the primary and compensating winding so as to maximize the switch $^{dv}/_{dt}$ pickup, and minimize cross-coupling capacitance between the compensating and secondary windings. The former can be accomplished by interleaving the two windings during construction, and the latter can be accomplished by the use of a few cents worth of electrical tape, as shown in the section on the half-bridge converter.

Chapter 4. Proposed Passive Cancellation in Non-Isolated DC/DC Converters

While applications of a passive CM noise cancellation scheme are perhaps most obvious for the front-end converter, it is no less important that these techniques be applied elsewhere in a distributed power system if the individual conversion units see a large ΔV from input to output. In this chapter methods are presented for achieving noise cancellation by modifying the filter inductors of the common families of non-isolated DC/DC converters: buck, boost, and buck-boost.

4.1. Buck Converters

4.1.1. Description of Technique and Model Results

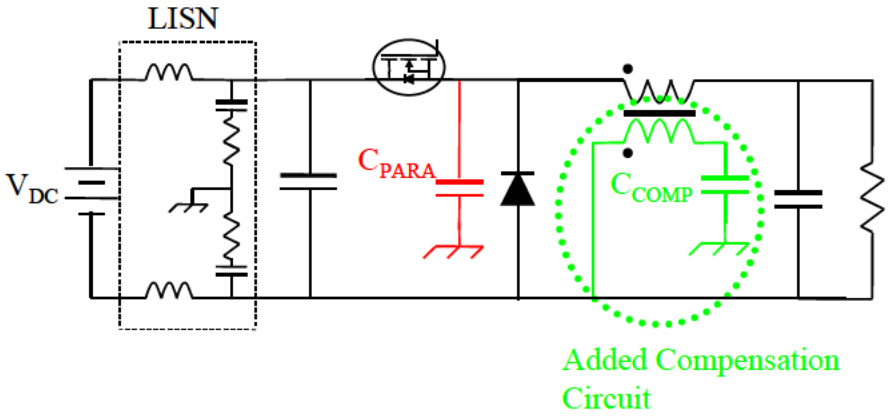

Figure 40: Buck Converter Incorporating Passive CM Noise Cancellation

Figure 40 shows how the common buck converter topology is modified to incorporate passive CM noise cancellation. This method is common to all the non-isolated topologies discussed in this chapter, as will be shown. The compensation winding is simply interwound with the filter inductor winding, to yield a 1:1 turns ratio and to ensure tight coupling between the primary and

compensating windings and to minimize leakage inductance. This technique allows the inductor design to proceed almost independent of the decision to incorporate passive cancellation, since the required filter inductance is normally quite adequate for the purposes of noise cancellation.

Simulated results are presented in the following graphs, and Figure 41 illustrates the Saber model used in these simulations. The same LISN model as used in the flyback converter from the last chapter is also used in this model. An ideal switch with t_{on} and t_{off} parameters and a piecewise linear diode model are used to approximate a MOSFET switching at 100 kHz, and 50 pF is used as the source to heat sink capacitance C_{PARA} (This assumes a TO-220 or similar type package). Note that there could also be a capacitance from the MOSFET drain to heat sink, but since the $^{dv}/_{dt}$ on the drain side is much smaller the effect of this parasitic is negligible and was therefore not included. Also included are package inductances for the MOSFET and commutating diode.

The input and output filter inductances are modeled here as electrolytics in parallel with low-ESL ceramic capacitors. Some results are shown later illustrating the necessity of a small ESL on these capacitors. The transformer (filter inductor) model uses a linear core model with an infinite B_{SAT} and a permeability of 1. The inductance value of 50 μH was chosen simply because it represented a reasonable value for the purposes of these tests. Parallel capacitances are used to simulate a resonant frequency of 700 kHz. A relatively large cross-coupling capacitance of 200 pF is used in this model to simulate the two windings being very closely spaced, and this capacitance is split into two parts and connected in a “criss-cross” fashion. This was done because it is assumed that the cross-coupling capacitance is very small between sections of the windings at opposite ends of the bobbin. The close spacing should also result in a very small leakage inductance, so a value of 0.1% was chosen and split into two equal parts for each side of the transformer.

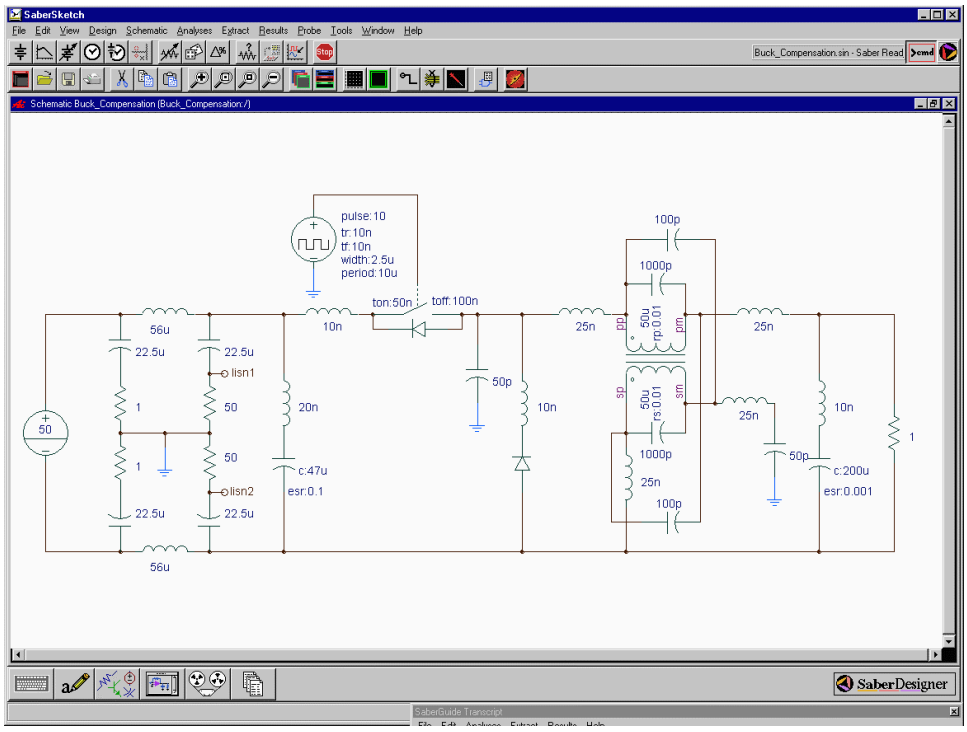

Figure 41: Saber Model for CM Noise Compensated Buck Converter

Figure 42 and Figure 43 show the parasitic and compensating voltages and currents under conditions when the noise cancellation technique is operating as it should. Under these circumstances one should expect approximately 10-15 dBμV of attenuation in the CM noise spectrum seen across the 50Ω LISN resistors with no appreciable degradation in the DM noise spectrum. This is illustrated in Figure 44 and Figure 45.

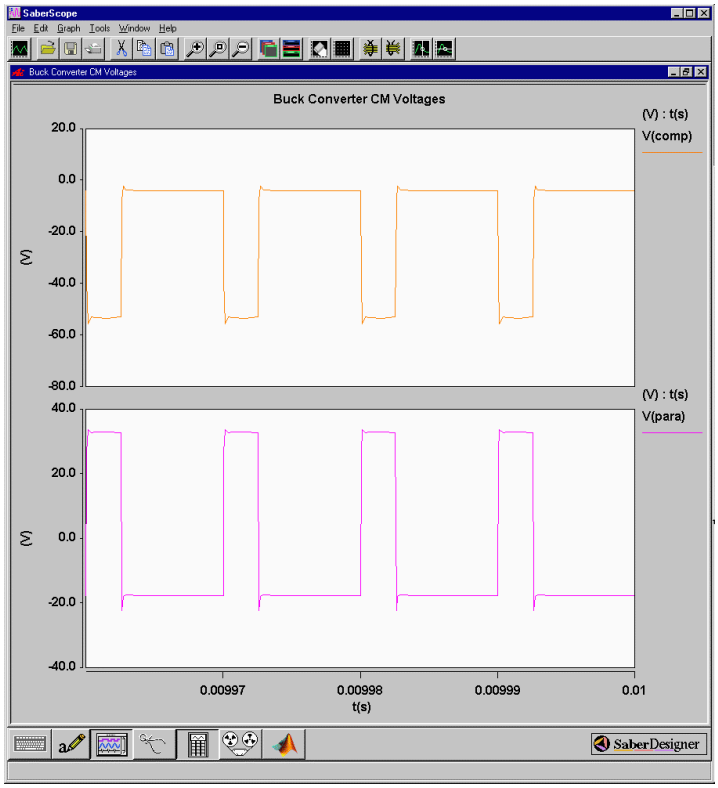

Figure 42: Buck Converter CM Voltages

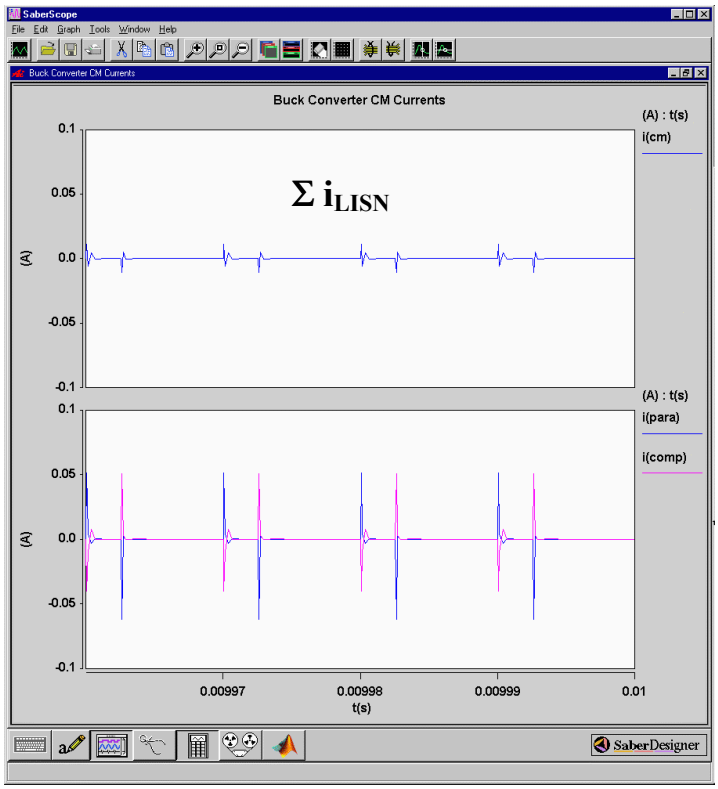

Figure 43: Buck Converter CM Currents

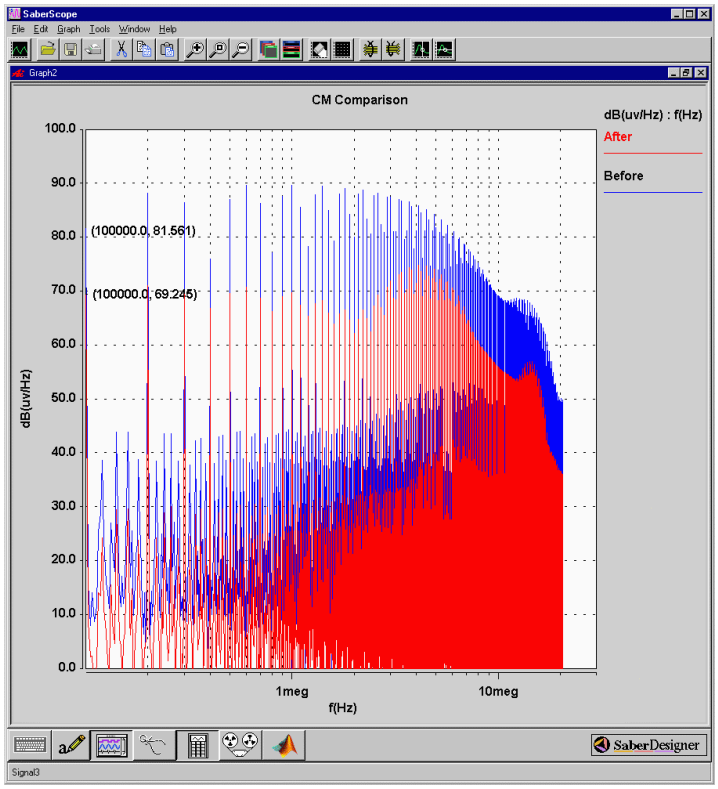

Figure 44: Buck Converter CM Noise Spectrum Comparison

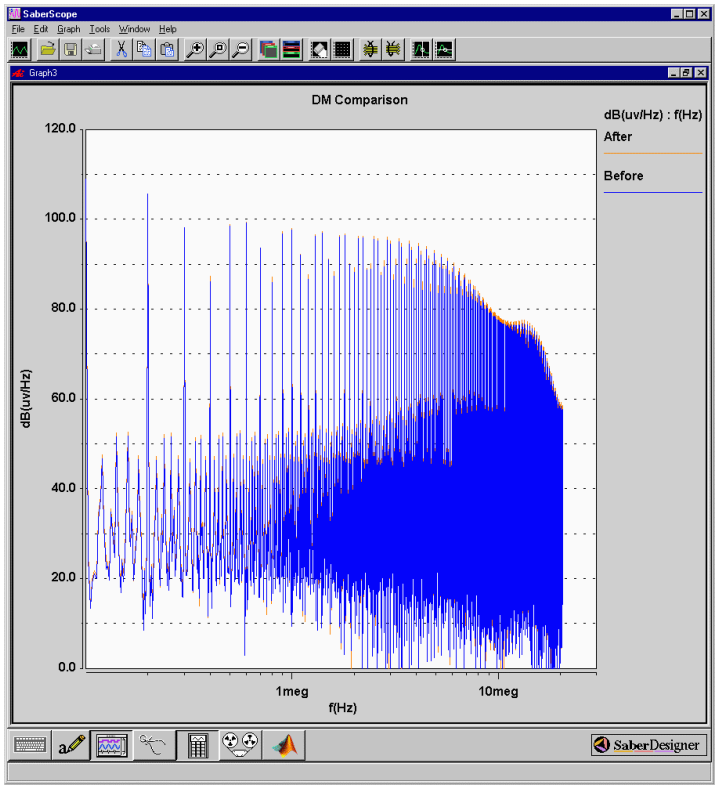

Figure 45: Buck Converter DM Noise Spectrum Comparison

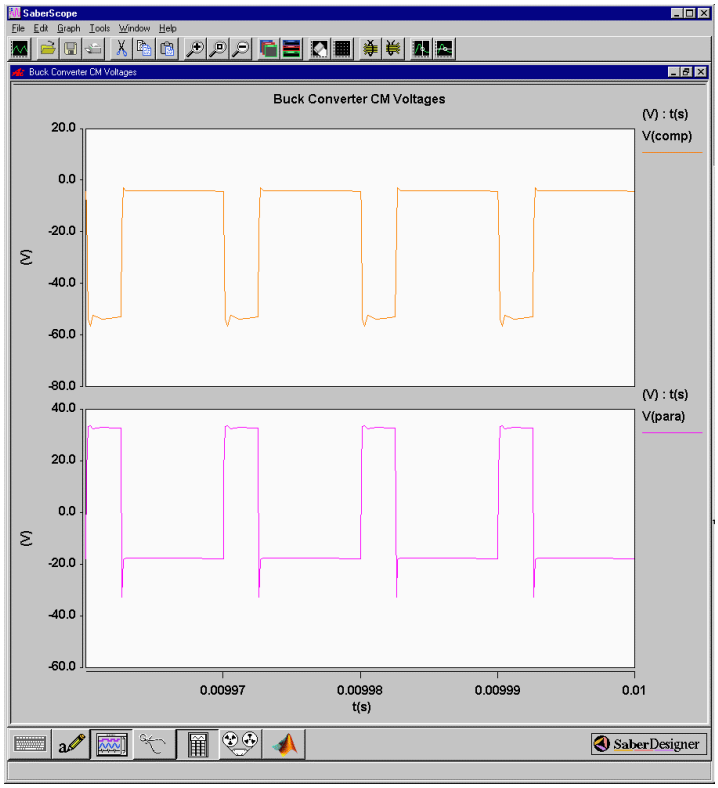

Figure 46: Buck Converter CM Voltages, High Input Capacitor ESL

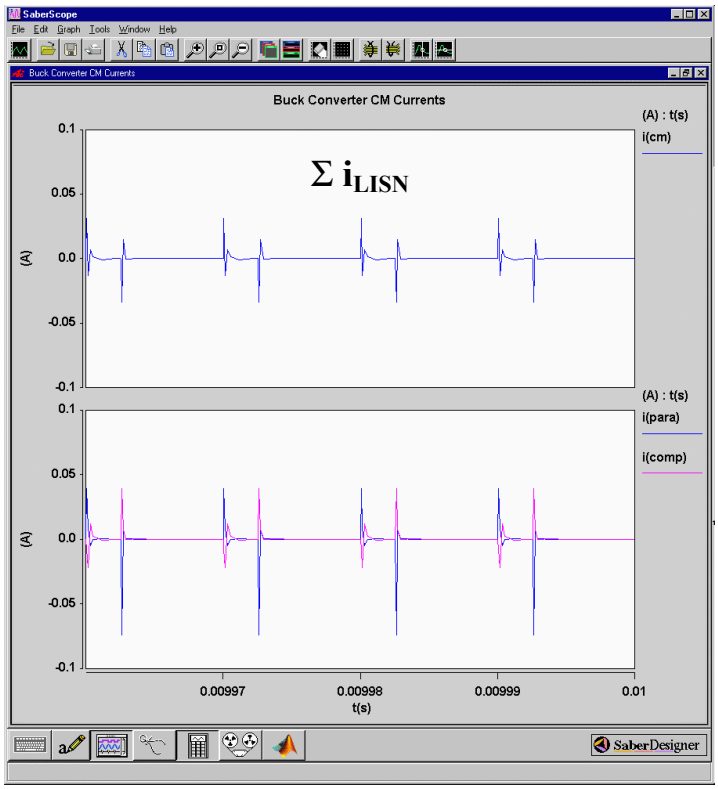

Figure 47: Buck Converter CM Currents, High Input Capacitor ESL

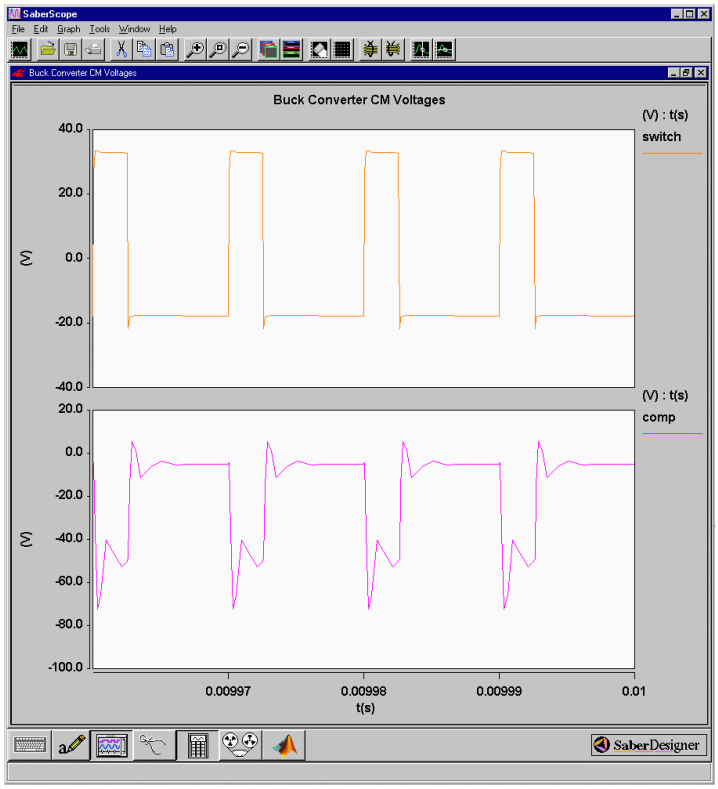

Figure 48: Buck Converter CM Voltages, High Leakage Inductance

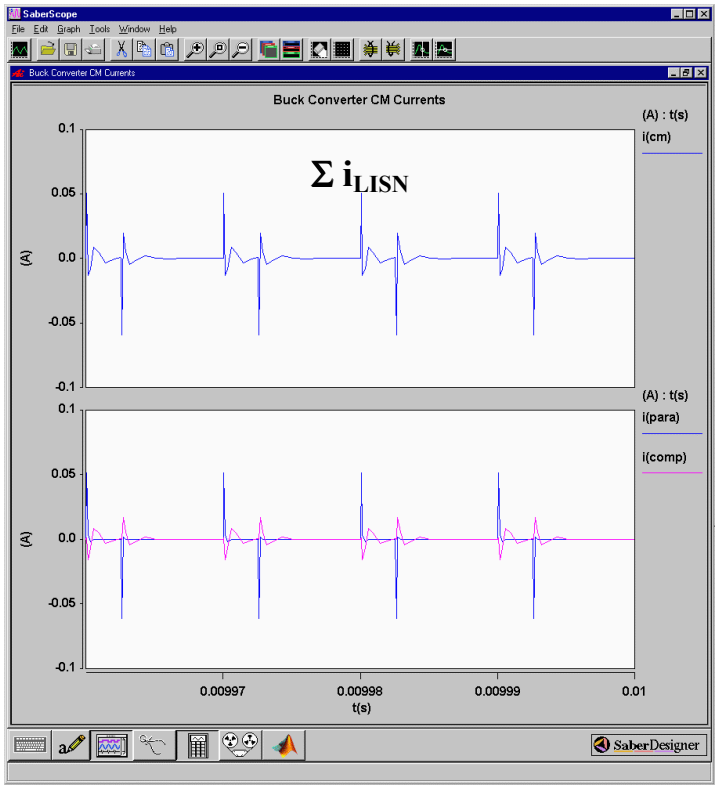

Figure 49: Buck Converter CM Currents, High Leakage Inductance

4.1.2. Limitations of the Technique

Circumstances in which the noise cancellation technique does not work are shown in the voltage and currents plots of Figure 46 through Figure 49. These circumstances encompass two main situations. The first limitation is encountered by the magnitude of the ESL of the input capacitor. Inductances act as $^{di}/_{dt}$ limitors in the overall circuit, and it should be immediately apparent that the large value of series inductance in the LISN limits the current-sourcing ability of the main power source of the converter. The energy for these pulsating currents must therefore be supplied by this input capacitor, but it's own series inductance will also limit its current sourcing capabilities. For the original working simulation this parasitic component was set at 10 nH.. As this value is increased the ability of the capacitor to source the high-frequency currents required by the compensating transformer becomes more and more limited. At 100 nH of ESL the noise compensation circuit is completely ineffective. As you can see in Figure 46 the voltage seen by the compensating is very similar to the parasitic CM voltage but in Figure 47 it is quite obvious that there is something that is limiting the current through the compensating capacitor.

The other serious limitation is the leakage inductance of the compensating transformer. Figure 48 and Figure 49 illustrate the ineffectiveness of the compensating circuit when the transformer leakage inductance is increased from 0.1% to 10% of the transformer magnetizing inductance. As the primary winding of the transformer is essentially serving as a voltage sensor in order to measure the switch $^{dv}/_{dt}$, the waveform tends to be split between the leakage inductance and the magnetizing inductance. So long as the leakage inductance remains small in comparison with the magnetizing inductance the distortion is negligible, but eventually the $^{dv}/_{dt}$ seen by the compensating capacitor becomes too degraded for effective use.

While the problems of ESL and leakage inductance are serious limitations, they can be easily avoided. In order to bring the input capacitor ESL down to an acceptable level, a low-ESL capacitor can be paralleled. Leakage inductance can also be easily minimized by closely winding the primary and compensating windings. For the experiments done in this thesis the two windings were twisted together and wound at the same time. This resulted in leakages much less than 0.1% and quite acceptable results. Leakage inductance still causes problems at high frequency since it stays relatively constant while the magnetizing inductance quickly drops off after the transformer resonant frequency. As discussed in the previous chapter, though, this is of less importance given the low frequency gains.

One important question the reader may have is the effect of different loads on the noise cancellation circuits. Various light and heavy resistive and inductive loads were simulated, and no noticeable degradation was observed. A problem does occur at extreme choices of duty cycle, because the natural ringing during turn-on and turn-off does not have sufficient time to be damped out and can therefore introduce errors into the $^{dv}/_{dt}$ measurement.

4.2. Boost Converters

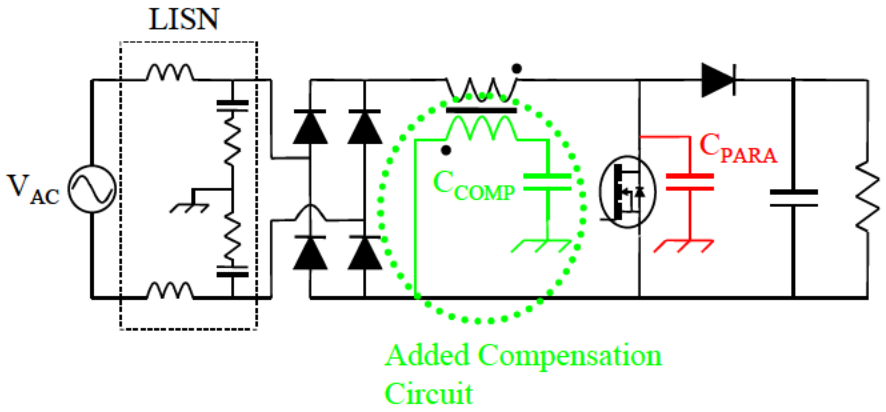

Figure 50: Boost Converter Incorporating Passive CM Noise Cancellation[27]

CM noise cancellation for the standard boost converter topology is illustrated by the diagram in Figure 50. This section is unique in this thesis because it presents work not performed by the author. Work on the boost converter was presented at the Applied Power Electronics Conference (APEC 2000) by Wu Xin and others from Zhejiang University and Hong Kong University in the Peoples Republic of China. As far as this writer can determine after exhaustive literature and patent searches, this and one other paper[28] are the only other publicly known works that have been done in the field of power converter passive noise cancellation. Since their work is publicly

[27] W. Xing, pg. 179

[28] F. Costa's work is discussed in Chapter 5.1.1.

available and generally complete, there is no advantage to be gained by my duplication of their efforts.

Figure 51 and Figure 52 show the experimental results for the prototype boost converter. Interestingly, the CM noise spectrum yields greater attenuation over a larger bandwidth than I have been able to achieve with my own experiments. As you can see in the CM spectrum comparison of Figure 52, the attenuation is close to 20 dBμV up to 10 MHz. My theory regarding this is that these authors did a better drop of minimizing other CM parasitic elements in their prototype. I expect also that they were more careful in the construction of the noise compensation transformer, which resulted in a higher resonant frequency and thus less interference from leakage inductance over a greater bandwidth. It is to be expected that the limitations shown in the previous section also apply to the boost converter.

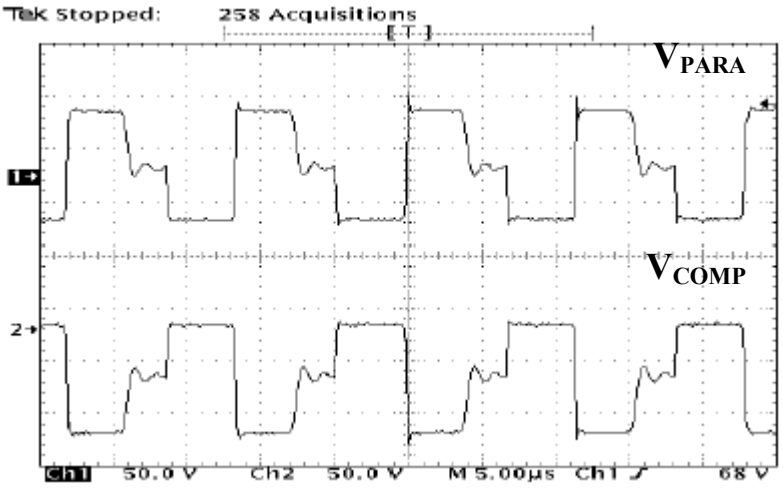

Figure 51: Boost Converter Parasitic and Compensating Voltage Waveforms[29]

[29] Wu Xing. pg. 180

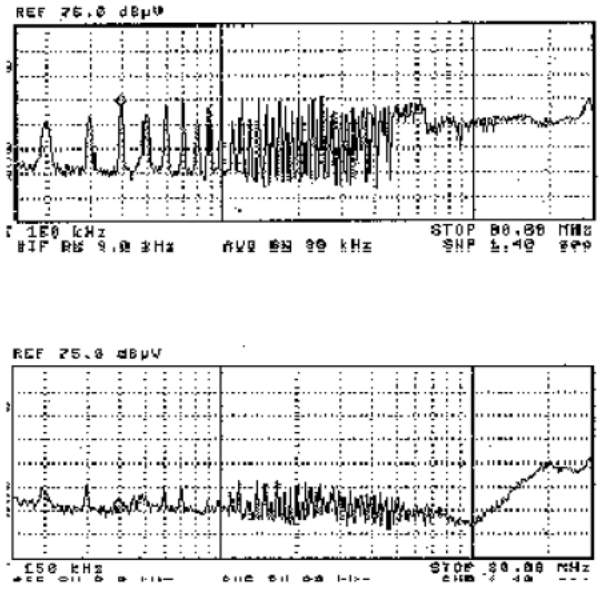

Figure 52: Boost Converter CM Noise Spectrum Comparison[30]

4.3. Buck-Boost Converters

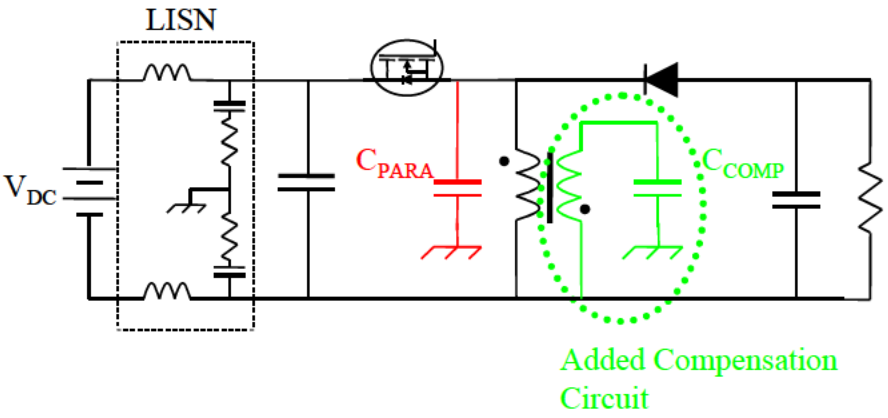

Figure 53: Buck-Boost Converter Incorporating Passive CM Noise Cancellation

[30] Ibid. pg. 180

The common buck-boost topology is also quite amenable to the inclusion of passive CM noise cancellation, as is shown in Figure 53. In order to shorten the time needed to develop a simulation model to test this modification, the same parasitic parameters were used here as were used in the buck converter and the complete Saber model is shown in Figure 54 for reference. The buck-boost converter was designed for 100 kHz operation, with 15 V output for 50 V input.

Figure 55 through Figure 58 show the noise cancellation circuitry under normal operation. Results are very similar to those observed with the buck converter, with 11 dBµV of attenuation is the first switching harmonic at 100 kHz. Naturally these results could be improved if input capacitor ESL and transformer leakage inductance are reduced further, but these values were picked as reasonable values for the purposes of illustration. Please also note, as before, that the DM noise performance is not degraded by the incorporation of the CM noise cancellation circuitry.

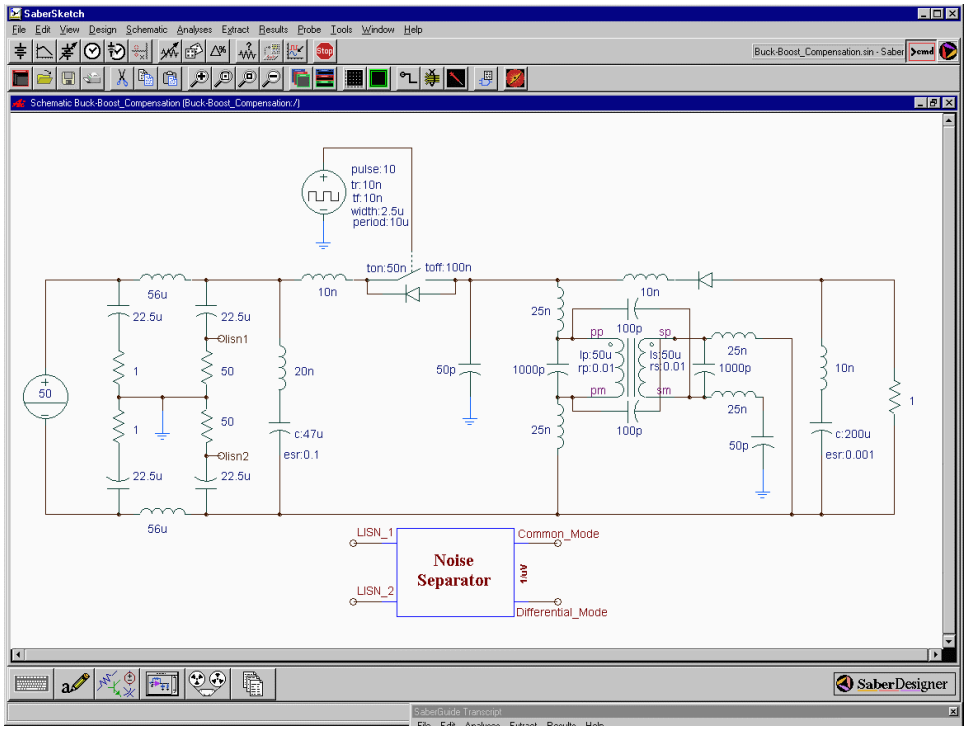

Figure 54: Saber Model for CM Noise Compensated Buck-Boost Converter

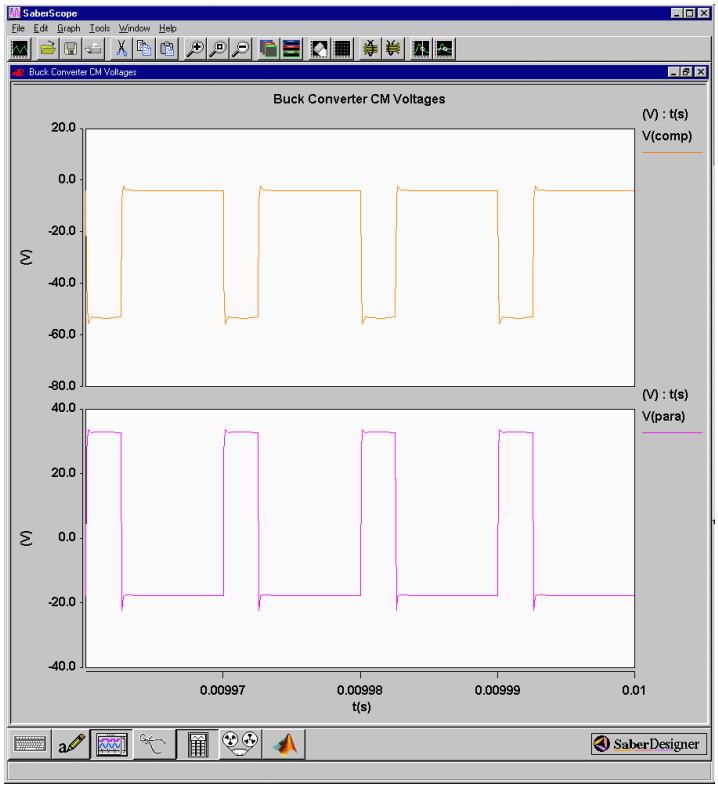

Figure 55: Buck-Boost Converter CM Voltages

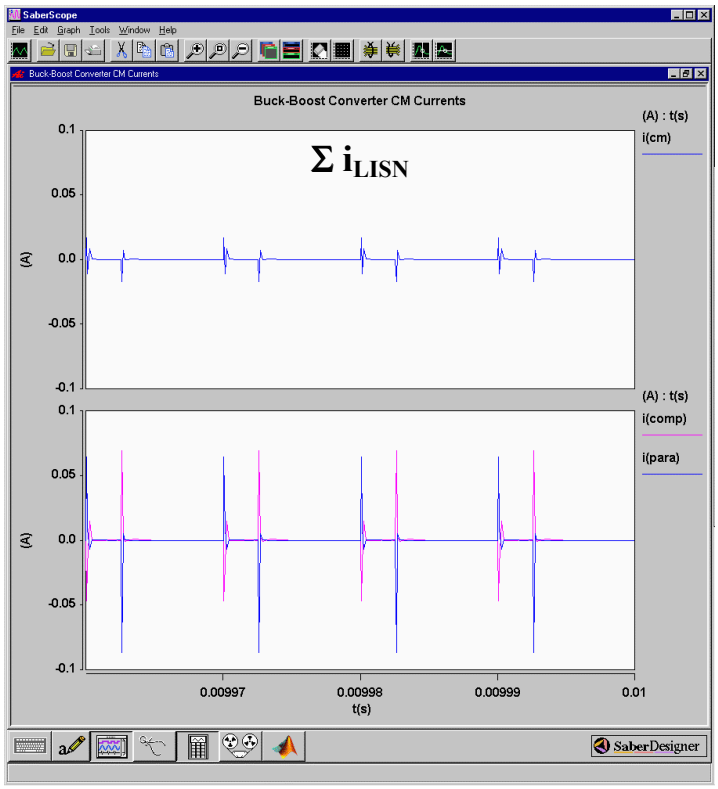

Figure 56: Buck-Boost Converter CM Currents

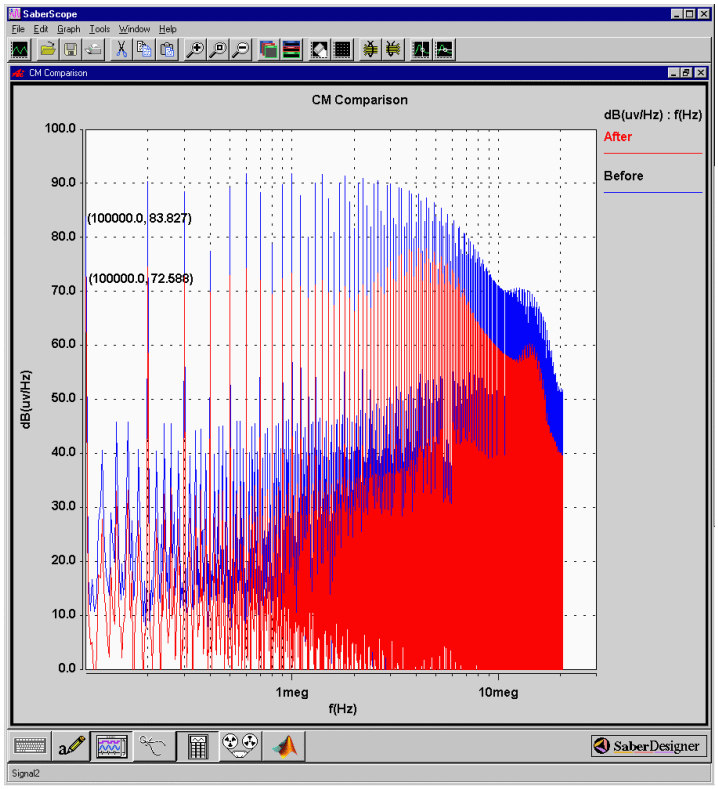

Figure 57: Buck-Boost Converter CM Noise Spectrum Comparison

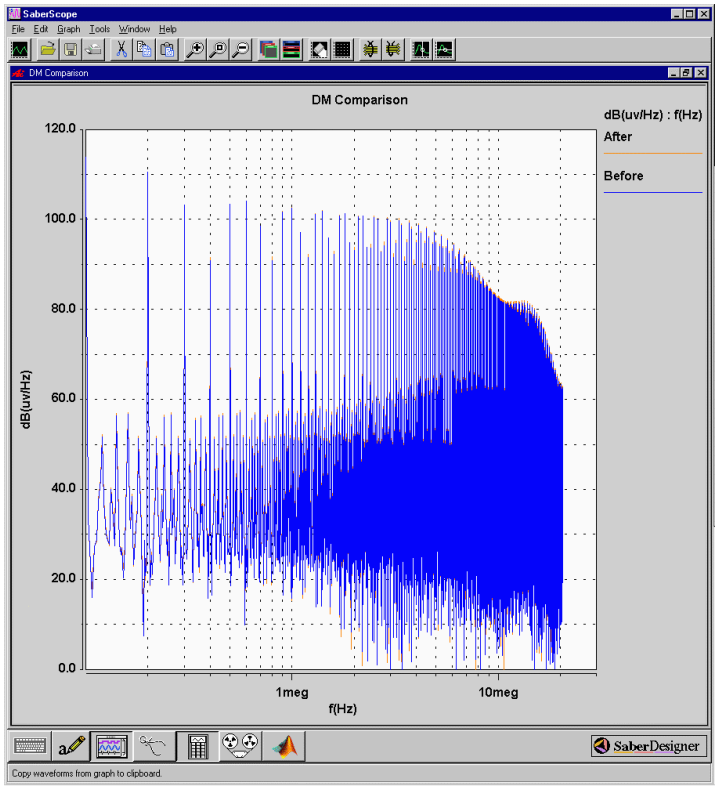

Figure 58: Buck-Boost Converter DM Noise Spectrum Comparison

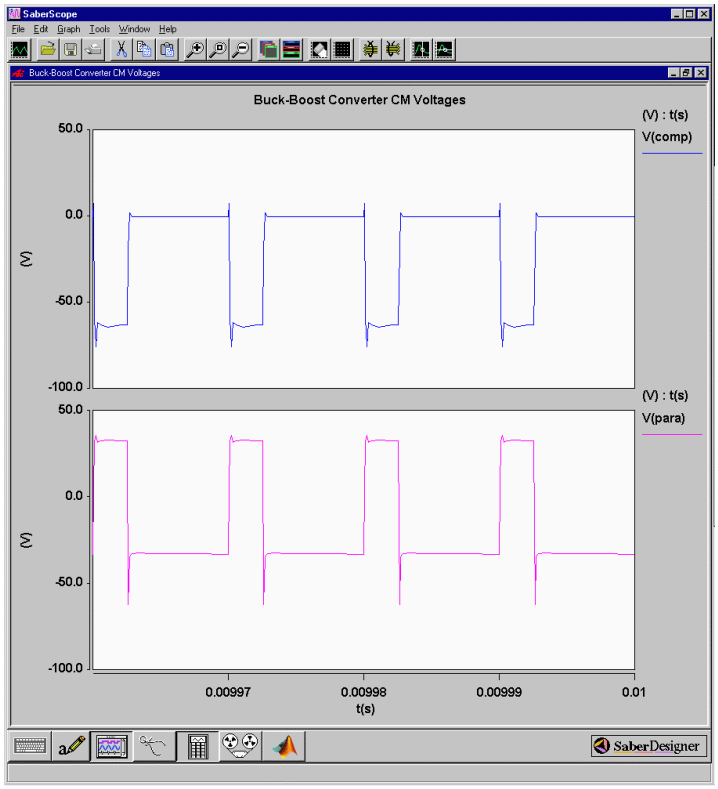

Figure 59: Buck-Boost Converter CM Voltages, High Input Capacitor ESL

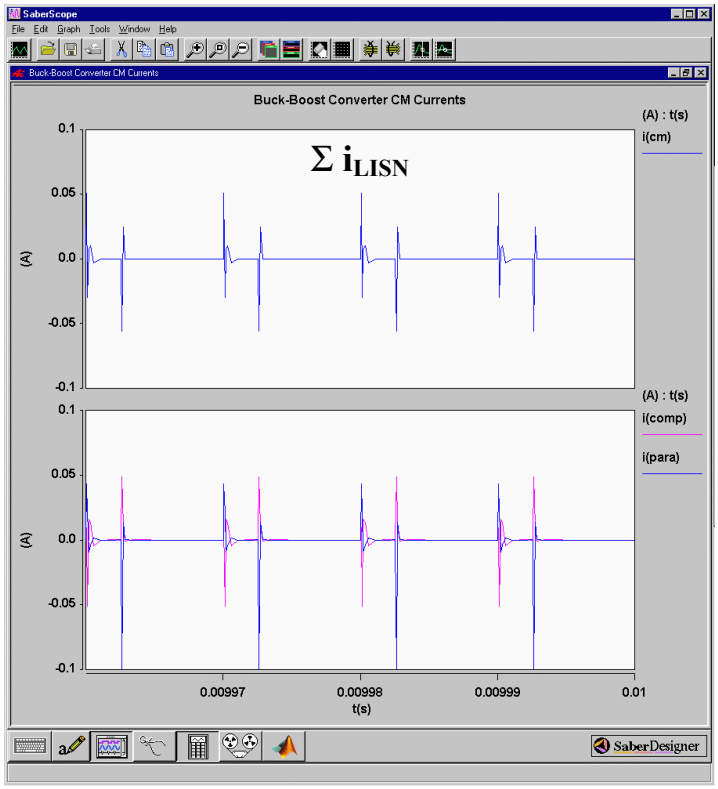

Figure 60: Buck-Boost Converter CM Currents, High Input Capacitor ESL

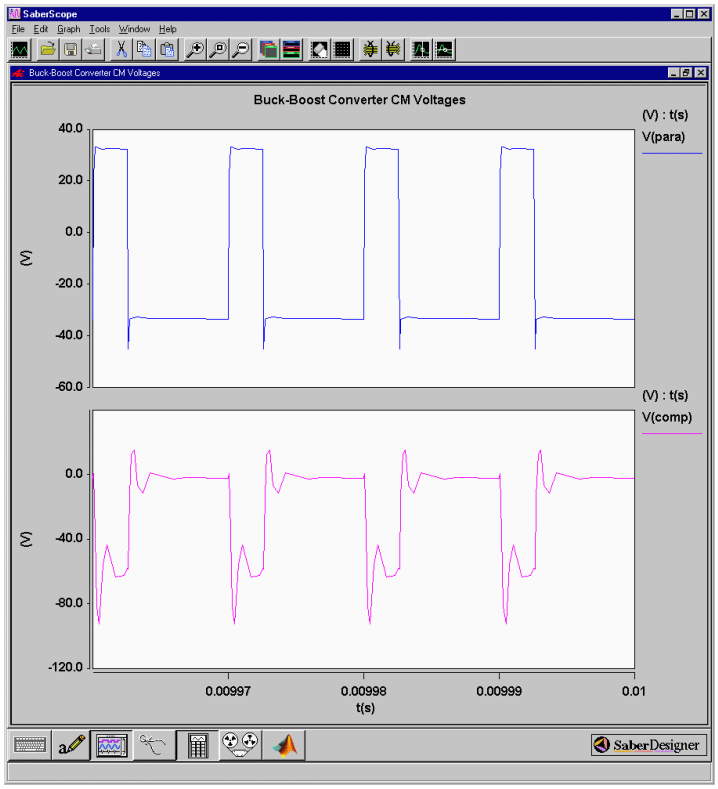

Figure 61: Buck-Boost Converter CM Voltages, High Leakage Inductance

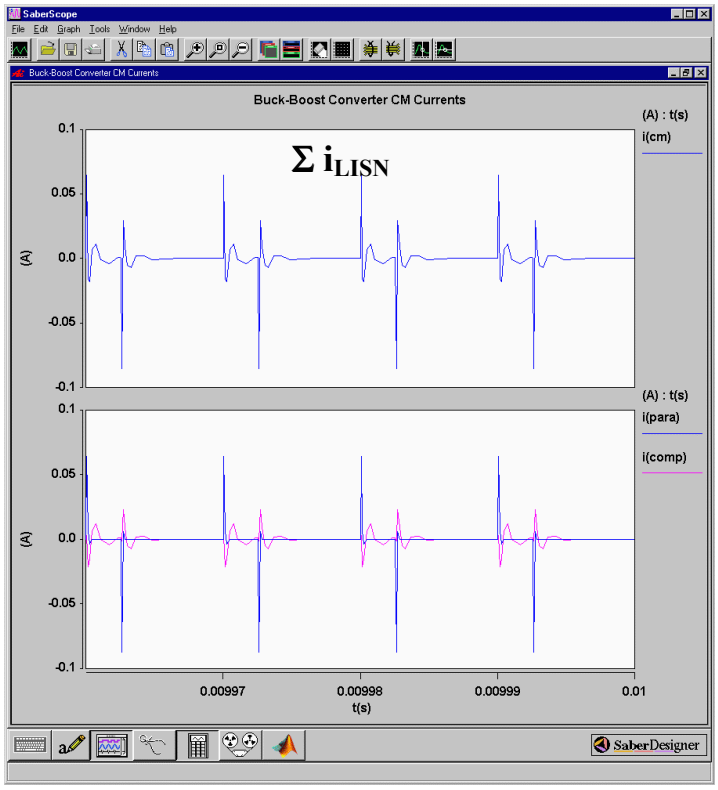

Figure 62: Buck-Boost Converter CM Currents, High Leakage Inductance

Figure 59 through Figure 62 show the reduced performance under conditions of high input capacitor ESL (100 nH) and high transformer leakage inductance (10%). This is nearly identical to the situation with the buck converter in the first section, and as before the explanations and solutions are the same.

Various load conditions were tested in this model, and the performance noise cancellation circuitry appears to be load independent so long as steady-state conditions are present.

4.4. Remarks

As was the case for the isolated topologies presented in the last chapter, it is an easy and simple task to incorporate passive noise cancellation into the most common families of non-isolated power converter topologies. While the work has not been done at this time, it should be expected that this could easily be extended to less common topologies such as the Cuk and SEPIC. While the limitations of input capacitor ESL and compensation transformer leakage inductance are severe, they are also easily avoided in practice. The magnitude of the leakage inductance on the compensating winding is a problem not easily corrected, but for these converters the size of the magnetics is such that this problem should not occur (200 nH at 0.1% leakage inductance yields a maximum inductance of 200 μH, not a value likely to be encountered in typical converter designs). The problem with extreme duty cycles is also one that cannot be corrected, but unlikely to be encountered under normal steady-state operation.

The results from the boost converter experiment performed by Wu Xin and others were somewhat surprising to the author. Upon reflection, however, it is evidence that with more careful construction and attention to details there is much room for improvement in the peformance of the noise cancellation results of Chapter 3. These authors were presumably more focused on this particular boost converter topology, and consequently spent more time and effort on it. My own work is much more broad and out of necessity much less time was spent on any one topology. This should be kept in mind by anyone who is considering the incorporation of these devices into a commercial power converter.

Chapter 5. Proposed Passive Cancellation in DC/AC Inverters and Motor Drives

In this chapter the methods of passive cancellation will be applied to various inverters topologies. Two techniques for passive CM noise cancellation are presented. The first method utilizes the output filter to achieve CM cancellation, and the second introduces a self-contained "cancellator" which is incorporated into the phase legs of the inverter. Performance, advantages, and disadvantages of both techniques will be discussed and commented upon. Examples of these techniques will be applied to a single-phase half-bridge voltage-sourced inverter (VSI) and a three-phase, three-leg VSI.

5.1. Method 1: Modifying the Output Filter

5.1.1. Description of Technique and Model Results

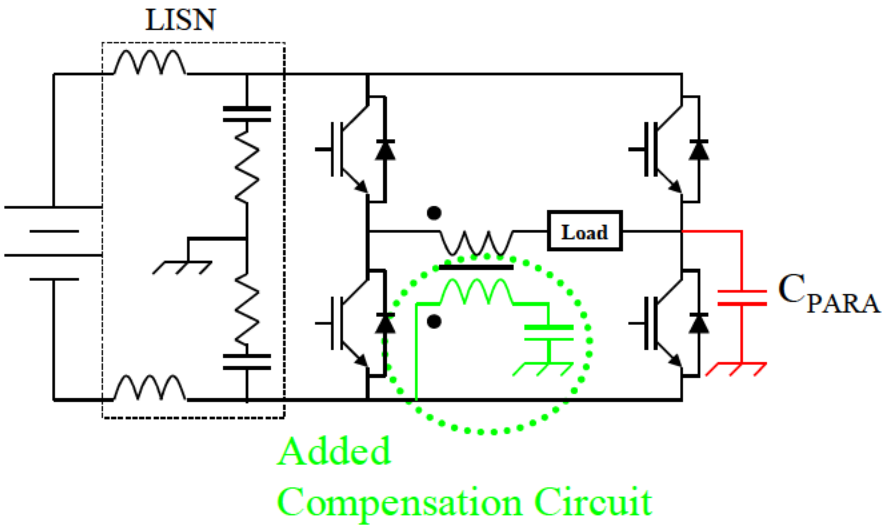

Figure 63: Inverter CM Reduction by Modified Output Filter

The first method of canceling the CM noise in an inverter is shown above in Figure 63. It should be apparent that the bridge elements will see the switching transients and since the inverter often includes some sort of filter inductor this should be a good spot to incorporate the noise

cancellation circuitry. The big question to be answered here, however, is what effect the load will have on the ability of the noise cancellation winding to process the switching $^{dv}/_{dt}$ signal?

In order to look at different combinations of filter inductor and load, the Saber model of a PWM modulated half-bridge inverter was developed and is shown below in Figure 64. The loads for these tests will be based upon an inductive load with a starting inductance of 100 µH, a series resistance of 0.01 Ω, and an interwinding capacitance of 100 nH. The modulation index was chosen to be 0.8 in order to develop 1 kVA at 60 Hz across the load for the given 170 V input. The modulator uses a 20 kHz triangular reference and the blanking circuit was adjusted to give a small amount of dead time to avoid errors related to cross-conduction of the switches. The output filter was arbitrarily chosen to be 50µH and the interwinding capacitance of 1000 pF was selected to give a resonant frequency of ~700 kHz. Other model parameters are the same as those used in previous simulations and need not be repeated here.

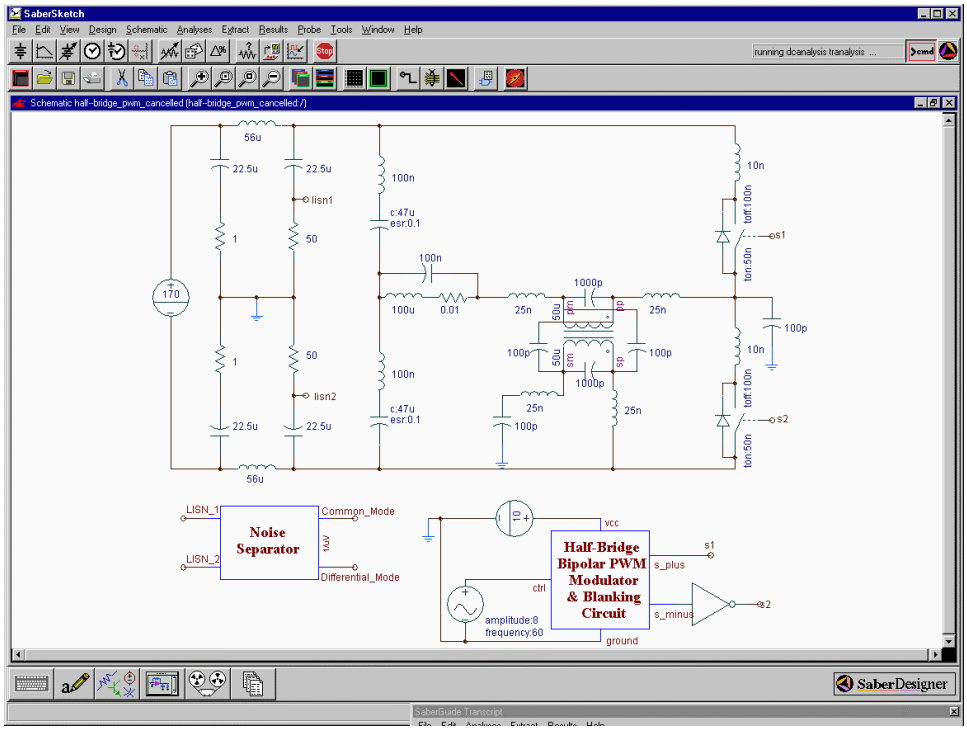

Figure 64: Saber Model for Half-Bridge PWM Inverter Output Filter Test

An FFT of the CM noise voltage across the LISNs is shown below in Figure 65, and the DM spectrum is shown in Figure 66. Cancellation of the fundamental switching harmonic is 13 dbµV, but the second is only 5 dbµV and the next three are actually increased before we see a steady 10—15 dBµV attenuation for the frequencies over ~150 kHz. Results for the DM noise spectrum

are unchanged as expected. While these results show many similarities with the results of previous topologies, we need some explanation for poor performance of the 2—6 harmonics.

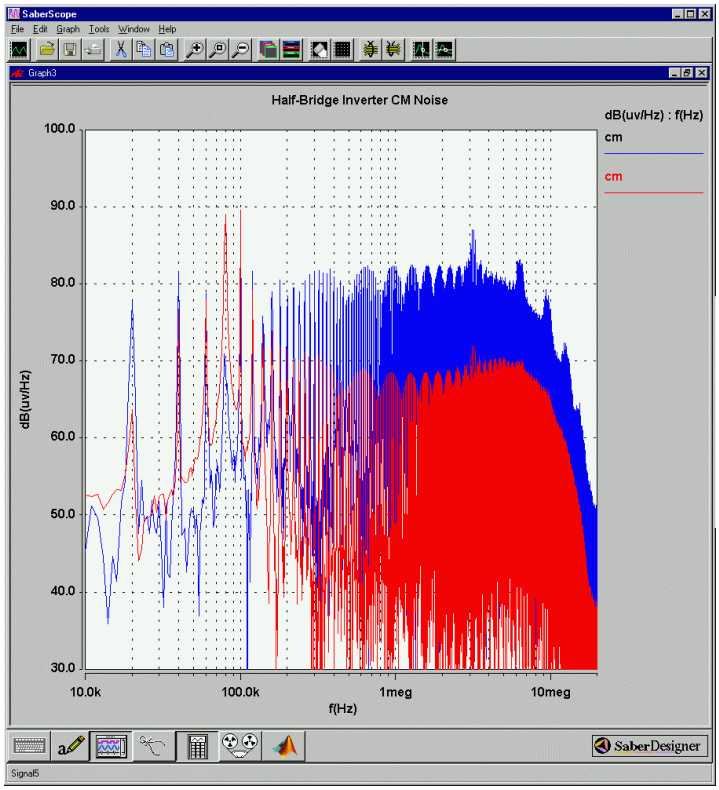

Figure 65: Half-Bridge Inverter CM Noise Spectrum

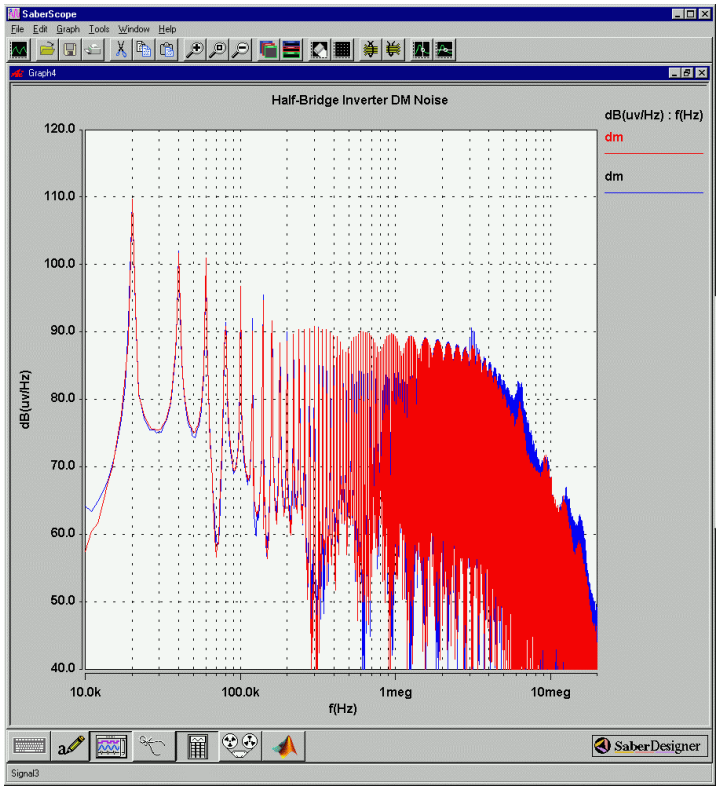

Figure 66: Half-Bridge Inverter DM Noise Spectrum

5.1.2. Limitations Due to Load Interaction

An explanation for this behavior can be realized by some circuit analysis. Figure 67 is the equivalent circuit of the passive elements of the bridge with the secondary-side circuit removed. By finding the transfer function of this circuit, we can see under what conditions the voltage V_f across the filter inductor L_f has a 1:1 gain with the switching waveform V_x.

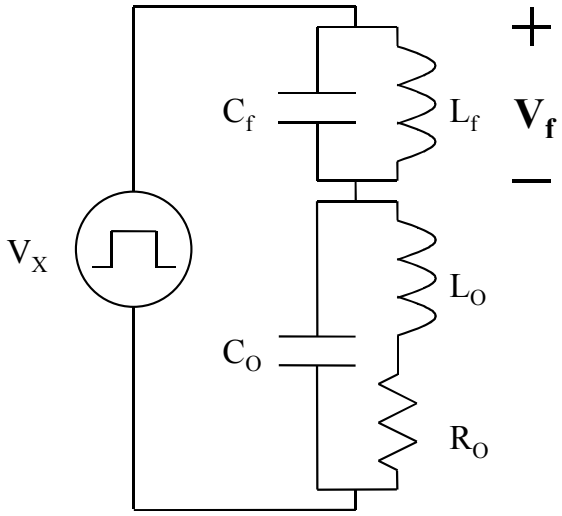

Figure 67: Equivalent Circuit of Half-Bridge Inverter Filter and Load

It is obvious that this circuit can be described as simple voltage divider circuit with the transfer function

$$\frac{V_f}{V_i} = \frac{Z_f}{Z_f + Z_O}, \text{ where}$$

$$Z_f = \frac{sL_f}{1 + s^2 L_f C_f} \text{ and } Z_O = \frac{R_O + sL_O}{1 + sR_O C_O + s^2 L_O C_O}.$$

This transfer function was then plotted in Matlab to show the effect of component variations. Starting with the baseline values of:

$C_O = 100$ nF $\qquad C_f = 1000$ pF

$L_O = 100$ µH $\qquad L_f = 50$ µH

$R_O = 0.01$ Ω ;

the parameters C_O, L_O, and R_O were varied individually to produce the gain and phase plots in Figure 68 through Figure 69. Examining these figures, we can make two observations regarding the effect of the load on the cancellation circuit.

The first observation is that for maximum effectiveness at low frequencies, the impedance of the filter inductor L_f should be much greater than that the load inductance L_O and R_O at the frequency of the switching harmonics for which attenuation is desirable. If this is not possible, then depending on the shape of the transfer function the compensating capacitance can possibly

be increased to yield a higher current pulse for a given voltage—effectively increasing the gain of the transfer function between the switch and C_{COMP}.

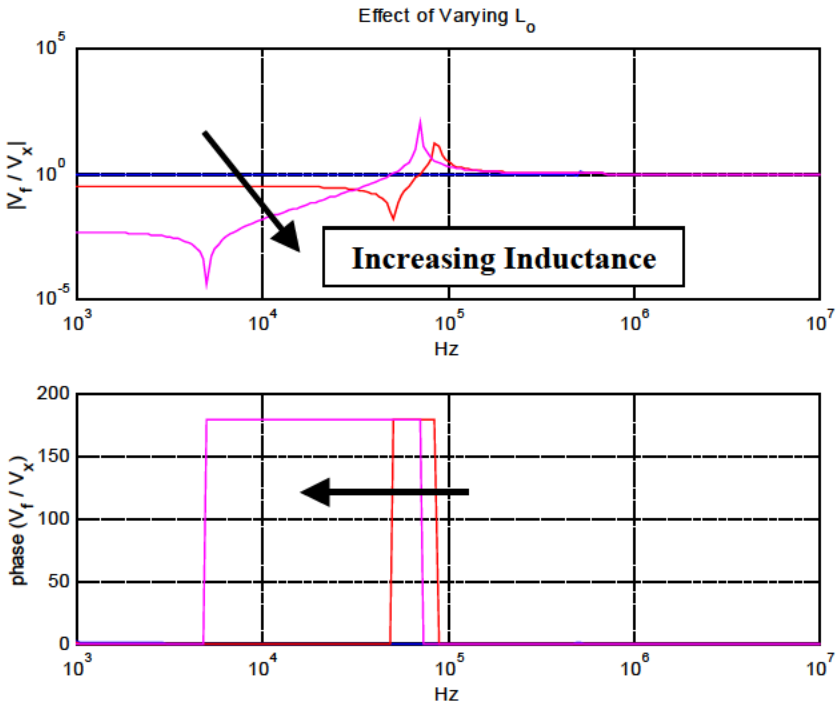

Figure 68: Bridge Transfer Function for L_o = 1µH--10mH

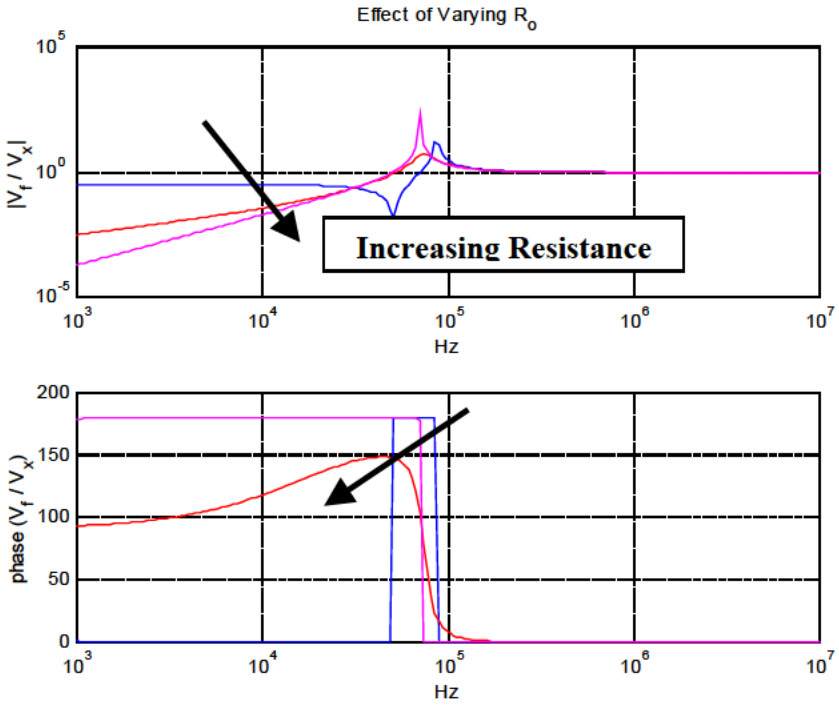

Figure 69: Bridge Transfer Function for R_o = 0.01—100k

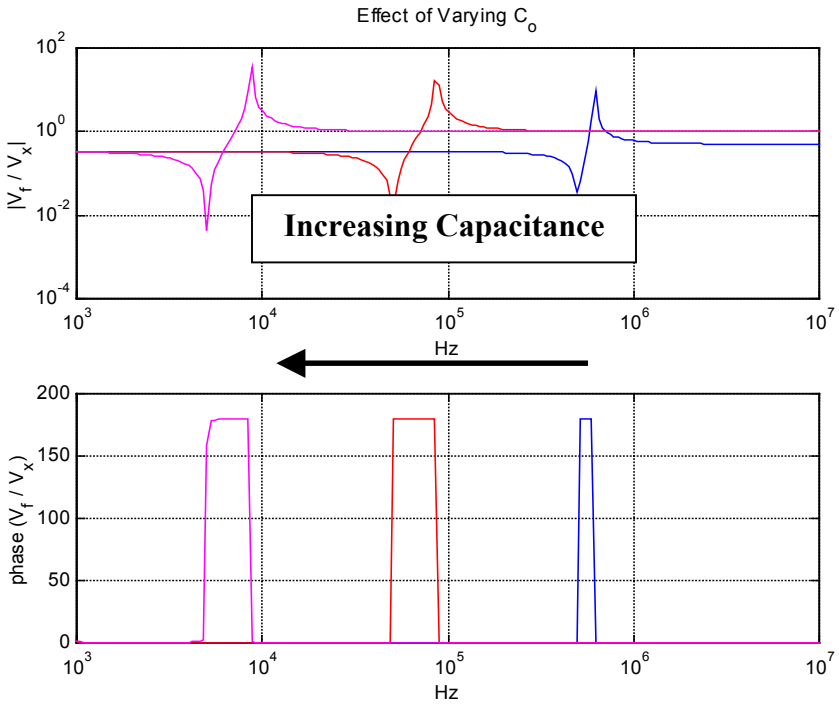

Figure 70: Bridge Transfer Function for C_o = 1nF—10μF

The second observation is that whenever possible, a large C_O should be used to reduce the corner frequencies, as seen in Figure 70. This makes sense intuitively, because C_O effectively shorts out L_O in the high frequency and allows the L_f to see the full switch voltage. This is also an option to use when the impedance of L_f is not greater than L_O and R_O at the desired frequencies.

With these explanations in mind, the CM comparison of Figure 65 is shown again in Figure 71 compared with the phase and gain plots of the bridge transfer function. It is quite clear from this comparison the reason for the increase in the 2—6 harmonics. The phase shift between 50 and 90 kHz nullifies the 180° phase shift in the anti-phase transformer, which results in the anti-noise currents generated by C_{COMP} actually being added to the existing noise currents rather than canceling them. The peak in the gain at 90 kHz only aggravates the problem.

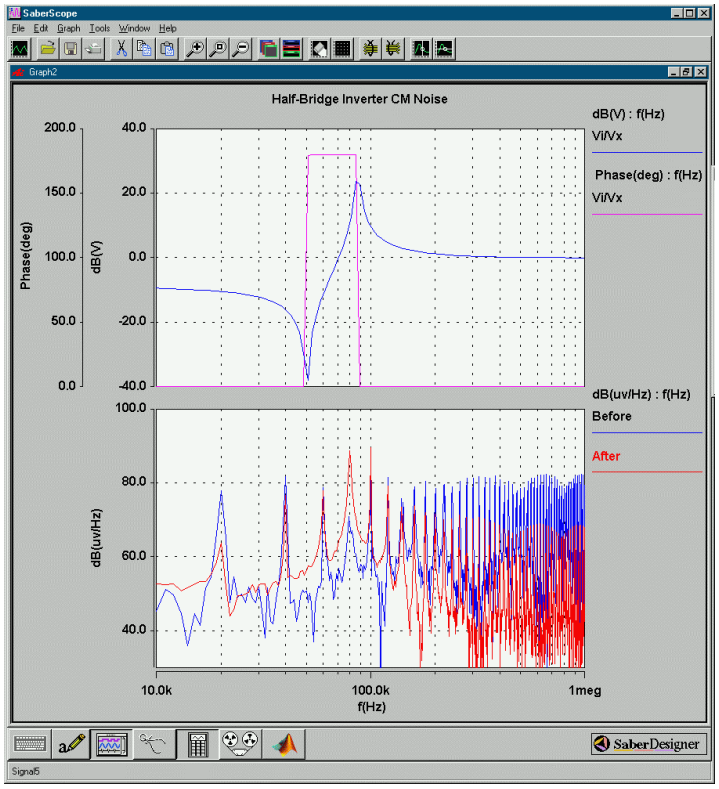

Figure 71: Half-Bridge Inverter CM Noise Spectrum with Bridge Transfer Function

What this means is that this technique will yield good results only when careful consideration is given to what load the inverter is to be tested under for EMI and also what EMI regulation the equipment is to be subject to. For example, if the required specification is MIL-STD-461E (which starts at 10 kHz) then the motivation should be to eliminate the fundamental harmonic to increase the line filter resonant frequency. If we consider the same inverter model as in the above tests, this could be done by increasing the value of C_{COMP} and thus increasing the low frequency gain of the cancellation circuit. Figure 72 shows the effect of doing this. The fundamental is now attenuated by 22 dBµV, but at the cost of increased high-frequency noise. If CISPR specifications (starting at 100 kHz) were now applied to this converter doing this would result in a larger filter than without the cancellation circuitry in place. This would be a good solution for use with MIL-STD-461E specifications, however.

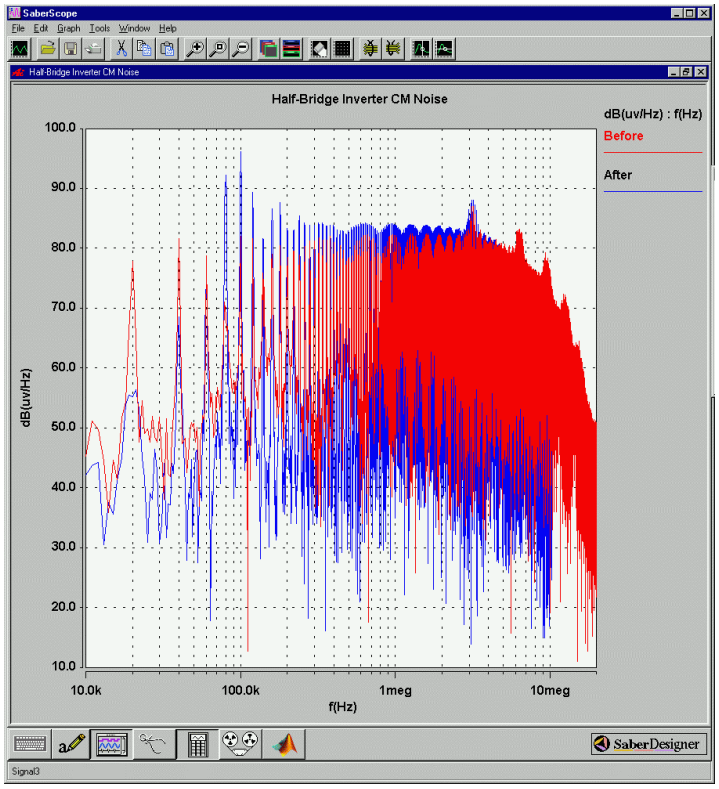

Figure 72: Half-Bridge Inverter CM Comparison with Increases C_{COMP}

As a postscript to this discussion it should be noted that all of the limitations of the previously discussed topologies also apply to this one. Figure 73 and Figure 74 show how cancellation is degraded in the presence of high transformer leakage inductance, for example.

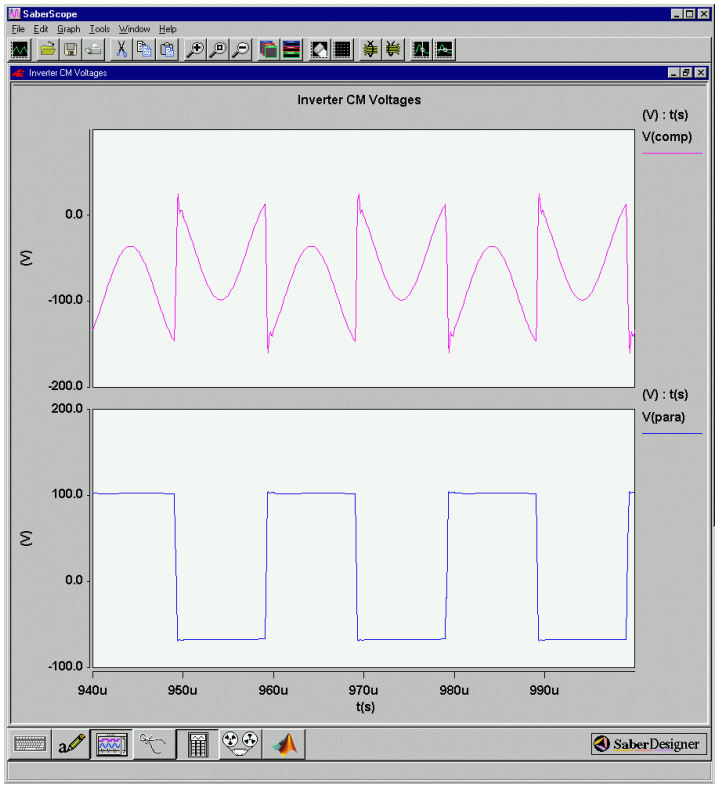

Figure 73: Half-Bridge Inverter CM Voltages, Leakage = 0.1%

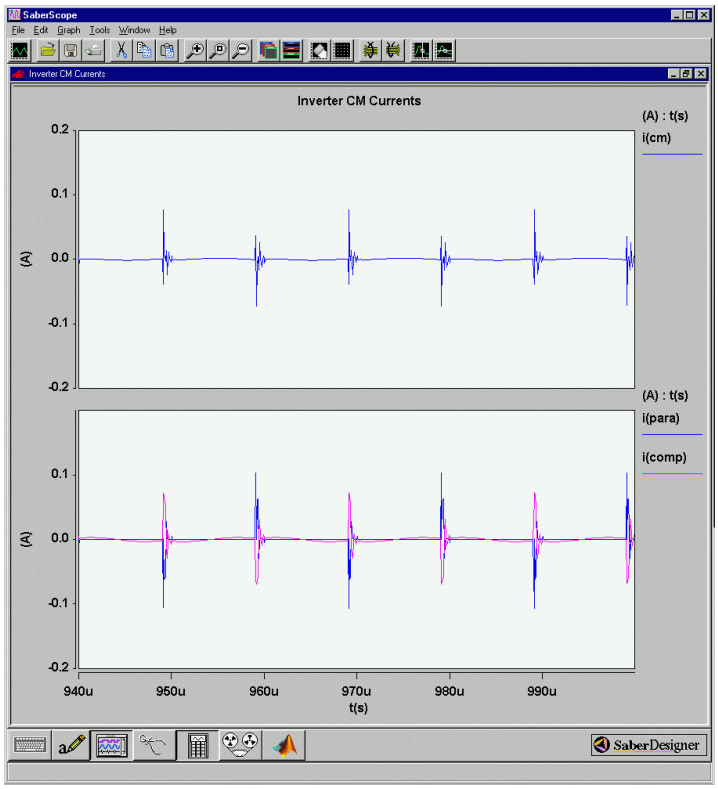

Figure 74: Half-Bridge Inverter CM Currents, Leakage = 10%

5.2. *Method 2: The Phase Leg Cancellation Circuit*

5.2.1. *General Description*

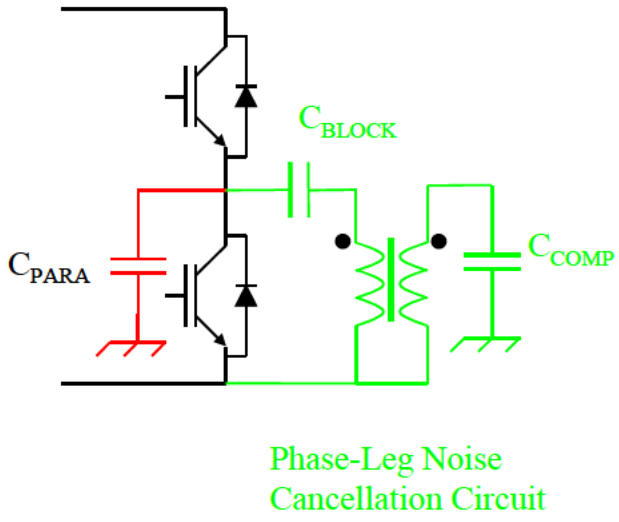

Figure 75: Generic Phase-Leg Cancellation Circuit

Figure 75 shows the basic idea behind the generic phase-leg cancellation circuit, hereafter referred to as the "cancellator". A transformer is placed across the bottom switch of the inverter phase-leg to measure the $^{dv}/_{dt}$ of the switching waveform. This information is then passed to the secondary and shifted 180° out of phase in order for the compensating capacitor to generate the anti-noise current pulses. In order to keep high currents from flowing through the cancellator a series capacitor C_{BLOCK} is added to the circuit to increase the low frequency impedance of the cancellator. This cancellator is not limited to use in inverters, but can in fact be used in any power converter topology simply by connecting the unit across the switch and including appropriate values of C_{BLOCK} and C_{COMP}[31]. A major additional advantage of the cancellator is that it is completely load independent—in contrast to the previous technique and of great usefulness when the converter is intended for use in applications such as uninterruptible power supplies where a wide variety of linear and non-linear loads will be seen.

[31] F. Costa shows how this same cancellator can be applied to a two-switch ZCS forward converter to mitigate the high-frequency CM EMI.

5.2.2. Analysis Using Saber

Before the experimental results are discussed in the next section, it would be useful to first look at some simulated results. Simulation makes it quite easy to see how changes in cancellator parameters, switching frequency, and the like can affect the overall performance of the cancellator. Figure 76 shows the Saber model of a 3-Φ inverter created to test an ideal cancellator. The inverter was modeled with a 10 kHz switching frequency, and had a 100 V DC bus that was modulated at a 0.5 index to produce a 60 Hz, 150 A/Φ output across a Δ-connected inductive load. This cancellator used a 1 μF capacitor with minimal ESR and a linear transformer model with a 1:1 ratio. The transformer model incorporates magnetizing inductances of 10 mH, interwinding capacitance of 100 pF, coil resistance of 0.1 Ω, and leakage inductance of 0.1 μH. C_{PARA} and C_{COMP} were made identical, at 500 pF. Results of simulation show that for this ideal case, the cancellator modules work quite well. Time domain plots of the parasitic and compensating capacitor voltages and currents are shown in Figure 77, while comparisons of the DM and CM noise spectrums are in Figure 78 and Figure 79. The CM spectrum has been reduced by 35 dBμV at the fundamental switching harmonic while the DM spectrum is unchanged, as expected.

While these simulated cancellators work quite well, there are some conditions that must be carefully considered. The first problem is that for a real situation it will be difficult to get a 1 μF blocking capacitor that has a >1 MHz bandwidth. The reason for the large capacitance is to get the resonant frequency of C_{BLOCK} and the transformer magnetizing inductance (1.6 kHz, for this simulation) down below the switching frequency and the low frequency EMI specification. This is because (1) the transformer needs to be able to see the switching frequency without interference and (2) the resonant frequency of this structure will show up on the CM noise spectrum. This is illustrated in Figure 80, where C_{BLOCK} has been reduced to 1 nF, increasing the cancellator resonant frequency to 50 kHz.

The other problem is coil resistance. Figure 81 and Figure 82 show the CM noise spectrum and time-domain waveforms where the resistance of the transformer has been increased from 0.1 Ω to 100 Ω. Figure 82 clearly shows that the increased resistance is acting as a current limiter, reducing the effectiveness of the cancellator.

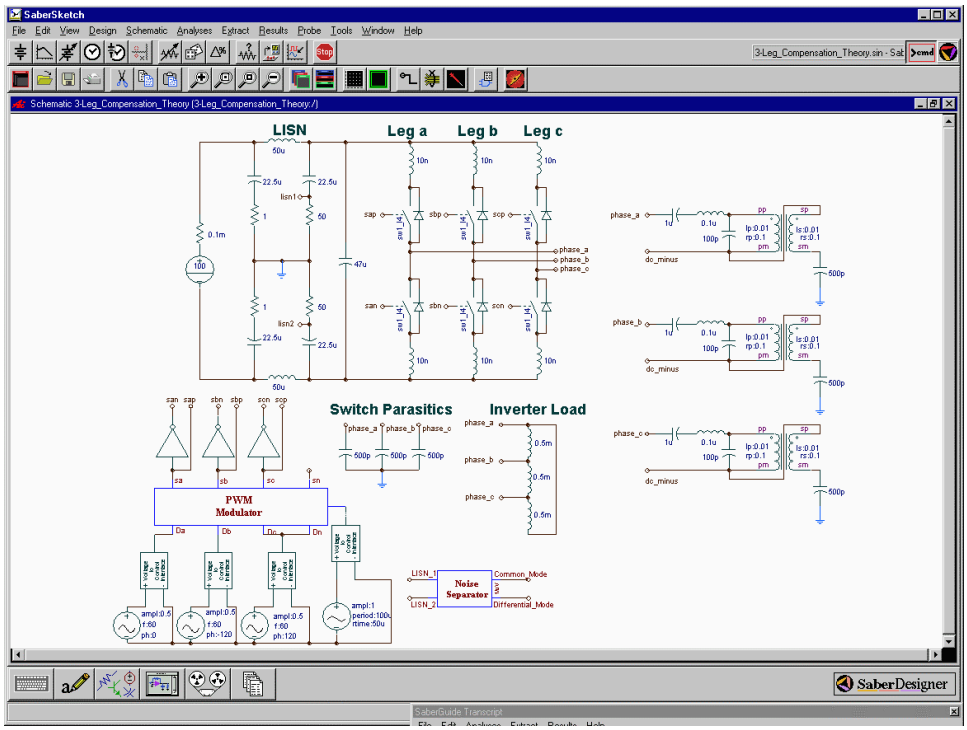

Figure 76: 3-Φ Inverter Saber Model with CM Cancellators

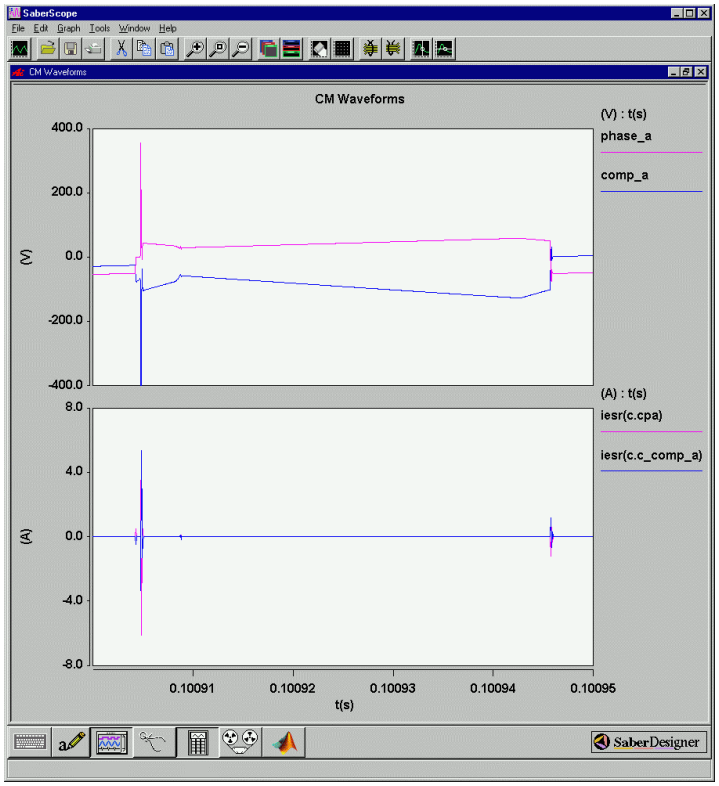

Figure 77: Inverter Parasitic and Compensating Waveforms with Non-Ideal Cancellator, High R_{COIL}

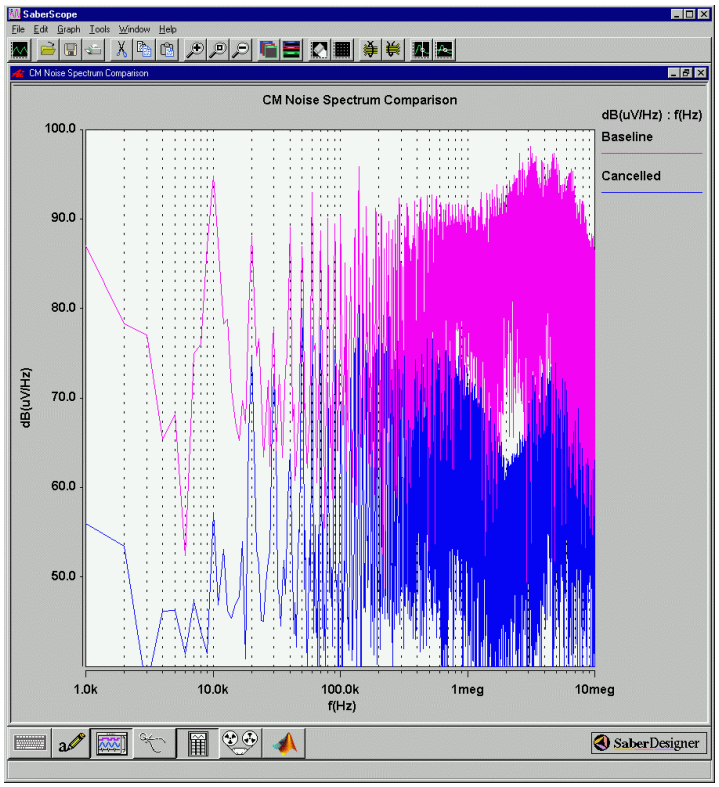

Figure 78: 3-Φ Inverter CM Noise Spectrum Comparison with Cancellator

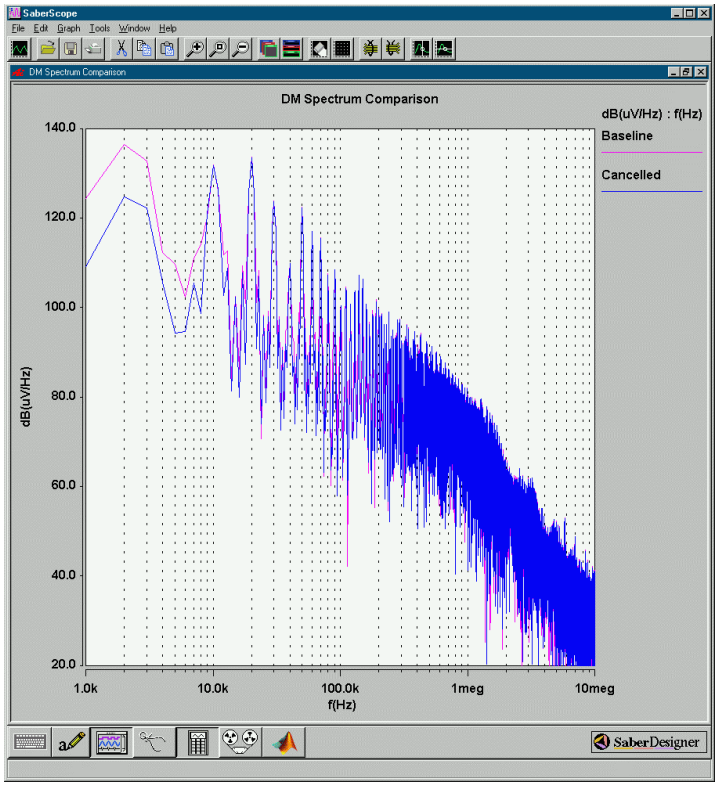

Figure 79: 3-Φ Inverter DM Noise Spectrum Comparison with Cancellator

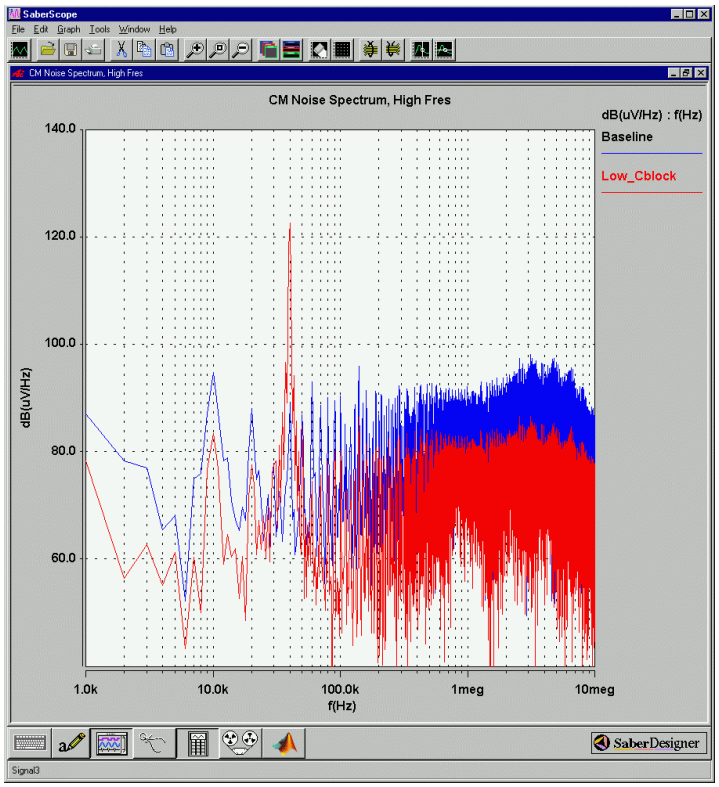

Figure 80: 3-Φ Inverter CM Noise Spectrum Comparison with Cancellator, Small C_{BLOCK}

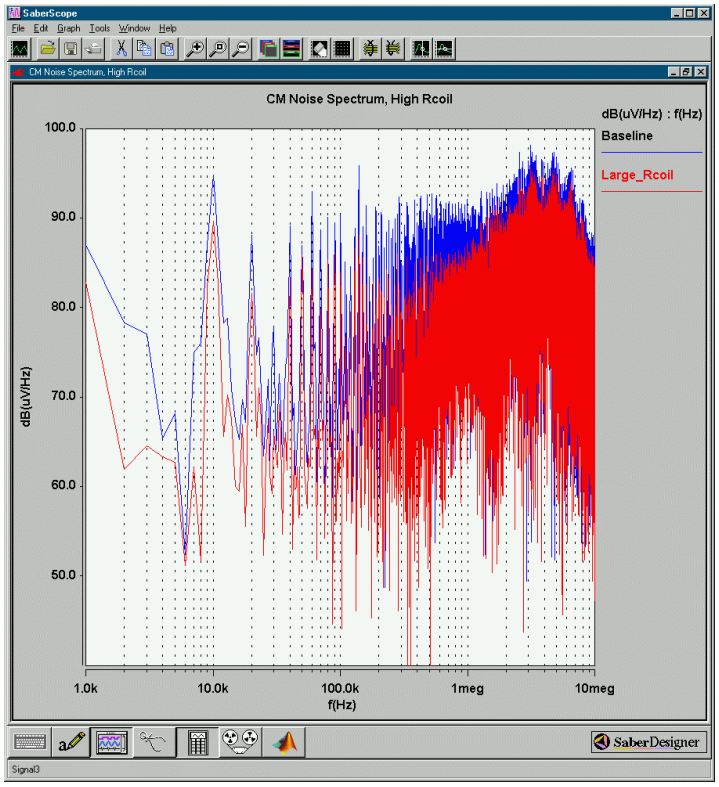

Figure 81: 3-Φ Inverter CM Noise Spectrum Comparison with Cancellator, Large R_{COIL}

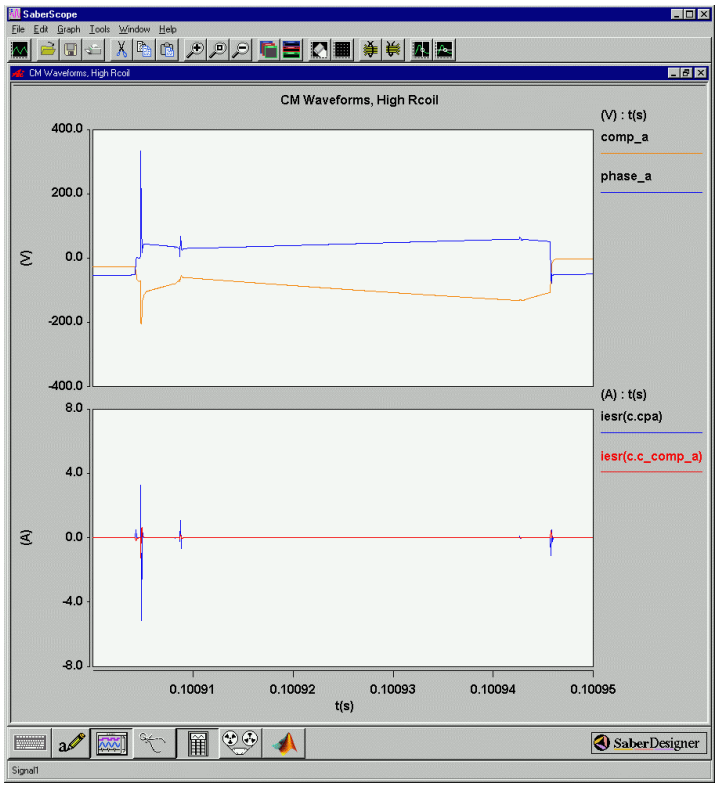

Figure 82: Inverter Parasitic and Compensating Waveforms with Cancellator, Large R_{COIL}

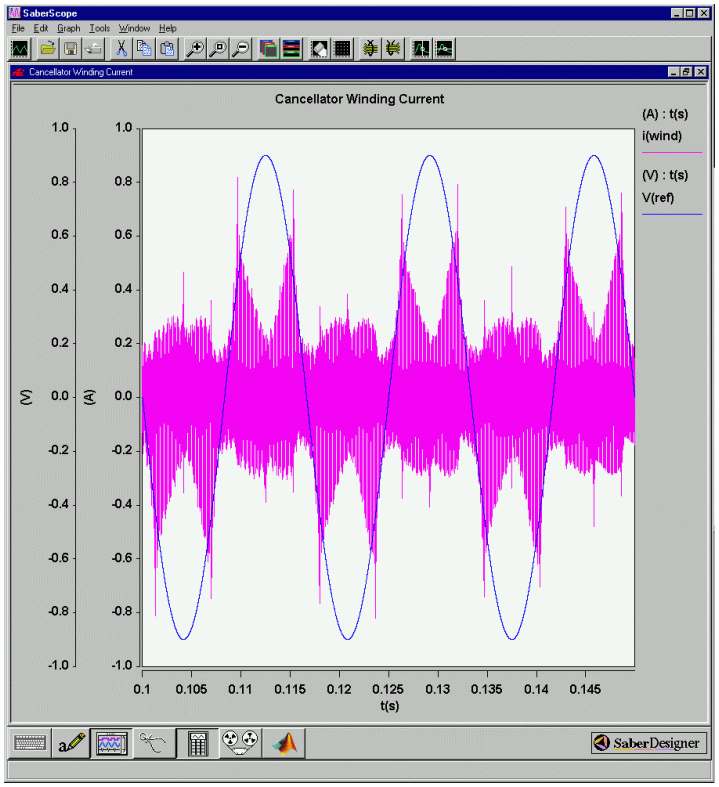

Figure 83: Cancellator Sees 60 Hz Inverter Output Frequency

Unfortunately in the case of inverter applications, the use of the blocking capacitor means that the transformer will see the inverter output line frequency in addition to the switching frequency, as illustrated in Figure 83. Because of the need to minimize coil resistance, this means that a high flux must be able to be tolerated by the transformer and thus common ferrite materials ($B_m \sim 0.3$ T) cannot be used. Cheap silicon-iron materials have the high saturation flux density required, but high-frequency core losses will adversely affect the converter efficiency as well as introducing reliability problems due to excessive heating of the transformer. More discussion about transformer materials will follow in the next section.

5.2.3. Construction of the Experimental Cancellators

For these experiments, two core materials were tested for use in a 3-Φ, 3-leg inverter. The first is the well-known amorphous material "Metglas" available from Allied-Signal/Honeywell. This is advertised to have a saturation flux density of 1.5 T and reasonable core losses at the 10 kHz inverter switching frequency.

The second is a very commonly available material—air. So long as sufficient inductance is present to pick up the switch transitions this material should work fine. Since the blocking capacitor blocks the low frequency currents the normal drawback of transformer saturation should not be a problem. The problem is how the wide-ranging flux fields are going to interact with the inverter control circuitry and gate drives. Unfortunately there is no easy way to simulate these interactions, which makes the experimental evidence critical to the evaluation.

The Metglas transformers were designed using W. McLyman's area product method[32]. The maximum flux of 1.5 T was selected in order to keep the core from saturating, and the #30 AWG was chosen in order to keep the size of the core small and also due to the availability of a large amount of the wire in the lab. Based on these results, a number of AMCC-25 C-cores and their corresponding bobbins were obtained from Allied-Signal. A summary of the transformer parameters can be seen below in Table 8 and the core parameters in Table 9. Photographs of the completed cancellator are below in Figure 84. The peak voltage of 150 V was selected to account for LC resonant overvoltage of the 100 V DC bus voltage. The pulse response of the cancellator to a 15 V, 10 kHz square-wave input using an HP33120A function generator can be seen in Figure 88. The response on the output looks good, although there is an attenuation of

[32] This method is explained in detail in McLyman, pg. 115-130

approximately $^1/_3$. This is most likely due to the resistance of the coil. Although not shown, the cancellator was able to follow the input pulse up to a frequency of 750 kHz.

Table 8: Metglas Transformer Design Details

Peak Voltage	150 V
RMS Current	0.1
B_m	1.5 T
Turns Ratio	1:1
Required Turns	1550
Wire	#30 AWG
Core	AMCC-25
Core Window Utilization	30 %

Table 9: AMCC-25 Core Information

A_C	2.7 cm^2
W_A	8.4 cm^2
Magnetic Path Length	19.6 cm
Mean Turn Length	12 cm
Mass	0.38 kg
Volume	52.3 cm^3

Air core design was comparatively trivial. A bobbin was found in the lab stores that gave a similar cross-sectional area similar to that of the Metglas core and 200 turns of #30 wire was wound on it to keep the resistance small. The maximum flux of the core was found by:

$$B_m = \frac{V}{4 f_s A_C N} \cdot 10^4 = \frac{150\ V}{4(60\ Hz)(1.95\ cm^2)(200)} \cdot 10^4 = 16\ T$$

The other components of the cancellator were chosen as follows: An HP4194A impedance analyzer was used to measure the capacitance between the IGBT phase-leg module and the inverter case at 700 pF. Since it is assumed that this capacitance is distributed evenly across the package, this would make each IGBT C_{PARA} equal to 350 pF. Therefore a 200 pF and a 150 pF high-voltage capacitor were used for C_{COMP} in all the cancellators. C_{BLOCK} was chosen to be 56 nF for the Metglas cancellators to allow the low frequency line currents to be blocked while allowing the switching harmonics to be seen across the transformer primary. 2 27 nF Phillips MKP high-frequency polypropylene capacitors were used to make up C_{BLOCK}. The impedance spectrum of the cancellator primary can be seen in Figure 86, where the second resonant frequency is at 400 Hz. Choosing C_{BLOCK} for the air core cancellator was more problematic because the much lower transformer magnetizing inductance of 430 μH demanded a very high capacitance (millifarads) to yield the same resonant frequencies. Since it is impossible to get high-frequency capacitors of such large values, a compromise had to be made. Therefore 3 56 nF MKP capacitors were chosen, yielding a second resonant frequency of 144 kHz seen in the impedance plot of Figure 87. While this choice would most likely result in little to no low frequency noise cancellation, it was

expected that there should still be some CM attenuation at frequencies above 100—200 kHz. This still allows the concept to be proven while leaving open the possibility for future improvements.

Photographs of the air core cancellators as well as a size comparison with the Metglas cancellators are shown below in Figure 85. The pulse response of the air core cancellator is seen in Figure 89. It is quite clear that the low inductance does not allow the full pulse information to be transmitted from input to output. However, the high-frequency $^{dv}/_{dt}$ part of the waveform does get transmitted so this will still allow a degree of cancellation to take place.

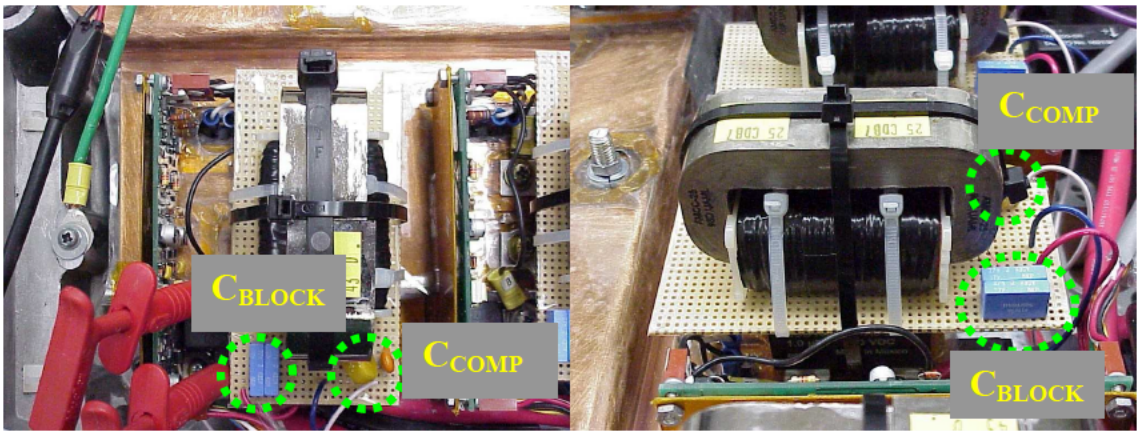

Figure 84: Phase-Leg Cancellation Circuit (Metglas)

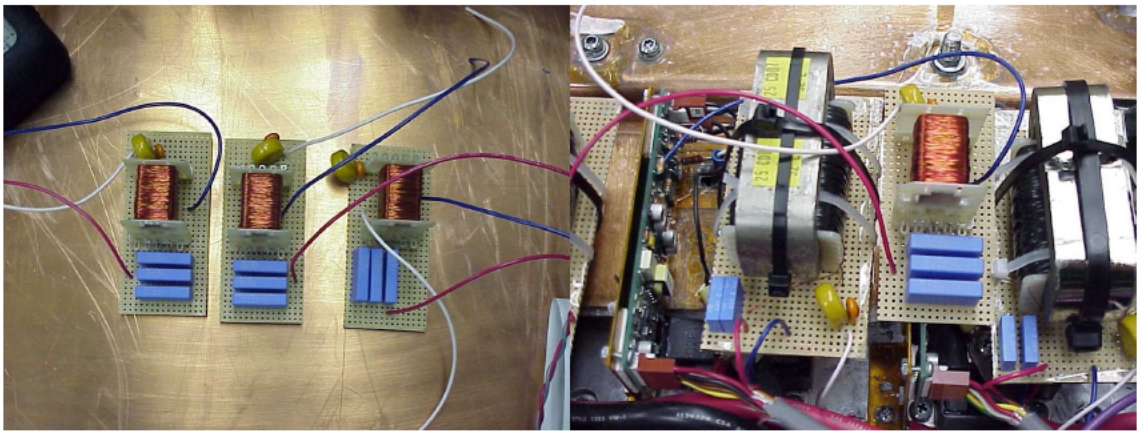

Figure 85: Phase-Leg Cancellation Circuit (Air / Metglas Core Comparison)

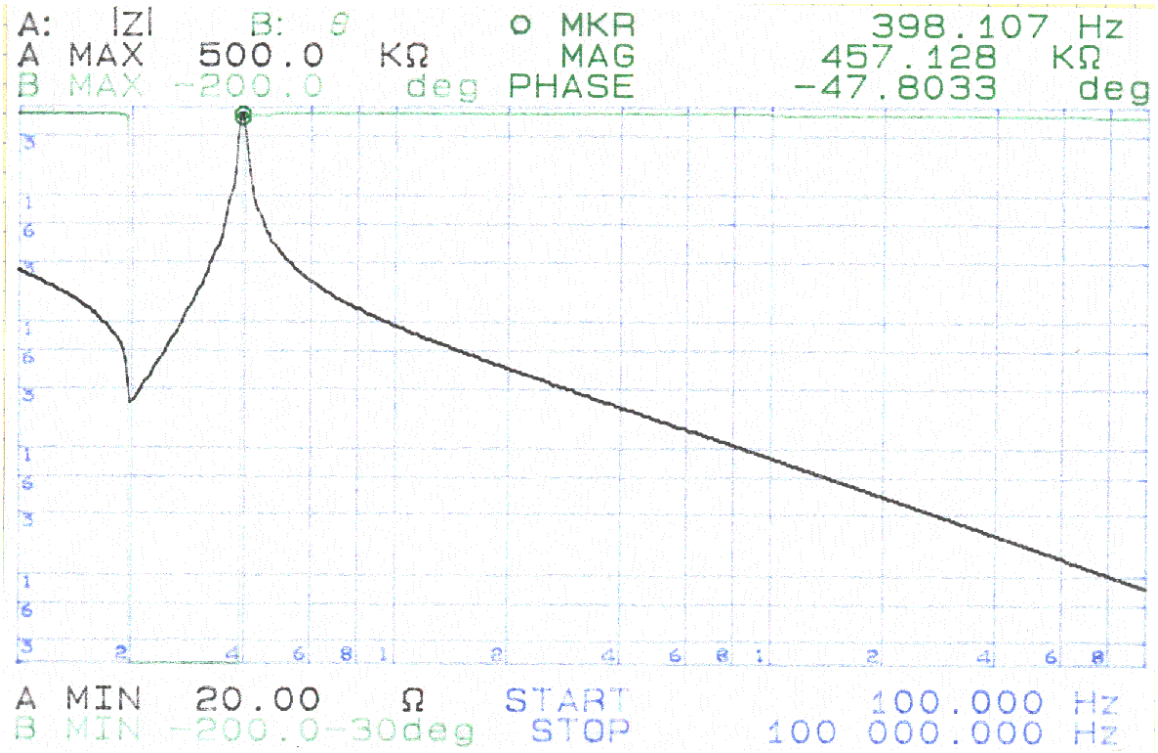

Figure 86: Primary Side Impedance of Metglas Cancellator

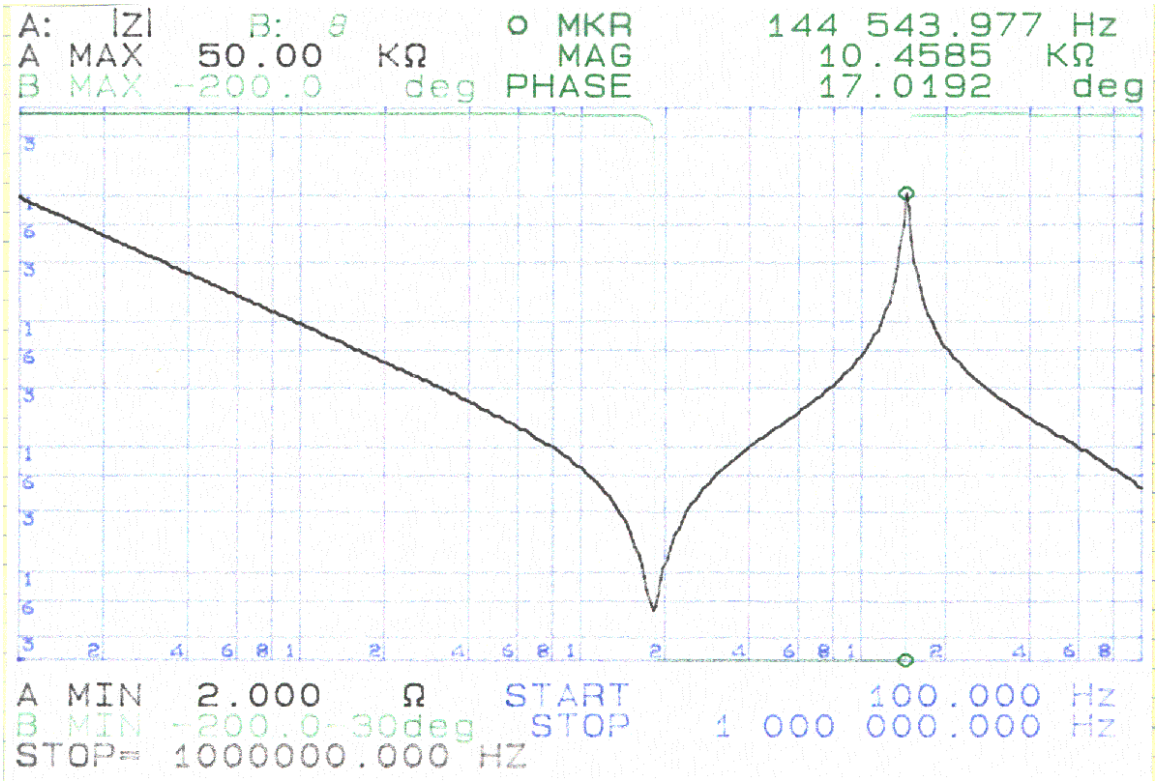

Figure 87: Primary Side Impedance of Air Core Cancellator

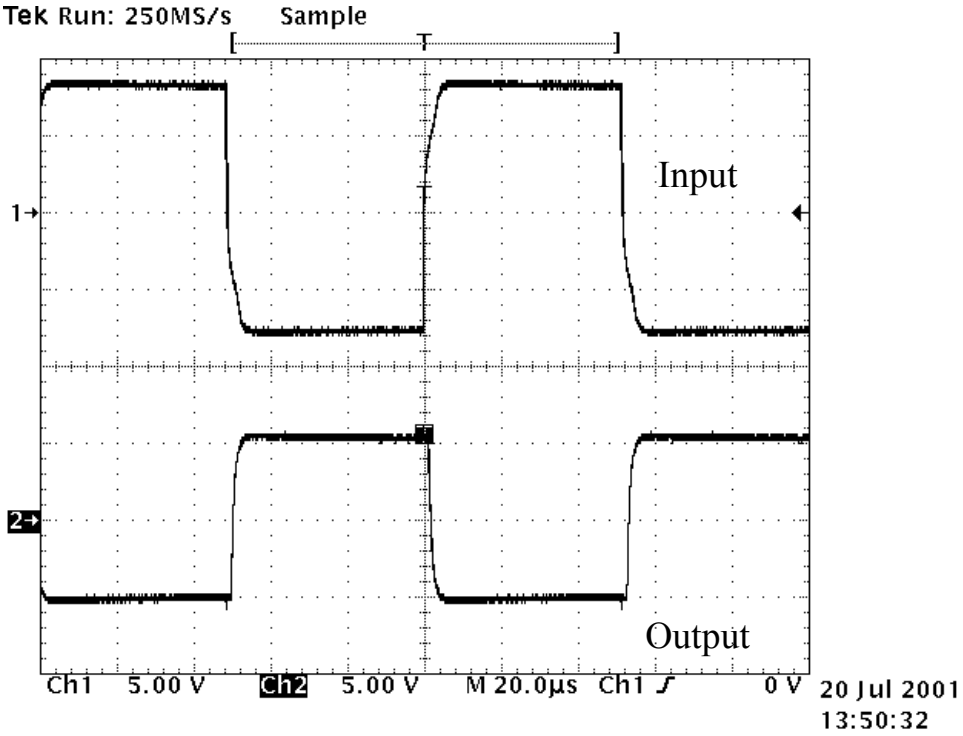

Figure 88: Pulse Response of Metglas Core Phase-Leg Cancellator at 10 kHz

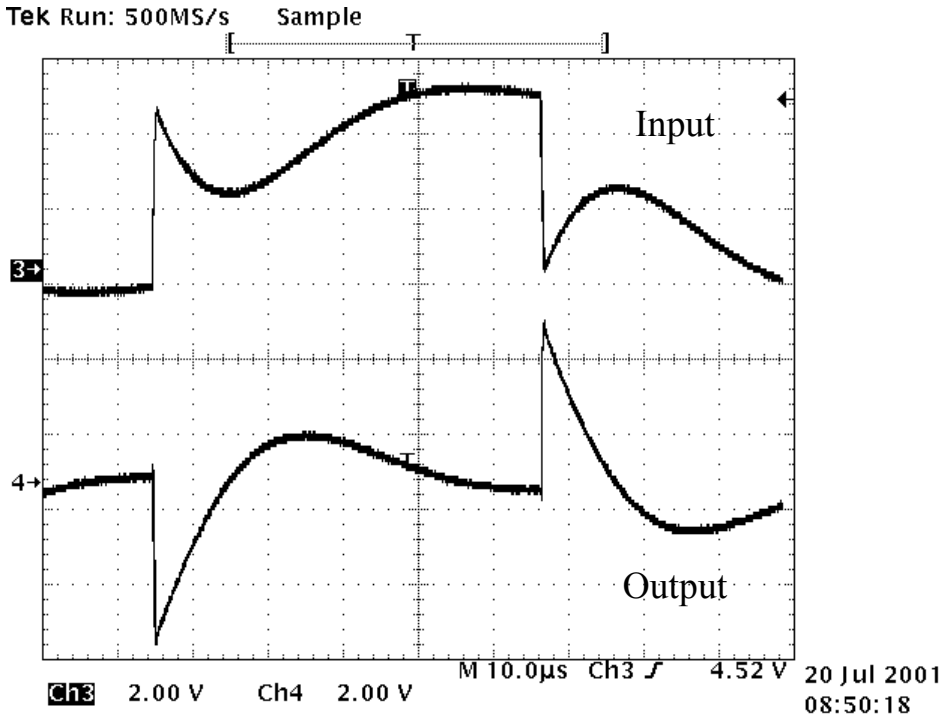

Figure 89: Pulse Response of Air Core Phase-Leg Cancellator at 10 kHz

After the transformers were constructed but before they were placed in the cancellator circuit some of the basic parameters were measured using an HP4194A impedance analyzer. These

results are compared below in Table 10. The unfortunate surprise to come from this was the magnitude of the Metglas coil resistance. The value of 191 Ω was slightly more than three times what had originally been calculated (63 Ω, using the published resistance of $10^{-6}\ \Omega/_{cm}$[33]). The coil resistance acts as a current limiter that prevents the compensating capacitor from producing equal and opposite noise currents from C_{PARA}. The calculated resistance was predicted to still allow measurable cancellation to be seen, but this value was now probably much too large to allow sufficient cancellation to take place. To get down to the original value of 63 Ω required reducing the turns by 3x, which was clearly impossible without letting the core go deep into saturation.

Table 10: Transformer Parameter Comparison

	L_M	L_{Leak}	C_{Wind}	R_{Coil}
Metglas	5 H	77 µH	154 pF	191 Ω
Air	430 µH	2 µH	105 pF	4.7 Ω

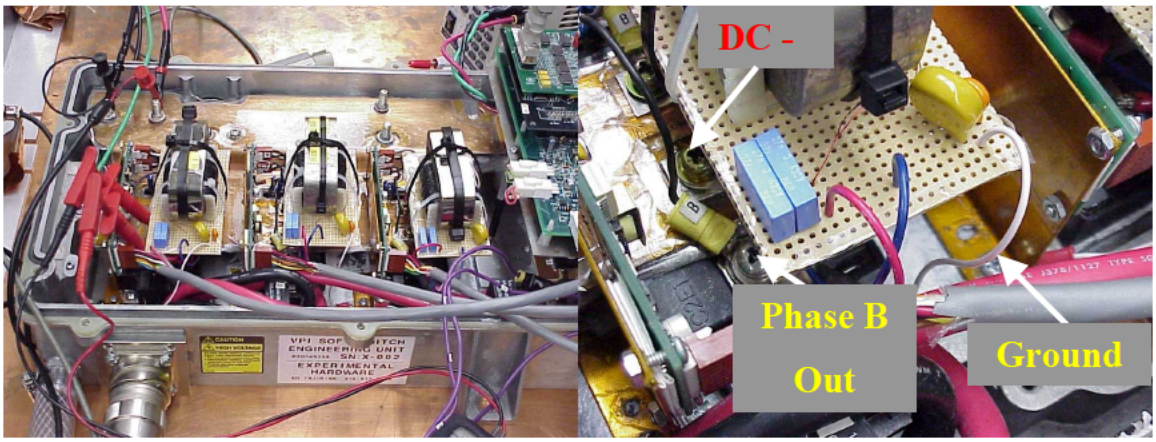

Figure 90: Installation of Phase-Leg Cancellation Circuit

[33] McLyman, pg 254

5.2.4. *Experimental Test Results*

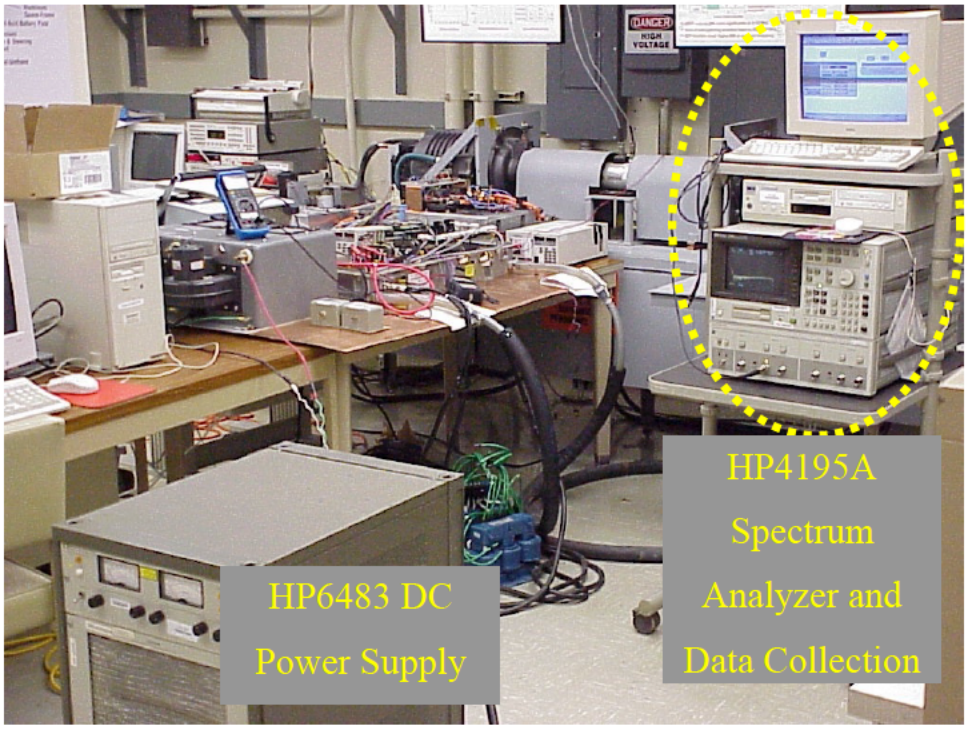

Figure 91: Inverter Test Setup (Right Side)

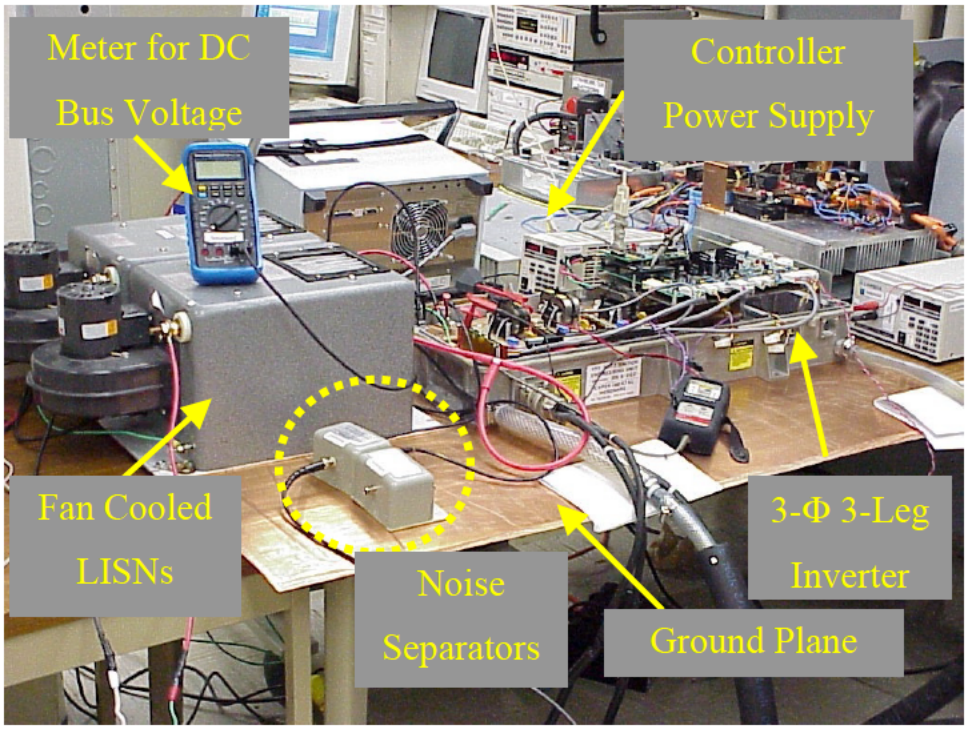

Figure 92: Inverter Test Setup Close-up

Figure 91 through Figure 93 show the experimental test setup for the cancellator circuits. The inverter used for these tests was a VPI Soft-Switch Engineering Unit (S/N: X-002) set up for operation in hard switching mode. Switching frequency was 10 kHz, and the modulation index was set at 0.1 in order to supply 35 A/Φ with a DC bus supply voltage of 100 V. The load for these experiments consisted of 3 0.4 mH inductors connected in a delta configuration. During the actual experiments, a DC bus voltage of 90 V was used because the amperage was slightly higher than expected (42 A) and a bus voltage of 100 V would have caused the load to exceed its rated current value of 45 A. The main power supply was a 600 V / 25 A HP 6483C DC power supply, while a Lambda 135 W DC supply was used to supply power to the inverter control board. Two standard commercial-grade fan-cooled LISNs were used and the whole assembly was placed on a grounded copper sheet.

At the time of these experiments the author was attempting to prove the feasibility of the cancellator for use in military-grade hardware used by the U. S. Navy, and therefore the emissions spectrum was set up for 10 kHz –100 kHz requirement of MIL-STD-461E CE102. The particular spectrum analyzer settings can be seen below in Table 11.

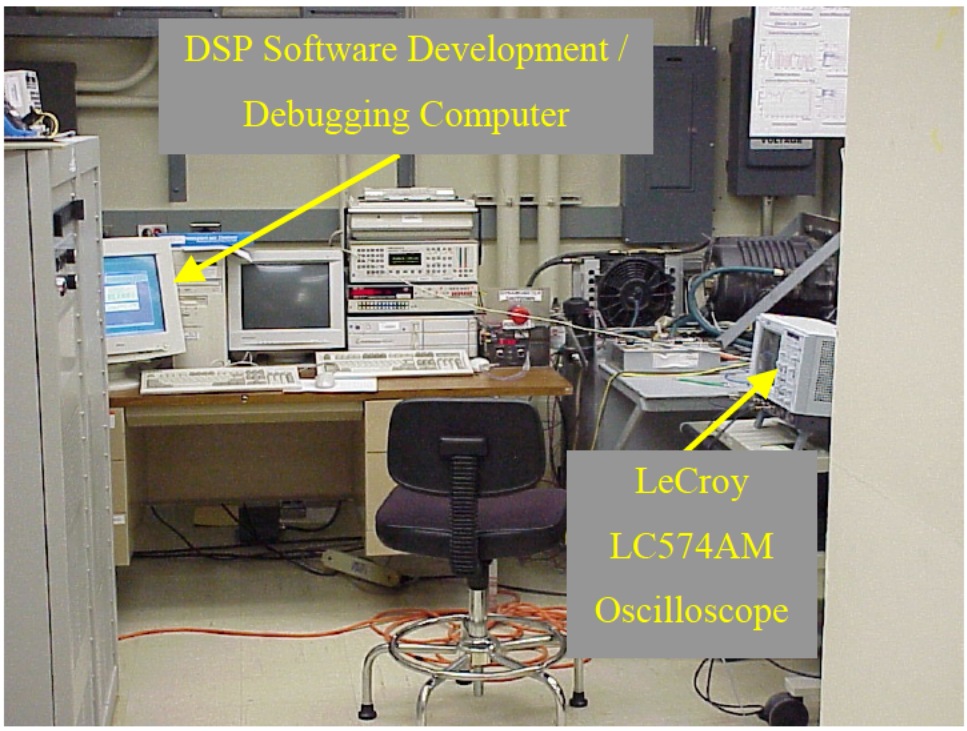

Figure 93: Inverter Test Setup (Left Side)

Table 11: Test Settings for HP4195A in Inverter Experiments

Resolution Bandwidth (RBW)	1 kHz
Start Frequency	10 kHz
End Frequency	10 MHz

Attenuation on Input	50 dB
Video Filter	Off
IF Range	Normal

Before the EMI tests were performed the inverter was checked out to ensure proper operation. Figure 94 shows the control signal sent from the control board DSP along with the phase C voltage and current. Once this was accomplished baseline CM and DM measurements were taken using the noise separators used in previous EMI experiments. Following these measurements the metglas and air core cancellators were installed and subsequent CM and DM spectrums were measured for comparison.

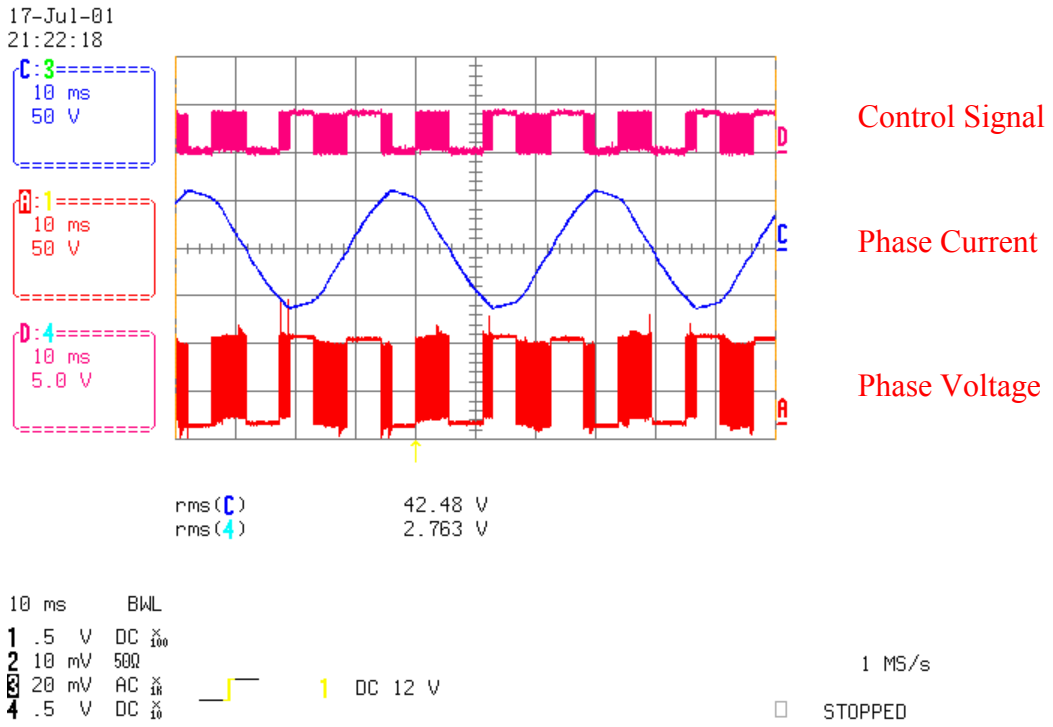

Figure 94: Inverter Power Waveforms

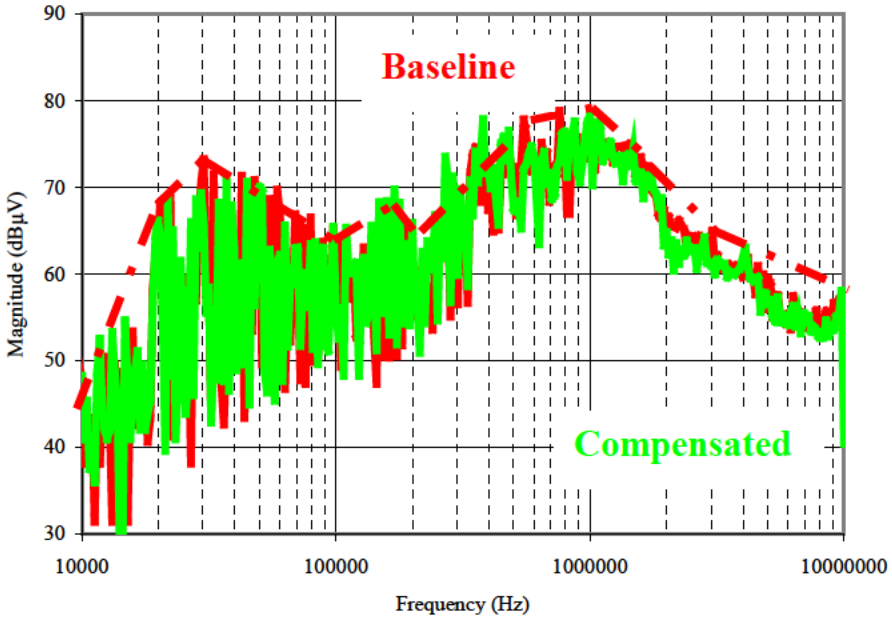

Figure 95: Inverter CM Noise Spectrum (Metglas) is Unchanged

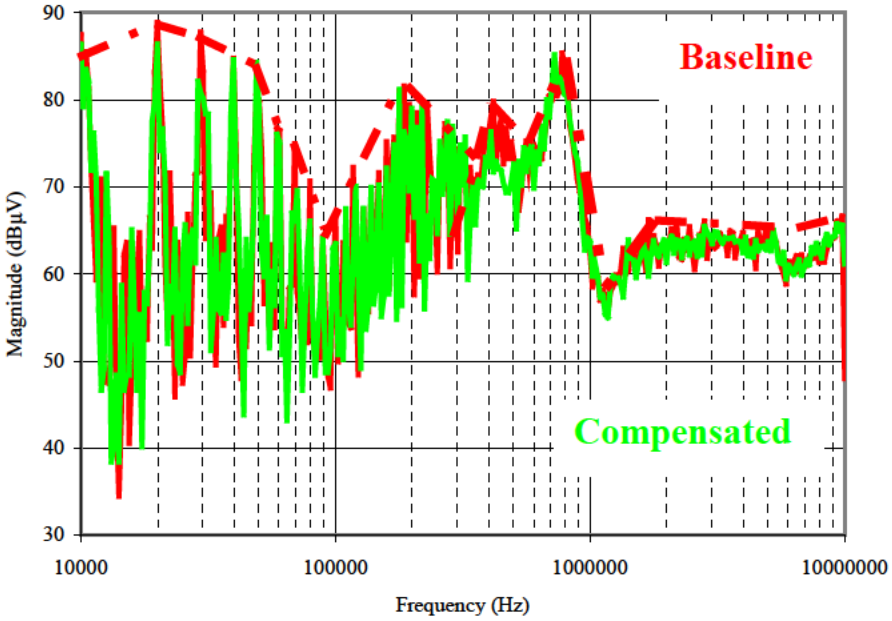

Figure 96: Inverter DM Noise Spectrum (Metglas) is Unchanged

Figure 95 and Figure 96 compare the CM and DM noise spectrums of the inverter using the Metglas cancellators. While using the cancellator does no harm to the noise spectrum, it doesn't noticeably help, either. The metglas cancellator was also simulated using the model previously

introduced in Figure 76 with the measured values of Table 10. Figure 97 shows the parasitic and compensating currents and voltages under these conditions. As expected, the rather large coil resistance limits the anti-noise current magnitude so that it cannot function as desired. Figure 98 shows these same waveforms when R_{COIL} has been reduced from 190 Ω to 1 Ω, and Figure 99 compares the CM noise spectrums for the two cases.

With these thoughts in mind, the author believes that by increasing the core size to an AMCC-40 from AMCC-25 and using #27 wire instead of #30 wire good results could be realized. These results are shown in Figure 100.

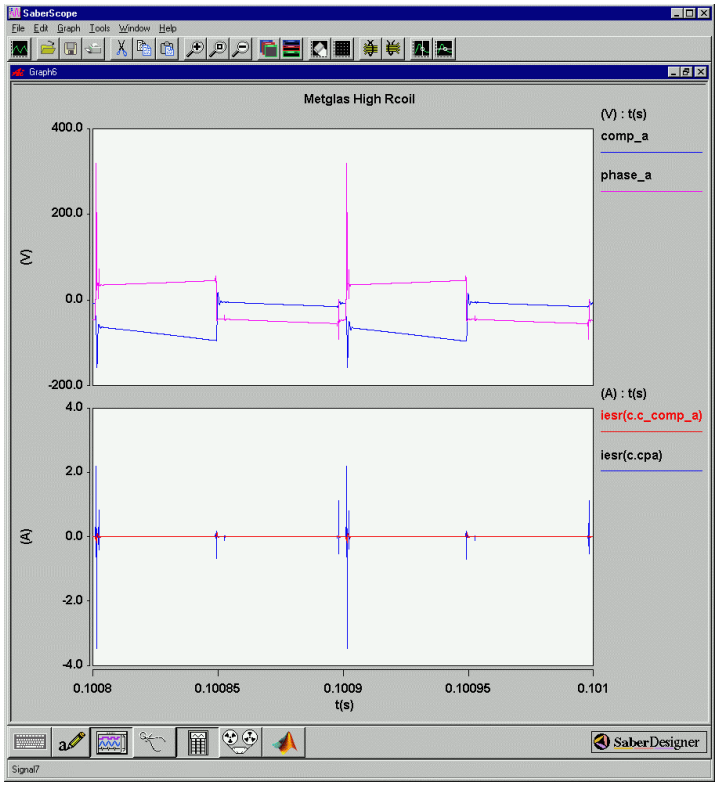

Figure 97: Simulated Metglas Cancellator, High R_{COIL}

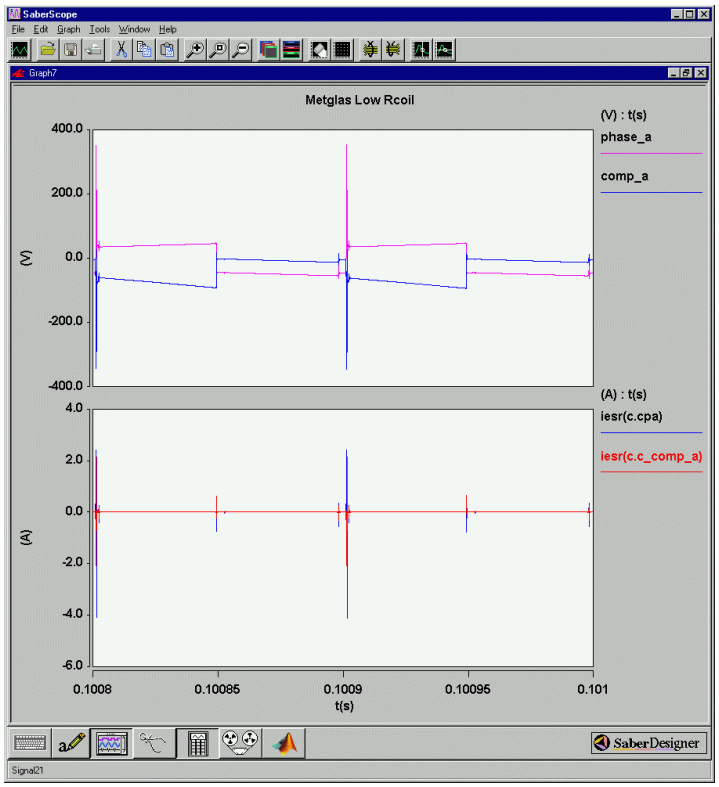

Figure 98: Simulated Metglas Cancellator, High R_{COIL}

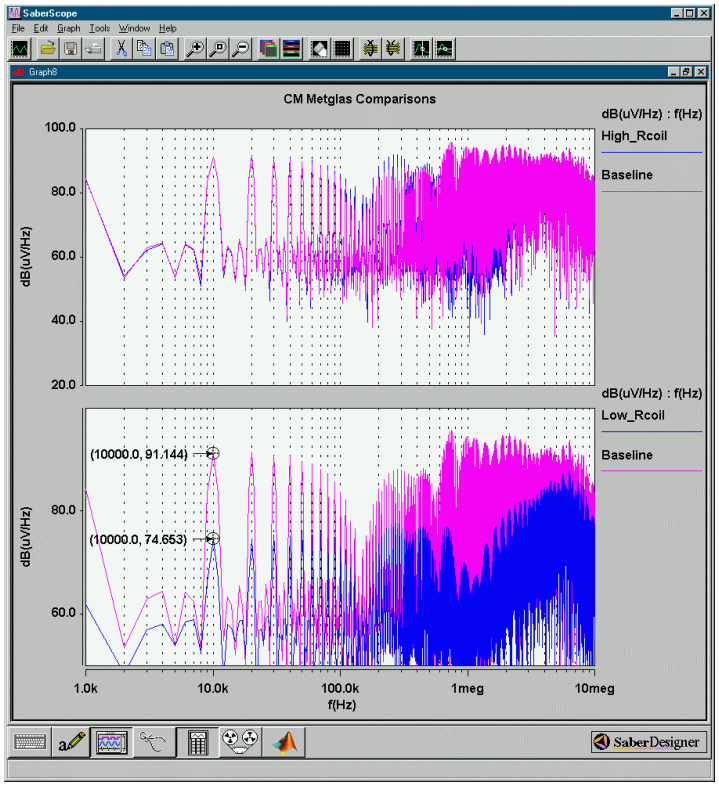

Figure 99: Simulated Metglas CM Noise Spectrum Comparisons

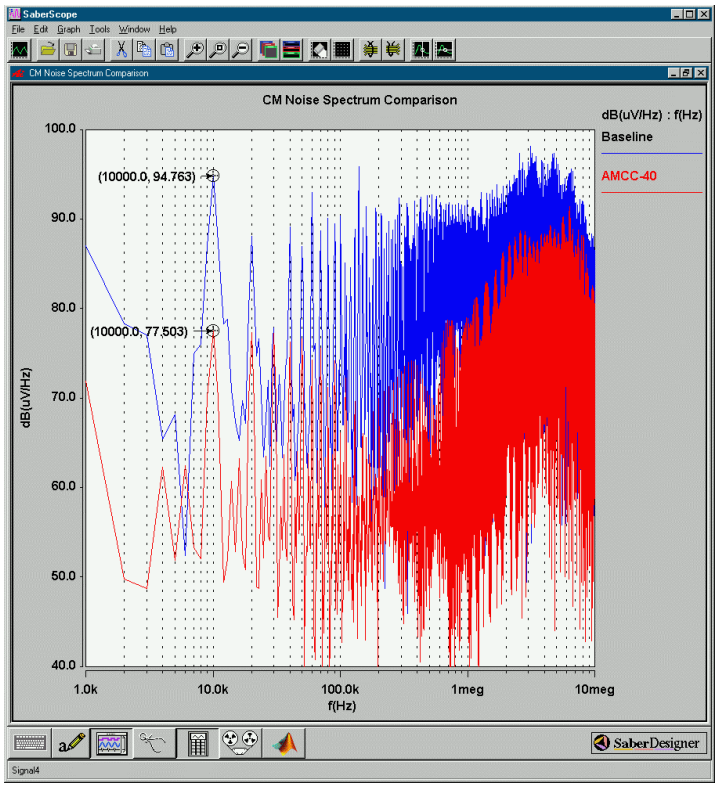

Figure 100: Inverter CM Results with AMCC-40 Core and #27 Wire

Figure 101 and Figure 102 compare the CM and DM noise spectrums of the inverter using the air core cancellators with the baseline measurements. The DM noise spectrum is unchanged as it should be, while the CM noise spectrum is quite interesting. Below 50 kHz there is no improvement due to the location of the resonant frequencies of the cancellator, and above 1 MHz the transformer leakage inductance causes an increase in the spectrum due to the high-frequency ringing also seen in previous experiments. Between 50 kHz and 1 MHz there is some noticeable improvement in the noise spectrum. At 100 kHz there is 10 dBµV of attenuation while at 400 kHz there is 14 dBµV of attenuation. While the results in the low frequency portion of the spectrum are somewhat disappointing, there is still conclusive evidence that the cancellator technique does work and it is expected that future revisions of the design will be able to extend the benefits to the lower frequencies.

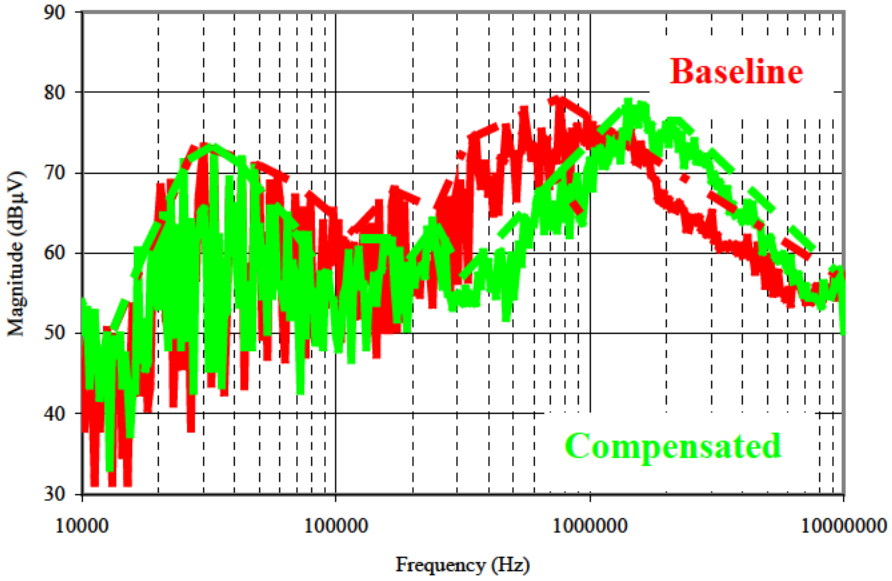

Figure 101: Inverter CM Noise Spectrum (Air Core)

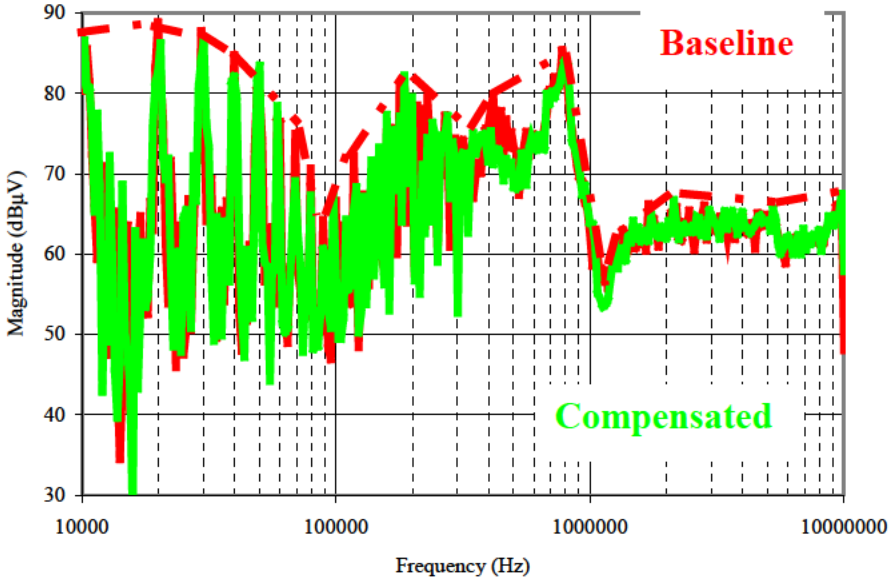

Figure 102: Inverter DM Noise Spectrum (Air Core) is Unchanged

5.3. Remarks

Cancellation techniques as applied to the inverter are something of a mixed bag. The first method, that of using an additional winding on the output filter inductor, can realize excellent results under certain combinations of load and filter. Under other circumstances the technique

works very poorly and can sometimes result in a larger input line filter requirement than without using the technique.

Results from the phase-leg cancellation circuit are best described as good but needing improvement before this technique can be successfully introduced into manufactured power converters. Even using a high B_{MAX} material such as Metglas still requires a bulky circuit because of the need to reduce the resistance of the coils. At the moment only air core transformers can meet the low-frequency requirement without exceeding coil resistance limitations. While no interference was observed in these particular experiments from the large flux fields, this author still has concerns about using these cancellators in a tightly packaged environment. It is also difficult to get good operation below 100 kHz with these cancellators due to capacitor size restrictions and therefore there is little benefit to be gained if the converter has to meet MIL-STD-461E standards starting at 10 kHz (Such was the case with this research). However, the 20 dBµV attenuation seen around the 450 kHz starting point of the FCC standards mean that this technique could be quite useful. As with the first method, the system developer must take careful consideration when deciding to use this technique.

Chapter 6. Conclusions and Future Work

6.1. Summary and Overview

In this thesis a number of techniques have been presented for attenuating common-mode noise currents by small, simple, and cheap passive circuits. Isolated topologies such as the forward, flyback, and bridge converters can achieve results by adding an extra winding in the power transformer and using a small ceramic compensating capacitor. Non-isolated topologies such as the buck, boost, and buck-boost converters can achieve the same results by adding an extra winding onto the output filter inductor.

Experimental evidence shows that the amount of attenuation is between 10 and 15 dBμV for the low frequency harmonics. What does this actually mean in terms of reducing the size of the line filter CM choke? Let us proceed through a simple example. Figure 103 is a filter attenuation requirement with a 40 $^{dB}/_{dec}$ filter attenuation slope line intersecting 0 dB at 27 kHz (The filter topology is the common π-type in Figure 104). If C_y is fixed at 0.01 mF, then it is obvious that the required value of L_{CM} will be 1.71 mH[34]. However, if passive cancellation is utilized then we can safely assume that this attenuation requirement will be reduced by at least 10 dB, which then allows the filter corner frequency to be raised to 47 kHz. Using the same value of C_y, the required choke value is only 0.55 mH. This is a savings of $^2/_3$ just by including a few feet of #30 wire and a ceramic capacitor. Of course if this is a 100 W converter drawing 1-2 A from the line then the size difference in the two chokes will not be very noticeable, but with converters drawing lots of line current then the savings will be very significant indeed.

[34] A full description of this technique of EMI filter design can be seen in Fu-Yuan Shih's paper referenced in the bibliography.

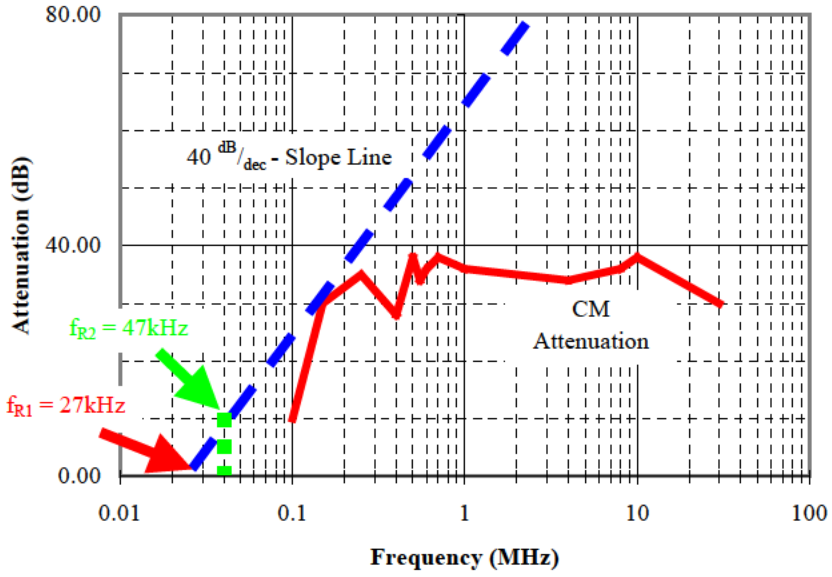

Figure 103: Noise Spectrum Attenuation Example

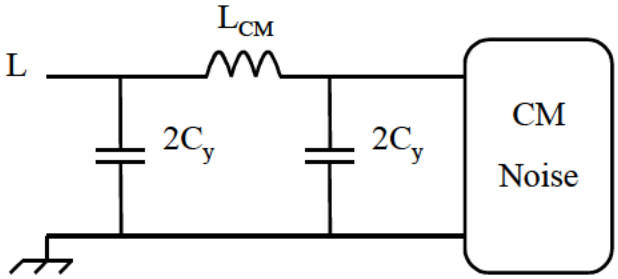

Figure 104: CM Filter for Example

Application of passive CM cancellation to DC/AC and AC/AC converters to date has not yielded the same kind of results that can be obtained with AC/DC and DC/DC converters. The first method of incorporating cancellation windings into the output filter inductor has limitations with regards to the type of load, and of course this technique first requires that the inverter use an output filter—not something that can be always guaranteed. The second method works well in concept, but has run into problems in practice. The Metglas cancellators as constructed had too

much coil resistance to be of usefulness, although this problem can be mitigated with larger cores and larger wire. This technique will therefore not be very useful unless the power requirements of the converter are large enough to justify the large size of the cancellator. The air core cancellators yielded useful results, but putting 10-15 T air cores in close proximity to sensitive gate drives and control circuitry is not something that designers are likely to look favorably upon. Getting good results at low frequencies is also difficult to do with this cancellator due to the requirement for large capacitors. Even so, if the converter only has to meet CISPR or FCC specifications starting above 100 kHz then the cancellator can successfully yield the desired 10—15 dBμV of CM attenuation.

Therefore the conclusion of this thesis is as follows: For converters with DC output passive CM cancellation is something that should be incorporated whenever the input current is more than a few amps. Doing so will yield significant savings in the size, weight, and cost of the EMI filter. For converters with AC output the circumstances where passive CM cancellation can be used successfully are limited at present, but the astute power supply designer should keep the techniques in mind so that the opportunities that present themselves are not wasted.

6.2. Future Research Topics

There is, of course, further work to be done in this area. One major issue is that of implementing the noise cancellation scheme in a production unit. Since my personal research was focused on proving the concept of noise cancellation, I did not address the problems associated with manufacturability other than the need to keep things small and simple. There is certainly a great deal left to be done in this area and I look forward to when I can hear that this work has used by a manufacturer with success.

Another area of improvement lies in the present scheme for inverter noise cancellation. While the cancellator idea has its merits in the area of simplicity and load independence, the big difficulty is the line frequency requirement. At the present time the only small, lightweight solution is to use air core transformers, which have some drawbacks due to the large fringing flux. It is also difficult to extend the benefits of the cancellator to low frequencies for application to MIL-STD-461E requirements. It would be of great benefit to have a better solution that avoids these unpleasantries. One such possible solution would be a mixed active-passive cancellator. This would replace the blocking capacitor with some active devices to keep the cancellator from seeing the low frequency voltage and current and allow small ferrite cores to be used.

The final research suggestion is one that involves the PEBB (Power Electronics Building Block) research program that is ongoing at the Center for Power Electronics Systems at Virginia Tech. This program is motivated by a desire to integrate all the necessary components for power converters into easy to use cells. It would certainly be invaluable to have the above described noise cancellation methods incorporated into those power electronics cells as well.

Bibliography

Busse, Doyle F, Jay M. Erdman, Russel J. Kerkman, David W. Schlegel, and Gary L. Skibinski, "The Effects of PWM Voltage Source Inverters on the Mechanical Performance of Rolling Bearings", *IEEE Trans. Industry Applications*, vol. 33, pp. 567-576, Mar/Apr. 1997.

Costa, F., E. Laboure, F. Forest, S. Lefebvre, "Quantification and Minimization of Conducted Interferences Generated in Hard Switching and Zero Current Switching Cells", *Proc. of APEC*, vol. 2, pp. 615-621, 1994.

Guo, T., D. Y. Chen, and F. C. Lee, "Separation of the Common Mode and Differential Mode Conducted EMI Noise", *IEEE Trans. Power Electronics*, vol. 11, pp. 480-488, May 1996.

Ide, P., F. Schafmeister, and N. Froehleke, "Active Common-Mode Voltage Cancellation for Three-Phase PWM Rectifier/Inverter Systems based on a New Topology", *Proc. of APEC*, vol. 1, pp. 201-207, 2001.

Julian, Alexander L., Giovanna Oriti, and Thomas A. Lipo, "Elimination of Common-Mode Voltage in Three-Phase Sinusoidal Power Converters", *IEEE Trans. Power Electronics*, vol. 14, pp. 982-989, Sep. 1999.

Mardiguian, Martin. *EMI Troubleshooting Techniques*, McGraw Hill, 2000.

"No Clearance for Interference", *CAA News* May/June 2001, CAA New Zealand.

McLyman, William T. *Transformer and Inductor Design Handbook*. Marcel Dekker, Inc. 2nd Ed. 1988.

Ogasawara, Satoshi, and Hirofumi Akagi, "An Active Circuit for Cancellation of Common-Mode Voltage Generated by a PWM Inverter", *IEEE Trans. Power Electronics*, vol. 13, pp. 835-841, Sep. 1998.

Ogasawara, Satoshi, and Hirofumi Akagi, "Modeling and Damping of High-Frequency Leakage Currents in PWM Inverter-Fed AC Motor Drive Systems", *IEEE Trans. on Industry Applications*, vol 32, Sept/Oct 1996.

Ott, H. W. *Noise Reduction Techniques in Electronic Systems*, John Wiley & Sons, Inc. 2nd Ed, 1988.

Rao, Aakash V. K. “The Design and Implementation of a Modified Single Phase Inverter Topology with Active Cancellation of Common Mode Voltage”, M. S. Thesis, University of Wisconsin—Madison, 1998.

Rockhill, A., Thomas A. Lipo, and A. L. Julian, “High Voltage Buck Converter Topology for Common Mode Voltage Reduction”, *Proc. of APEC*, vol. 2, pp. 940-943, February 1998.

Shih, Fu-Yuan, D. Y. Chen, and Y. T. Chen, “A Procedure for Designing EMI Filters for AC Line Applications”, *IEEE Trans. Power Electronics*, vol. 11, pp. 170-181, Jan. 1996.

Xin, Wu, M. H. Pong, Z. Y. Lu, and Z. M. Qian, “Novel Boost PFC with Low Common Mode EMI: Modeling and Design”, *Proc. of APEC*, vol. 1, pp. 178-181, 2000.

Xin, Wu, N. K. Poon, C. M. Lee, and M. H. Pong, “A Study of Common Mode Noise in Switching Power Supply from a Current Balancing Viewpoint”, *Proc. of IEEE 1999 International Conference on Power Electronics and Drive Systems (PEDS’99)*, pp. 621-625, July 1999.

Ye, Zhihong, D. Boroyevich, K. Xing, F. C. Lee, and C. Liu, “Active Common-Mode Filter for Inverter Power Supplies with Unbalanced and Nonlinear Load”, *Proc. of IAS*, vol. 3, pp. 1858-1863, 1999.

Vita

The author was born in Charlottesville, Virginia and grew up in Huntington, West Virginia. He received his B. S. in Electrical Engineering from Cedarville College in 1999. Since the fall of 1999 he has been working toward the completion of his Master's of Science degree at the Bradley Department of Electrical Engineering, Virginia Polytechnic Institute and State University. Since the fall of 2000 he has been employed as a research assistant at the Center for Power Electronics at Virginia Tech where he has continued to investigate passive compensation techniques as well as EMI and power quality issues relating to the design of solid-state frequency converters. Upon completion of his master's degree, he will be taking a position with Northrop-Grumman in Baltimore, Maryland.