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(54) VIDEO DATA COMPRESSION SYSTEM, VIDEO RECORDING/PLAYBACK SYSTEM, AND VIDEO DATA COMPRESSION **ENCODING METHOD**

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(51) Int. Cl.⁷ H04N 7/12

Field of Search 348/402, 409,

348/14.1, 14.08, 159, 385.1, 705, 176

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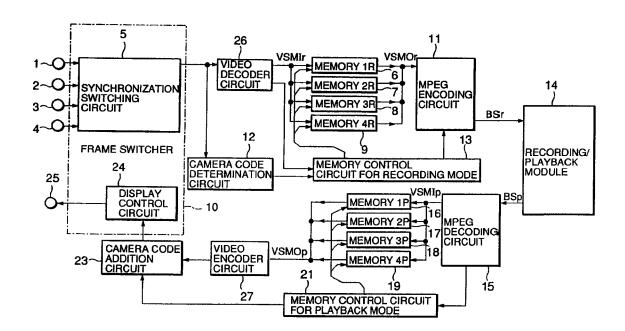
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(57)**ABSTRACT**

A video data compression/playback system efficiently compresses a plurality of video data pieces through inter-frame predictive-encoding. Mixed video data VSMIr composed of time-divided video data received by video input terminals are divided video data pieces each of which corresponding to video input terminals and the video data pieces are written into memories respectively by a memory control circuit for recording mode. The mixed video data written into the memories is read, a specified number of frames at a time. An MPEG encoding circuit performs inter-frame predictiveencoding for each specified number of frames.

13 Claims, 20 Drawing Sheets





^{*} cited by examiner

RECORDING/ PLAYBACK MODULE 14 BSp BSr MPEG 17 DECODING CIRCUIT 5 MEMORY CONTROL CIRCUIT FOR RECORDING MODE MPEG ENCODING CIRCUIT 16 VSMIp, 18 MEMORY CONTROL CIRCUIT FOR PLAYBACK MODE MEMORY 2P MEMORY 1P MEMORY 3P **MEMORY 4P** <u>6</u> 8 MEMORY 3R **MEMORY 4R MEMORY 1R MEMORY 2R** S VSMOp CAMERA CODE DETERMINATION CIRCUIT VIDEO DECODER CIRCUIT VIDEO ENCODER CIRCUIT 27 10 CAMERA CODE ADDITION CIRCUIT SYNCHRONIZATION SWITCHING CIRCUIT FRAME SWITCHER DISPLAY CONTROL CIRCUIT S 23^



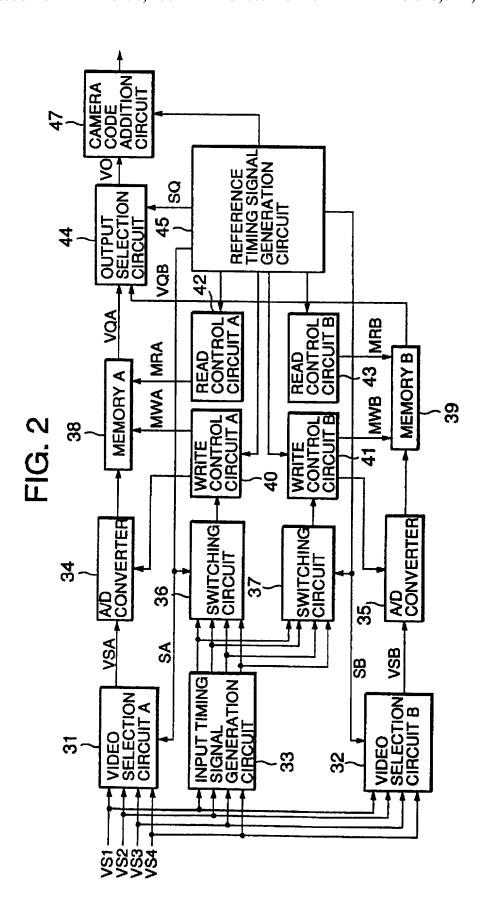




FIG.3

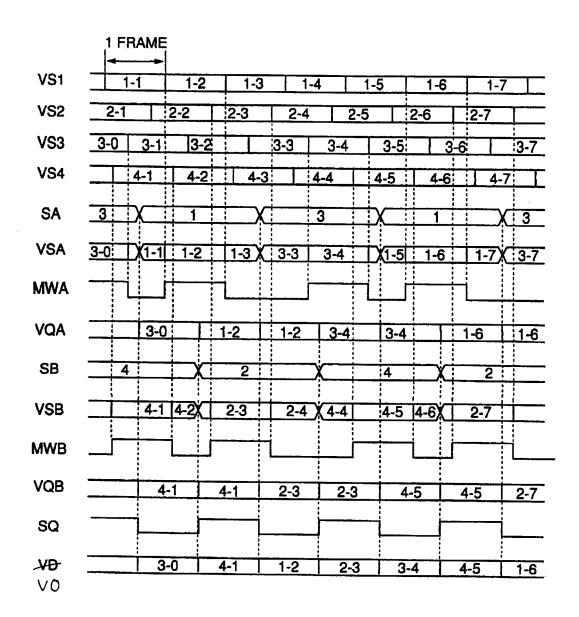




FIG. 4

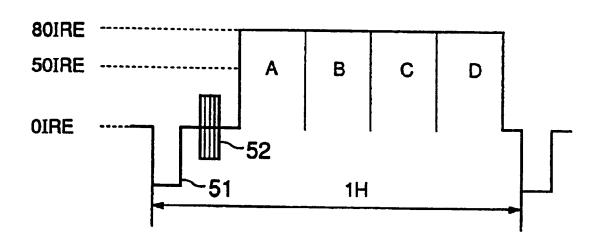
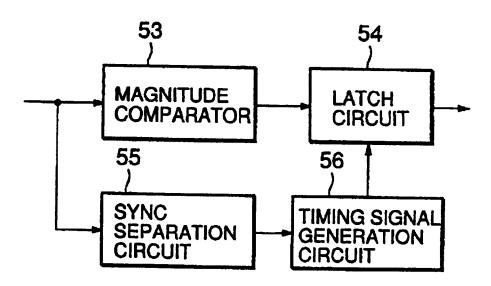


FIG. 5





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