CONSUMER APPLICATIONS OF THE IEEE 1394 SERIAL BUS, AND A 1394/DV VIDEO EDITING SYSTEM

Alan T. Wetzel, Michael R. Schell*

Texas Instruments, Inc., Dallas, Tx.
*Interactive Images, Inc., Colorado Springs, Co.

This paper was prepared for and presented at the International Conference on Consumer Electronics held in Chicago, Ill., June 1996, conference session WPM-6, Intelligent Home Networks.

CONSUMER APPLICATIONS OF THE IEEE 1394 SERIAL BUS, AND A 1394/DV VIDEO EDITING SYSTEM

Alan T. Wetzel, Michael R. Schell*

Texas Instruments, Inc., Dallas, Tx.
*Interactive Images, Inc., Colorado Springs, Co.

ABSTRACT

The IEEE 1394-1995 High Performance Serial Bus [1] has been created with consumer use in mind. Some of the more important features of the base standard are reviewed. Enhancements and additions to the standard to support new consumer applications, such as MPEG-2 transport and the new Digital Video (DV) tape format, are described. Consumer DV products incorporating 1394 are now on the market, more have been announced, and related developments portend even more in the future. The HD-DVC "DV" [2] system has features which have significant advantages for video editing systems. The 1394 interface used by DV equipment brings many benefits to a video editing system. A PC based nonlinear video editing system is described, which takes advantage of the combination of DV and 1394 features in a high performance, low cost implementation.

WHY CONSUMERS WILL BE WINNERS WITH 1394

Superior digital quality and performance at low cost

The most obvious benefit seen by consumers in the shift to digital technologies is the improvement in quality. This has been true for some time with audio CDs, as well as the newer DBS systems. This is now becoming true again with the new HD-DVC "DV" (digital video) tape systems. The digital recording and playback, combined with the digital 1394 interface, completely eliminates the noise pick-up and signal losses that occur in analog systems and interconnects. The digital record/playback avoids the audio flutter and video picture jitter that is common in present analog systems. The 1394/DV combination also provides for virtually lossless audio/video editing and dubbing. This recognition of the superior quality of the all-digital systems has resulted in an unprecedented demand for products.

The 1394 serial bus interface is designed to support these digital devices, both from the user experience and feature/cost points of view. The 1394 interface has been completely implemented in generic digital ASIC CMOS silicon processes. Multiple integration possibilities exist, from today's first generation, multi-chip architectures, to single-chips, to full integration (zero additional chips) into other ASIC chips. Full ASIC integration is a key benefit to reducing circuit board space requirements in space critical applications. As the silicon processes evolve to smaller feature sizes, the area required to implement the 1394 logic will also decrease.

Hassle-free hook-up

The first, and perhaps only, 1394 item that a consumer is likely to encounter is the plug and cable. A user-friendly connector and cabling system is fundamental to 1394. The cable assemblies feature small and durable connectors. The plugs and sockets are designed for ease of use. The shape of the connector nose and socket opening provide unambiguous tactile feedback, which facilitates frustration-free blind insertion. A very flexible cable, less than ¼ inch in diameter, is standard. This system has been evolved from the child-proof connectors used by the Ninetendo Game Boy.

The second thing that a consumer is likely to notice about the 1394 interconnect system is the freedom from connection constraints. Because 1394 is a bus, with all devices sharing the same transmission domain, it is irrelevant as to which way the different pieces of equipment are connected together. Because all the digital signals for a particular piece of equipment can be carried on the same 1394 cable, only one connection is required for any unit. There is no in-out or up-down direction sense in 1394, so the connectors at each end of the cable will generally be the same. And it makes no difference which socket is used on a particular device, since they are all equivalent.

One of the many things the consumer will probably not notice is the automatic configuration and management that is built in to 1394. The user does not have to set any configuration switches because the node IDs are assigned automatically during 1394 bus initialization. And no special device needs to be provided or designated as a central controller or bus manager.

CONSUMER ORIENTED FEATURES OF THE IEEE 1394 SYSTEM

The 1394 connector and cabling system

Two connector and cable systems are presently defined. The original 6-pin/6-conductor style contains two shielded twisted pairs for data, plus another pair for optional power and ground. The 6-pin system uses a detent or optional latching retention system. A newer and smaller 4-pin/4-conductor system was developed for use on digital camcorders and other size sensitive applications. It has the two twisted pairs for data signaling, but eliminates the optional power and ground pair. Both cables have overall shielding. The connectors for the two cable systems are shown in Fig 1.

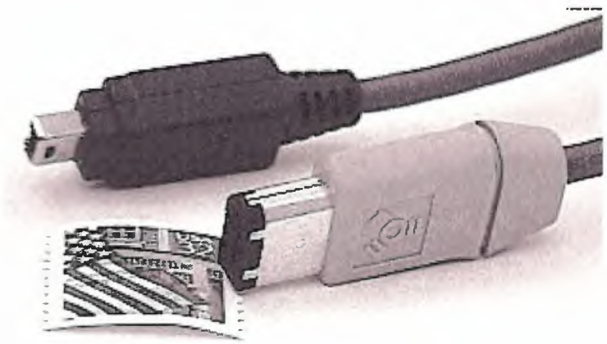

Fig 1: The 1394 connectors

Unconstrained interconnect

The topology of a 1394 bus may be a simple daisy-chain, a tree, a star, or a combination of these. The 1394 standard indicates that the most widely separated devices should have no more than 16 cable hops between them, but in reality the generous margins designed in to the 1394 system ensures that nothing breaks even if this limit is exceeded.

Automatic configuration

During initialization, each device on the 1394 bus takes a turn to announce its configuration and capabilities, and acquires a unique node ID. This process of bus enumeration and device ID assignments is handled completely automatically, and provides support for Plug-and-Play compatibility.

All 1394 devices have the capability of being the root, which is a simple function to resolve bus arbitration requests and grants. This means that no special device must be included to initialize or manage the operation of any 1394 bus. This is a significant difference from some other busses which require a central processor running dedicated real-time processes for management and control. In a similar fashion, any isochronous-capable consumer device is able to function as the cycle master, which regulates the isochronous cycles.

The distributed intelligence that handles the initial configuration and root arbitration functions is contained entirely within the 1394 physical layer. This allows a device to be an active member of a bus even if its higher layer (link and above) functions are not active. By eliminating the need for higher layer activity the process is much faster, and power saving strategies can be realized. The implementation of these physical layer functions is purposefully simple enough to allow it to be built as a small state machine. Hardware implementation also contributes to the speed of configuration. Because most of the 1394 functionality is implemented in silicon, the cost for 1394 will continue to drop as die size scales down with smaller process sizes.

Isochronous "real-time" channels

Besides scaling the 1394 implementation costs with each successive generation of silicon processes, the 1394 system provides a special feature to minimize the system complexity and costs. This feature is isochronous data transport.

The 1394 Serial Bus provides two distinct modes of operation, asynchronous and isochronous. The bus alternates between these two modes of operation, with isochronous operation taking precedence over asynchronous communication. Isochronous operation occurs at a cycle rate of 8,000 times per second. Under normal circumstances the isochronous operation may take up to 80% (100 µsec) of the available cycle time, reserving at least 20% for asynchronous traffic. The asynchronous data delivery and verification is assured by an acknowledge and retry protocol, and is normally used for control, status, and accuracy-critical data.

Isochronous data delivery is a "just in time" type of service. Data is broadcast on assigned channels with guaranteed bandwidth or time allocations. Delivery of preallocated real time data packets, at a uniform rate, is built into the 1394 protocol.

Up to 64 isochronous channels may be allocated on the 1394 Serial Bus. All allocated channels can send their data during each isochronous cycle. Only one device may transmit data on a given channel, but any number of devices may listen to a particular channel.

A major advantage of isochronous transport is that a much smaller FIFO is required for buffering the video and audio data before and after transmission across the 1394 bus. Because the bandwidth and latency are guaranteed, the 1394 interface silicon can use a minimally-sized FIFO memory, which reduces the die size and the ultimate product cost to the consumer. Non-isochronous transport systems require significantly larger FIFO memories to accommodate the wide swings in data-rates or transport delays.

ENHANCEMENTS AND EXTENSIONS TO IEEE 1394

MPEG-2 transport

The MPEG-2 System standard, ISO/IEC 13818-1, Part 1 [3] assumes that the transmission system for transporting packets has a constant delay characteristic. The maximum deviation or jitter allowed is 500 nanoseconds. This limit is a significant challenge to any shared access system, including 1394.

Two primary factors may contribute to variations in delivery delay of 1394 isochronous packets: 1) Delays in starting an isochronous cycle, and, 2) Changes in the order in which channels (packets) are transmitted. Cycle start delays can be caused by an asynchronous transaction being active at the time when cycle start should occur. With a maximum sized asynchronous packet this delay can be approximately 75 microseconds. The ordering of isochronous channels in any particular cycle is unlikely to change unless there is a change in bus configuration, or in bus utilization. The worst case would be for a channel's packet to move between the beginning and end of the 100 microsecond transmission window of the isochronous cycle.

In order to meet this MPEG-2 jitter requirement, a technique was developed that allows cancellation of almost all of the 1394 induced packet delivery jitter. This technique takes advantage of the fact that all nodes participating in isochronous traffic share a common time reference. The cycle start packets that signal the beginning of an isochronous cycle also include the current value of the master clock. This clock is based on the basic 1394 reference frequency of 24.576 MHz.

When an MPEG-2 transport packet is received by a 1394 device, the current 1394 system time value is prefixed to the transport packet. This time stamp is one quadlet, or four bytes of data. At the receiving end of the 1394 transport system, the 1394 time stamp is removed, and is compared to the current system time. By passing the transport packets to the destination device at a constant offset from system time, the original temporal relationship between the packets will be restored. This eliminates 1394 transport jitter to the resolution of two 1394 clock periods, or 2 x 1/(24.576 x 10^6) = 81.41 nanoseconds.

A proposed addition to the MPEG2 standards, Extensions for real time interfaces for system decoders [4] has clarified transport stream jitter measurements and suggested a more generous limit. The new transport jitter limit is 25 microseconds, measured peak-to-average (or 50 μsec peak-peak). The 1394 time stamping system provides jitter cancellation capabilities that account for less than 1/6 of 1% of this proposed limit, so 1394-induced jitter effectively can be ignored.

The CIP header system

As part of the development of the 1394 time stamping and jitter canceling functions, a standardized formatting of the data was developed. This has been named the Common Isochronous Packet, or CIP, header. The CIP header is an extensible format that can be adapted for future applications as they arise. Today there are sets defined for the SD, HD and SDL formats of the DV tape systems, along with MPEG-2 transport packets as used by the DVB and ATV digital television systems. These formats are defined in the HD DVC "Blue Book."

In addition to the previously described time stamping function, the CIP header system also supports a number of other system functions. The two most notable of these are the Plug Control Register, or PCR, and the Function Control Protocol, or FCP. The specifications for both of these, together with the associated Connection Management Protocol (CMP), also are covered in the HD-DVC "Blue Book."

The purpose of PCR/CMP is to provide a method for controlling the virtual connection between transmitting and receiving devices on a 1394 bus. Two primary functions are: 1) To prevent active connections from being accidentally broken, and 2) To permit broadcasting devices with no listeners to be turned off. In the first case, a listener can register with the sender, and the sender knows not to stop as long as the connection is

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.

WHAT WILL YOU BUILD? | **sales@docketalarm.com** | **1-866-77-FASTCASE**

fastcase®
Smarter legal research.