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Helms

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(54) **SYSTEM AND METHOD FOR SELECTING BETWEEN A VOLTAGE SPECIFIED BY A PROCESSOR AND AN ALTERNATE VOLTAGE TO BE SUPPLIED TO THE PROCESSOR**

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(52) **U.S. Cl.** **713/300**
(58) **Field of Search** 713/300, 320, 713/340

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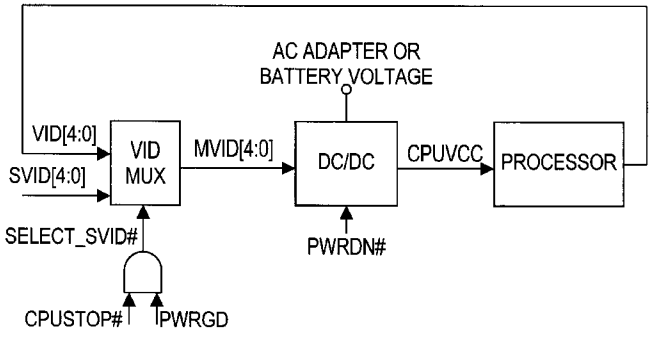
(57) **ABSTRACT**

Disclosed herein are a method and apparatus to provide a deterministic power-on voltage in a system having a processor-controlled voltage level. In one embodiment, the system includes a DC/DC converter, a processor, and a selection circuit. The DC/DC converter receives a voltage setting signal or signals from the selection circuit and provides an adjustable power output signal having a voltage indicated by the voltage setting signal. The processor is powered by the adjustable power output signal. When powered, the processor provides a programmable voltage setting signal or signals. The selection circuit receives the programmable voltage setting signal or signals, a hardwired voltage setting signal, and a selection signal or signals, and when the selection signal is in a predetermined condition, the selection circuit provides the programmable voltage setting signal or signals from the processor to the DC/DC converter. Preferably, when the selection signal is in a second predetermined condition complementary to the first predetermined condition, the circuit provides the hardwired voltage setting signal to the DC/DC converter. The first and second predetermined conditions of the selection signal are preferably de-assertion and assertion, respectively. The selection signal may be determined by a logic gate that combines a mode control signal and a power good signal, and causes the selection signal to select the voltage setting signal from the processor only when the power good signal is asserted and the mode control signal is de-asserted. This advantageously allows for the processor to dictate its operating voltage level, an ability that is extremely useful for power and thermal management in notebook PCs.

17 Claims, 2 Drawing Sheets



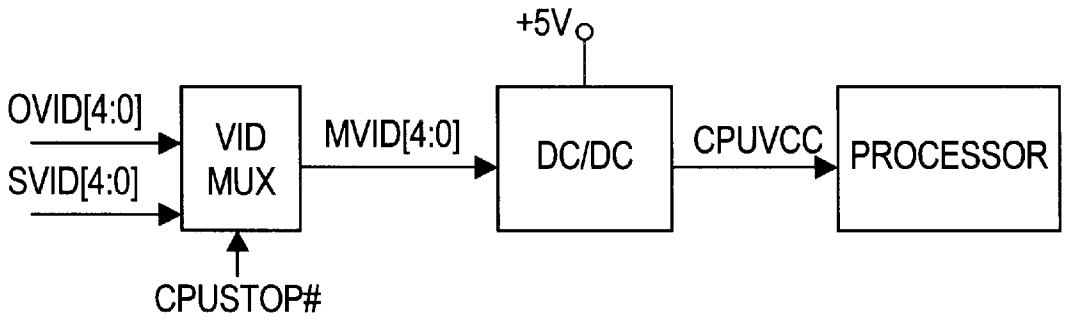


FIG. 1

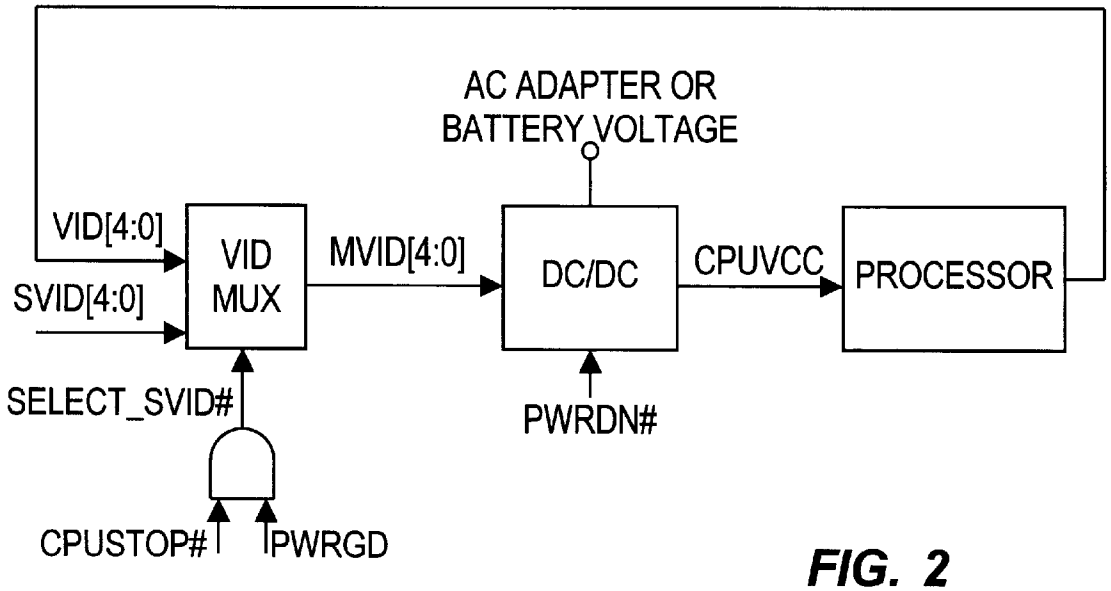


FIG. 2

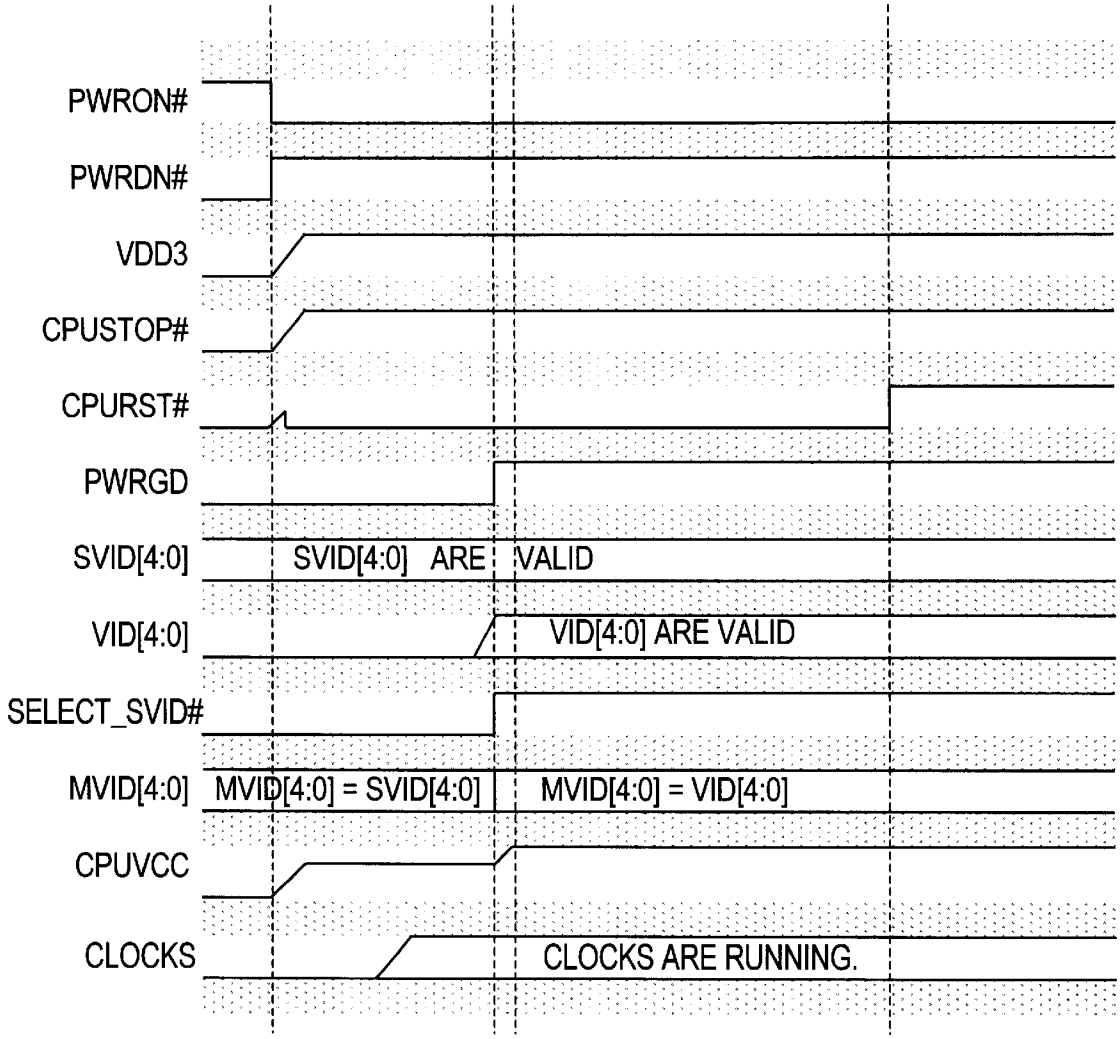


FIG. 3

SYSTEM AND METHOD FOR SELECTING BETWEEN A VOLTAGE SPECIFIED BY A PROCESSOR AND AN ALTERNATE VOLTAGE TO BE SUPPLIED TO THE PROCESSOR

BACKGROUND OF THE INVENTION

The present invention generally relates to a method for setting an initial power supply voltage in a system having a programmable power supply voltage.

It has recently been regarded as desirable to dynamically adjust the power supply voltage and clock frequency of computer system processors to minimize power consumption and regulate heating of the processor core. The computer system processors themselves would seem to be an ideal mechanism for controlling these adjustments but for the fact that they must first receive the power and clock before they can determine the appropriate settings.

Until the processor is supplied with a minimum power-up voltage, it is not capable of driving the voltage identification outputs to control its operating voltage. Therefore it is necessary for the system hardware to ensure the processor is supplied with the required power-up voltage and to prevent the DC/DC converter from responding to the processor's voltage identification outputs until the processor is driving them to select the startup voltage. To avoid damaging the processor, it is necessary to ensure that as the system is powered on, indeterminate signals from the processor do not cause the power supply voltage level to exceed the processors maximum operating limits.

SUMMARY OF THE INVENTION

The above issues are solved by a method and apparatus to provide a deterministic power-on voltage in a system having a processor-controlled voltage level. In one embodiment, the system includes a DC/DC power converter, a processor, and a selection circuit. The DC/DC converter receives a voltage setting signal from the selection circuit and provides an adjustable power output signal having a voltage indicated by the voltage setting signal. The processor is powered by the adjustable power output signal. When powered, the processor provides a programmable voltage setting signal. The selection circuit receives the programmable voltage setting signal, a hardwired voltage setting signal, and a selection signal, and when the selection signal is in a predetermined condition, the selection circuit provides the programmable voltage setting signal from the processor to the DC/DC converter. Preferably, when the selection signal is in a second predetermined condition complementary to the first predetermined condition, the circuit provides the hardwired voltage setting signal to the DC/DC converter. The first and second predetermined conditions of the selection signal are preferably de-assertion and assertion, respectively. The selection signal may be determined by a logic gate that combines a mode control signal and a power good signal, and causes the selection signal to select the voltage setting signal from the processor only when the power good signal is asserted and the mode control signal is de-asserted. This advantageously allows for the processor to dictate its operating voltage level, an ability that is extremely useful for power and thermal management in notebook PCs.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description of the preferred embodiment is considered in conjunction with the following drawings, in which:

FIG. **1** is a functional block diagram of a system having hardwired voltage settings;

FIG. **2** is a functional block diagram of a system having processor-controlled voltage settings; and

FIG. **3** is a timing diagram showing the operation of the deterministic power-on method.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

Certain terms used throughout this disclosure are hereby defined. The term "signal" is intended to refer to a value conveyed via electrical impulses or electromagnetic waves on one or more conductive wires or other suitable transport media. Hence the word signal may be used to refer to a binary value conveyed by transmitting the representative bit values in parallel across multiple conductors. It may also be used to refer to an analog value conveyed by a proportional voltage on a single wire. It is to be understood that there are many ways to convey a value between components, and the use of the singular term "signal" in a claim does not limit the scope of the claim. The terms "asserted" and "de-asserted" are intended to refer to complementary conditions of a two-state signal. They are not necessarily respectively limited to digital logic "high" and "low" voltages. It is to be understood that the system designer can individually decide for each signal which digital logic states will represent the assertion and de-assertion of that signal. Such design considerations do not limit the scope of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Turning now to the figures, FIG. **1** shows a processor receiving a power supply voltage signal (CPUVCC) from a programmable voltage converter (DC/DC). The converter receives power (in this case +5V) and a voltage setting signal (MVID), and provides a regulated output voltage at the level indicated by the voltage setting signal. Because it is desirable to provide the system with a power-saving mode in addition to the normal operating mode, the voltage setting signal has two possible values: SVID for "sleep" mode and OVID for "operating" mode. A multiplexer (VID MUX) selects between these two voltage settings in response to a mode control signal (CPUSTOP#) which may be provided from the south bridge. In this embodiment, the OVID and SVID are hardwired, i.e. set by resistors, fuses, jumpers, or some other non-volatile mechanical means.

It is noted that computer systems typically have multiple buses with devices called "bridges" that allow communications between components on different buses. It is also noted that computer systems typically have support circuitry that perform administrative functions such as interrupt management (the interrupt controller), clock/calendar/timer functions (the clock), configuration management, power supply control, and power-on signal sequencing. This support circuitry has commonly been placed in the bridge from the PCI bus to the peripherals and lower bandwidth busses, i.e. the "south bridge".

Consequently, one of skill in the art will recognize that the south bridge may be configured to monitor the activity level of the computer system, and to place the computer system into a "sleep" mode if it is determined that the computer system has been inactive for a predetermined length of time. In the embodiment of FIG. **1**, the assertion of the mode control signal causes the power supply voltage to be lowered to the hardwired sleep setting. In systems having APM (Advanced Power Mangaement), if the south bridge later detects activity, (e.g. a key press or motion of a pointing device), the south bridge can deassert the mode control signal to raise the power supply voltage to the hardwired "operating" setting. In systems having ACPI, the operating system decides when to place the system into a sleep state, and calls device drivers to place the devices into a low power state and then manipulates a register in the south bridge to initiate the hardware sequence into the sleep state.

One example of a programmable voltage converter is a MAXIM MAX1711 High-Speed, Digitally Adjusted Step-Down Controller or its equivalent. The MAX1711 can transition between selected voltages in less than 100 us. The MAX1711 uses its D4 through D0 inputs to determine the output voltage level as follows:

D4:D0	Output Voltage
00000	2.00
00001	1.95
00010	1.90
00011	1.85
00100	1.80
00101	1.75
00110	1.70
00111	1.65
01000	1.60
01001	1.55
01010	1.50
01011	1.45
01100	1.40
01101	1.35
01110	1.30
01111	Shutdown
10000	1.275
10001	1.250
10010	1.225
10011	1.200
10100	1.175
10101	1.150
10110	1.125
10111	1.100
11000	1.075
11001	1.050
11010	1.025
11011	1.000
11100	0.975
11101	0.950
11110	0.925
11111	Shutdown

See the MAXIM Data sheet for more information on Shutdown.

It is desirable to provide processors such as upcoming versions of AMD's K6-III and Athlon processors with voltage identification (VID) output signals that they will drive to the DC/DC converter that supplies their operating voltage. These, in addition to adjustable core frequencies, will allow for maximum Notebook PC performance in any thermal environment, and will also allow the user to determine the tradeoff between performance and battery life.

The processors will preferably be provided with a register that contains the current voltage setting. When the processor is reset, the voltage setting is initialized to some "safe" voltage such as, e.g. 1.5 V, and during the assertion of the reset signal, the setting signals are driven to the processor output pins. When desired, the voltage setting signals are changed by writing to this register.

When the system would be first powered on, the processor would not be powered, and would therefore not be capable of driving its VID outputs until its voltage becomes stable at an operational level and its clock is running. Also, as power is applied to the processor, the state to which it would drive its VID outputs could not be guaranteed until the voltage is within its specified limits, reset is asserted, and the clock to the processor is running and stable. Additionally, some processors require a power good signal to be asserted to the processor before the processor drives its startup VID. However since outputs of the processor are used to dictate to the DC/DC converter what voltage level should be driven to the processor, it cannot be known what voltage will be driven to the processor when the system is first powered on. The possibility exists that the DC/DC converter could drive a voltage so low that the processor would not be able to operate enough to drive its VID outputs to select the intended power up voltage. If this scenario occurred the system would he "hung" in a state that it could not exit from. Another possibility is that the DC/DC could drive a voltage level that is higher than the maximum allowed voltage for the processor. Either of these scenarios could damage the CPU after some period of time.

FIG. **2** shows a configuration that solves this problem by ensuring that the processor is always supplied with a voltage at which it will be operational when the system is powered on. In this embodiment, the sleep voltage setting signals SVID are still hardwired, but the operating voltage setting signals are provided by the processor. A selection signal (SELECT_SVID#) is provided to the multiplexer to select the appropriate multiplexer input. A logic circuit is used to produce this selection signal. When the selection signal is asserted, the multiplexer selects the hardwired voltage setting signals, whereas when the selection signal is de-asserted, the multiplexer selects the voltage setting signals from the processor.

The logic circuit is preferably designed to assert the selection signal during the initial power-up sequence and whenever the computer system goes into the sleep mode. Accordingly, the logic circuit operates on the mode control signal (CPUSTOP#) and the power-good signal (PWRGD). Only if the mode control signal is asserted to indicate sleep mode or if the power-good signal is de-asserted does the logic circuit assert the selection signal. Otherwise the selection signal is de-asserted.

Persons of skill in the art are familiar with the power-good signal. When power is initially applied to a computer system, this signal is held in a de-asserted state until all of the voltage rails in the system are stable within specified limits. At that time, the power-good signal is asserted and maintained until the system is powered down. The PWRGD signal of FIG. **2** is deasserted so that SVID[4:0] drives the DC/DC until CPUVCC is at a level where the processor can deterministically drive the VID signals. It will be the responsibility of the BIOS or system software to set the VID signals early in the POST routine to transition the processor core voltage to the desired performance level.

As a quick aside, it is noted that the DC/DC converter of FIG. **2** may receive a power down (PWRDN#) signal. PWRDN# is a control input that when asserted causes the DC/DC to shut off its outputs, and enter a low power state.

FIG. **3** illustrates the operation of the deterministic power-on circuit by showing a sequence of signal transitions after

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