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Multi-Standard DSP based wireless system

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Abstract

Rapid growth in the wireless communication has pushed semiconductor manufacture to seek low cost, highly integrated and multi-standard design for a wireless handset due to marketing situation - existing different air interface of wireless system.

The paper will focus on the description of:

- Different kind of the multi-standards DSP based transceiver architecture include mixing analog function;
- Advantage and technical overview among different kind of the multi-standard transceiver.
- Describe new architecture: single conversion band pass sampling DSP based multi-standard receiver.

The paper also state different kind of standard and focus the main interesting topic in a high level design example of new receiver architecture for this multi-standard specification such as GSM, DCS1800, DECT, PHS, FHSS-DCT, and FHSS-WLAN.

Introduction

Digital radio personal communication most utilizing the band between 800MHz to 2.5GHz will play important role in overall communication infrastructure in next decade. For a multi-standards TDMA handset specification as shown in table 2, we know that tasks processing and resource allocation by commonalties will list as follows:

Table 1.0 Multi-standard wireless system

LAYER	ITEM	GSM FHSS-DCT DCS1800 PHS DECT FHSS-LAN
1	Rx I Q receiver	● Multi-band digital tuning LNA,Mixer, plus AGC IF I,Q demodulator in BiCMOS ● Wideband LNA, Mixer plus AGC IF I,Q demodulator
	Frequency select	VCO+PLL for different spec. and band can use : ● Ring OSC, clock PLL in CMOS as reference paper 1, ● BiCMOS or CMOS multi-band VCO plus PLL
	Tx power	PA for different standards is most difficult, we can choose technical approach : ● Multiple PA module in GaAS, HBT, MOSFET, BJT (Bulky) ● Several, multi-band PA in GaAS, HBT, MOSFET, BJT ● Single Multi-band PA in GaAS, HBT

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	Duplexing	● Several DR filter (Bulky and high cost) ● Wideband band tunable filter (Difficult) ● Multiple middle and wideband selectable filter by LTCC combined with IR mixer in receiver and spurious performance tuning in transmitter
	Power control	● Ramp & power class control by Mixing analog H/W and no problem to migrate different spec. Most important is programmable clock and Ramp generator.
	Multiple Access	● Programmable frame based and clock generator in digital H/W
	Bandwidth	● Hardware DSP for IF channel selection plus IF under sampling can support different bandwidth channel selection spec.
	Modulation	● Hardware DSP for modulation of GMSK, G2FSK, G4FSK, p/4DQPSK
	Vocoder	● G.726, RPE_LTP(Full Rate,Half Rate,Enhance Full Rate) easily include DSP S/W
	Frame,ch. rate	● Programmable frame based logic and clock generator in digital H/W
	Channel coding	● DSP SW
	Encryption	● DSP SW
	Ch. Structure	● Programmable frame based and clock generator in H/W and MCU layer 1 S/W
	AFC,ATC,Sync.	● DSP SW and MCU S/W
	AGC	● DSP SW and MCU S/W
	Layer 1 or MAC	● MCU S/W
2	Data link	● MCU S/W
3	Call control	● MCU*
	Radio resource*	● MCU*
	Mobility	● MCU*
	Short message	● MCU*
	Supplementary	● MCU*
-	MMI	● MCU

From the TDMA commonality of the multi-standards as table 2, which only one different is CSMA in frequency hopping wireless LAN; we know the most difficulty for this multi-standards specification is the programmable transceiver; as the table 2 states, the transceiver can design as DSP portion after IF signal processing, this characteristic is obvious in receiver signal processing.

Table 2.0 Multi-standard wireless system

	GSM	DCS1800	DECT	PHS	FHSS-WLAN	FHSS-DCT
Frequency:Mhz	T 890-915, R 935-965	T 1710-1785, R 1805-1880	1880-1900	1895-1907	2400-2483.5	902-928
Bandwidth (kHz)	200	200	1728	300	1000	open
Modulation	GMSK, BT=0.3	GMSK, BT=0.3	GMSK, BT=0.5	π/4 QPSK	G2FSK,G4FSK	G2FSK,G4FSK
# of Carriers	124	374	10	40	79	open
Peak Tx power	0.8W,2W,5W,8W	0.25W,1W	250mW	10mW	1W MAX (USA)	1W MAX
Multiple Access	FDMA/TDMA	FDMA/TDMA	TDMA/FDMA	TDMA/FDMA	CSMA	TDMA/FDMA
Duplexing	FDD	FDD	TDD	TDD	TDD	TDD/FDD
# of Slot per carrier	8	8	12:1	4:1	-	open
Vocoder	RPE_LTP	RPE_LTP	ADPCM G726	ADPCM G721	-	ADPCM G726
Bit Rate	13Kbps	13Kbps	32Kbit/sec	32Kbit/sec	-	32Kbit/sec
Power control	MS,BTS	MS,BTS	-	MS	-	open
Channel Rate	270.833 Kbps	270.833 Kbps	1152Kbps	384Kbps	1Mbps,2Mbps	open
Frame	4.615mSec	4.615mSec	10mSec		-	open
Standard Doc.	ETS	ETS	ETS 300 175	RCR Std-28	IEE802.11	open
*Sensitivity	-108dBm	-108dBm	-96dBm	-104dBm	-96dBm	-105dBm

Note: Sensitivity is an engineering specification to meet type approval.

Transceiver architecture

To seek low cost, highly integrated and multi-standard design for a wireless system, especially in handset or portable terminal will drive the system architecture as below into:

- **Classic Transceiver plus DSP/MCU.**

This architecture shown in Figure 1 is not easily to meet multi-standard Air interface, even programmable DSP capable to process different physical layer 1 protocol such as demodulation, modulation, channel coding and so on, but main problem is coming from transceiver can't be programmable, this make this architecture need different kind subsystem for multi-standards, this make all seems impossible and cost expensive.

- **Transceiver with single conversion band pass sampling wideband receiver plus DSP/MCU**

Single conversion receiver with IF band pass sampling, I-Q digital mixer, AFC, AGC, and NCO logic is quite important at current stage due to difficulty of high resolution and higher frequency ADC with low distortion. This architecture as shown in Figure 2 can process different air interface, filter BPF-IF1 can receive several Rx channel and do final channel selection at ASIC DSP portion, this will make filter BPF-IF1 can use middle Q type such as middle Q LTCC filter instead of higher Q SAW's and lower Q type of VCO at receiver side if we choose proper sampling frequency; it actually means the cost down and easily production of RF module. This architecture has several characteristics as below :

1. Duplexing still need several type duplexer.
2. It can use several middle bandwidth selection LNA + Double balance mixer for receiver front end.
3. IF filtering can use high Q SAW filter or middle Q LTCC filter.
4. AGC budget need several stages among LNA, IF AMP, Digital Attenuator before ADC.
5. Channel selection filter must process by IF processing DSP or ASIC DSP.
6. PA in transmitter still need several module

- **Transceiver with direct conversion baseband sampling receiver plus DSP/MCU**

Direct conversion receiver with baseband sampling, I-Q filtering, AFC, AGC, and NCO logic. This architecture shown in Figure 3 can process different Air interface, filter LPF can receive several Rx channel and do final channel selection at ASIC DSP portion, this will make filter LPF can use low Q type switching capacitor filter instead of higher Q SAW's; main disadvantage of the architecture is this need to cancel DC-offset and deal with spurious leakage problem. Most difficult of DC-offset canceling is different physical layer standard with different DC-offset canceling tracking filter, it is information dependent. This architecture has several characteristics as below :

1. Duplexing still need several type duplexer.
2. It can use several middle bandwidth selection LNA + Image rejection (IR) mixer for receiver front end. Several band IR mixer is quite difficult due to quadrature phase shifter, so that it need digital phase shift tuner
3. AGC budget is same situation as band pass sampling single conversion architecture.
4. PA in transmitter still need several module, if we combine DDS based modulator as shown in Figure 5, we can build Image rejection mixer for up converter.
5. VCO and its spurious leakage are difficult to pass specification of multi-standards.
6. DC-offset is also quite difficult as stated above.
7. Major advantage of the architecture is IF filtering and channel selection, this can process with low Mips programmable ASIC DSP filter or switching capacitor filter.

- **Transceiver with direct sampling wideband receiver plus DSP/MCU**

Direct sampling wideband receiver is an architecture without any RF mixer in RF front end; most of direct sampling receiver use under sampling approach. This architecture can process different air interface, filter BPF can receive full of Rx channel and do final channel selection at ASIC DSP portion, this will make filter BPF must have several band middle Q type LTCC, DR or SAW filter; Due to higher gain AGC LNA is difficult to integrate in one RF integrated chip, so it need higher dynamic range and most precise ADC

for receiver signal. Higher precision and high frequency ADC is difficult subject for under sampling architecture; for example, How can a GSM/DCS1800 dual band receiver using a 41MHz under sampling rate ADC operate precisely in 1800MHz, it is quite obvious this need a higher sampling rate Sigma-Delta ADC for precision consideration, it can convert low bits - higher sampling rate signal data to higher bits-middle rate sampling data, so that high precision characteristic can keep; but it still have a lot challenges like the jitter of sampling clock, low power consumption, longer taps of programmable channel filter and so on. This architecture has several characteristic as below :

1. Duplexing still need several type duplexer.
2. It can use several middle bandwidth selection LNA + double balance mixer for receiver front end.
3. AGC budget is become critical comparing with band pass sampling single conversion architecture due to 45 maximum AGC range in LNA.
4. PA in transmitter still needs several module.
5. Only one transmitter band switching VCO need.
6. No DC-offset problem.
7. Higher ADC sampling rate and input range need.
8. Higher resolution and dynamic range of ADC need.
9. Higher IP3 LNA need due to higher gain at this stage.

- **Transceiver with direct sampling wideband receiver, DDS based modulator plus DSP/MCU**

Direct sampling wideband receiver have great advantage as description above, but it is still need a VCO to meet different Air interface specification among standards, so DDS based modulator can overcome the problem but consume higher power than original one, the DDS based architecture makes transmitter frequency selection in ASIC DSP portion and only a narrow band switchable VCO needed in RF up-converter, so that different standard can use same type of band switchable VCO. Due to low power DDS operating frequency up to 180MHz consume only 50mW at 1V CMOS process, DDS based modulator will be trend for multi-standards wireless handset. Even, the high performance modulator can produce; it also have many challenges in the jitter of DAC clock, low power consumption, higher SFDR, higher order low distortion switching capacitor filter and so on.

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