# Low-Power Implementation of a Fifth-Order Comb Decimation Filter for Multi-Standard Transceiver Applications

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## ABSTRACT

In multi-standard transceivers a programmable decimation filter is required to perform channel select filtering at baseband since the channel bandwidths, sampling rates, and CNR requirements are different. This paper presents a low power fifth-order comb decimation filter with programmable decimation ratios (16 and 8) and sampling rates (12.8 MHz and 44.8 MHz) for GSM and DECT applications. The non-recursive architecture for comb filter is employed and low power VLSI implementation techniques are developed.

## INTRODUCTION

Recent research on radio frequency (RF) communication transceivers focuses on both higher integration and multi-standard operation. Higher integration can be obtained by optimizing receiver architectures to eliminate the off-chip components. The receiver architectures that performs channel select filtering on chip at baseband are preferred since digital signal processing techniques can be easily applied to adapt to multiple communication standards. Fig. 1 shows the wide-band intermediate frequency with double conversion (WIF) architecture [1] which can be used to implement a multi-standard (DECT and GSM) receiver. The WIF architecture needs a high dynamic range oversampling sigma-delta (SD) analog-to-digital (A/D) converter that can adapt to the different requirements from the multi-standards. The dynamic range of a SD A/D converter can be easily adjusted by selecting different oversampling ratios. Therefore a decimation filter with programmable decimation ratios is needed in the A/D converter.

While the sampling rate and resolution of oversampling SD A/D converters are typically determined by their analog modulators, the power consumption is governed largely by the digital decimation filters [2]. It is possible to attenuate the quantization noise and undesired channels with a single filter and then decimate to the Nyquist rate, but this approach consumes much power. By decimating in multiple stages, the complexity of the filters is reduced, and subsequent filters operate at lower sampling rates, further reducing the power consumption [3]. In multi-stage decimation filters it has been shown in [4] that the comb filter is an efficient way to decimate the output of the analog modulator to four times the Nyquist rate. Fig. 2 shows a multi-stage decimation filter suitable for GSM and DECT applications. To meet the system requirements, a fifth-order comb decimation filter (6-bit input) with programmable decimation ratios 16(GSM) / 8(DECT), and sampling rates 12.8 MHz(GSM) / 44.8 MHz(DECT) is needed. Since the comb filter operates at the high sampling rate its power consumption is large. Hence low power implementation of the comb filter is very important.

The non-recursive architecture [5] for comb filters has lower power consumption compared with Hogenauer's cascaded-integrator-comb (CIC) architecture [3] especially when the filter orders and decimation ratios are high. In this paper the non-recursive architecture is employed to design the comb filter. Low power techniques have been developed for VLSI implementation of the non-recursive architecture.

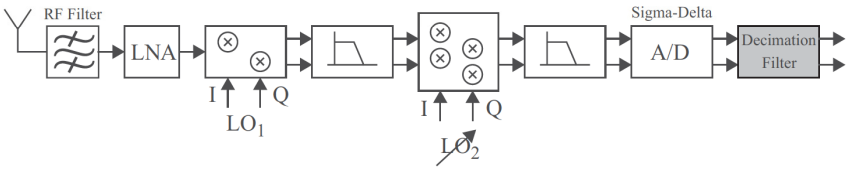


Fig. 1. Wide-band IF with double conversion receiver architecture.

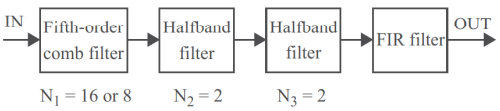


Fig. 2. Multi-stage linear-phase decimation filter.

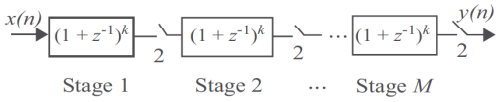


Fig. 3. The non-recursive architecture for comb decimation filters.

## REVIEW OF THE NON-RECURSIVE ARCHITECTURE

Comb filters has the following transfer function

$$H(z) = \left(\frac{1-z^{-N}}{1-z^{-1}}\right)^k = \left(\sum_{i=0}^{N-1} z^{-i}\right)^k \qquad (1)$$

where $N$ is the decimation ratio and $k$ is the filer order. Notice that sometimes a scaling factor $1 / N^k$ is included in the transfer function in order to make the dc gain unity.

Usually the decimation factor $N$ is chosen to be $M$-th power-of-two, i.e. $N = 2^M$. The transfer function can be rewritten as

$$H(z) = (1+z^{-1})^k (1+z^{-2})^k (1+z^{-4})^k \ldots \left(1+z^{-2^{M-1}}\right)^k \qquad (2)$$

By applying the commutative rule, the non-recursive architecture for comb decimation filters is resulted, shown in Fig. 3. The switches in the figure indicate the reduction in the sampling rates by a factor of 2. Every stage is a simple FIR filter (i.e., $(1+z^{-1})^k$). The word length increases through every stage by $k$ bits but the sampling rate decreases through every stage by a factor of 2. Reducing the sampling rates as early as possible helps to save power consumption. On the other hand, the wordlength of the first stage is very short ($m + k$, where $m$ is the wordlength of the input $x(n)$) so the non-recursive architecture can achieve higher speed compared with the CIC architecture.

## LOW POWER IMPLEMENTATION OF THE NON-RECURSIVE ARCHITECTURE

One approach to implement each stage $(1+z^{-1})^k$ is to cascade the $(1+z^{-1})$ processing element, shown in Fig. 4(a). In this paper $k$ is 5. By further investigating this approach, we noticed that half of the computational operation is not necessary in each stage since only half of the output data will be fed into the next stage because of the decimating by a factor of 2. In order to reduce power consumption the unnecessary computation should be eliminated. Based on this consideration, we developed a new technique to implement each stage. Using polyphase decomposition [6][7], the transfer function $(1+z^{-1})^5$ of each stage can be rewritten as

$$\begin{aligned} H(z) &= (1+z^{-1})^5 = 1 + 5z^{-1} + 10z^{-2} + 10z^{-3} + 5z^{-4} + z^{-5} \\ &= (1 + 10z^{-2} + 5z^{-4}) + z^{-1}(5 + 10z^{-2} + z^{-4}) \\ &= E_0(z^2) + z^{-1}E_1(z^2) \end{aligned} \qquad (3)$$

where $E_0(z^2)$ and $E_1(z^2)$ are polyphase components. By applying commutative rule, a low-power polyphase implementation for each stage is resulted, shown in Fig. 4(b). Where

$$\begin{aligned} E_0(z) &= 1 + 10z^{-1} + 5z^{-2} \\ E_1(z) &= 5 + 10z^{-1} + z^{-2} \end{aligned} \qquad (4)$$

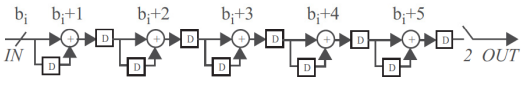


Fig. 4(a). An implementation of stage *i* by cascading $(1 + z^{-1})$ computational element.

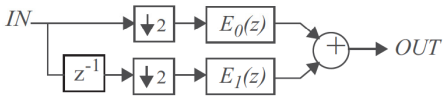


Fig. 4(b). Polyphase implementation for each stage.

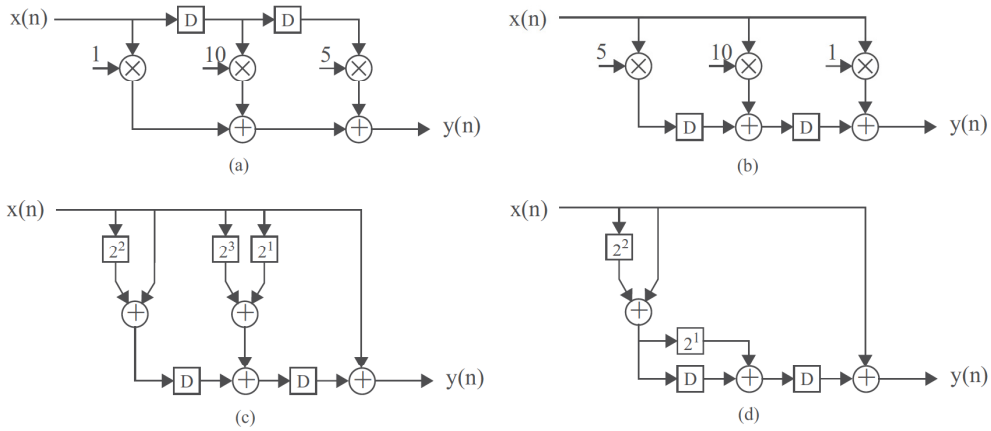


Fig. 5. Implementation of $E_0(z)$ (a) The direct-form structure for FIR filter; (b) The data-broadcast structure; (c) The multiplications are simplified to a few of shifts and adds; (d) The low-power implementation with substructure sharing.

In this implementation, the input is decimated by 2 at first and the odd-numbered input data will go through $E_0(z)$ and even-numbered input data will go through $E_1(z)$. The output data are obtained by adding all polyphase components ($E_0(z)$ and $E_1(z)$) together. Notice that each polyphase operates at half of the input sampling rate (i.e., $f_{si} / 2$, where $f_{si}$ is the input sampling rate of stage *i*) meanwhile the unnecessary computation has been eliminated. Therefore polyphase implementation consumes less power than the cascade implementation.

Low power implementation of each polyphase component (FIR filter) is also important. A FIR filter can be designed with different structures. We take polyphase component $E_0(z)$ (see (4)) as an example to illustrate this. The direct-form structure is shown in Fig. 5(a). The critical path for processing a new sample is limited by 1 multiply and 2 add times so this structure has lower speed. An alternative approach to reduce the critical path of the direct-form structure without introducing any pipelining registers is to transpose the structure with the transposition theorem [8]. Fig. 5(b) shows the transposed structure which is referred to as data-broadcast structure. Notice that the critical path is reduced to 1 multiply and 1 add times so the data-broadcast structure can operate at higher speed. This makes it possible to use simple lower-speed adder to perform the addition in the moderate-speed applications instead of high-speed adders, such as carry-select adders and carry-lookahead adders, etc. Power consumption caused by the addition operation can be reduced. Another low-power issue is how to implement the multiplications in Fig. 5(b). First the multiplications are simplified to a few of shifts and adds, shown in Fig. 5(c). $5x(n)$ is calculated as $2^2x(n) + 2^0x(n)$ and $10x(n)$ is calculated as $2^3x(n) + 2^1x(n)$. The data-broadcast structure make it possible to use substructure sharing techniques to reduce the power consumption. For example, $10x(n)$ can be obtained by only left-shift $5x(n)$ 1 bit instead of using 4 shifts and 1 add. This is shown in Fig. 5(d).

Finally the block diagram of the whole decimation filter is shown in Fig. 6. There are four

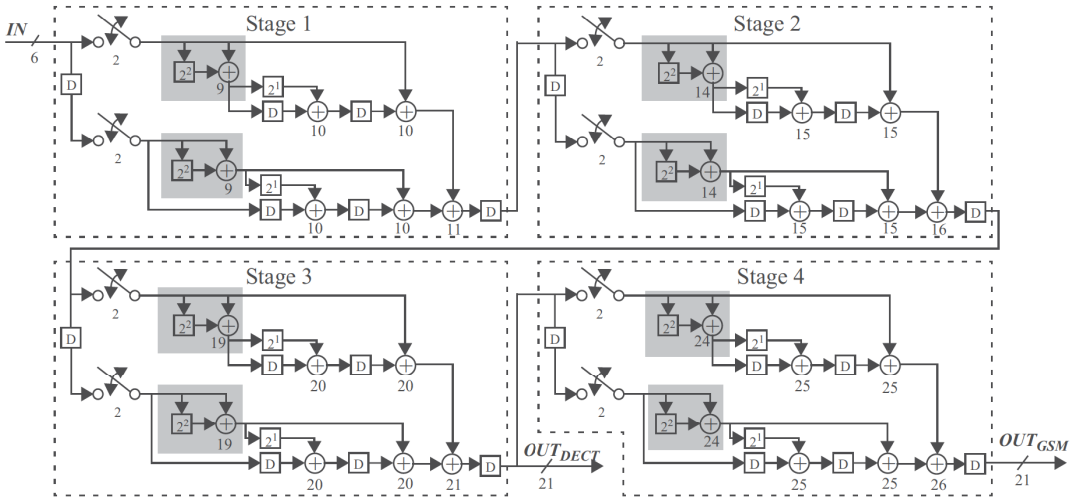


Fig. 6. The block diagram of the fifth order comb decimation filter with a decimation ratio of 8 or 16.

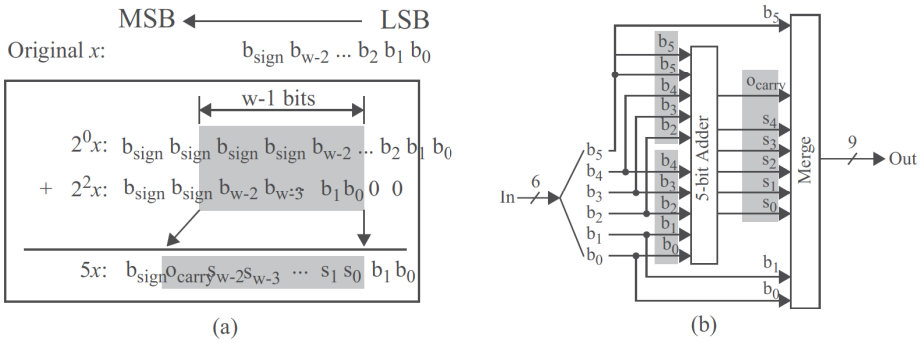


Fig. 7. Low power implementation of 5x (= $2^2$x + $2^0$x).

stages. Each stage is implemented with the same structure (polyphase plus data-broadcast). The switches in the figure indicate the reduction of the sampling rate, and the number close to each adder indicates the wordlength of the adder. For GSM applications, the four stages are needed since the decimation ratio is 16. But for DECT applications, only first three stages are needed because the decimation ratio is 8. In this case, a reset signal will make stage 4 inactive to save power consumption.

Recall that each polyphase component has the $5x(n)$ operation, and $5x(n)$ is calculated as $2^2x(n) + 2^0x(n)$ (see the shadowed areas in Fig. 6). If the wordlength of $x(n)$ is $w$, a $(w+3)$-bit adder is needed in the 2's complement arithmetic to avoid the overflow problem. At first $2^0x(n)$ and $2^2x(n)$ are extended to $(w+3)$ bits as shown in Fig. 7(a). Notice that the two LSB bits of $2^2x(n)$ are zero and the two MSB bits of $2^0x(n)$ and $2^2x(n)$ are $b_{sign}$. The two LSB bits of $5x(n)$ will be "$b_1b_0$" and the first MSB bit of $5x(n)$ will be "$b_{sign}$". In actual design we only need a $(w-1)$-bit adder (the shadowed area in Fig. 7(a)) to get other bits. Therefore we save 4 bits in the adder wordlength. As an example, assume $w = 6$. We only need a 5-bit adder

instead of a 9-bit adder to complete the $5x(n)$ operation as shown in Fig. 7(b).

## CONCLUSIONS

A low-power fifth-order comb decimation filter with programmable decimation ratios (16 and 8) and sampling rates (12.8 MHz and 44.8 MHz) has been presented for GSM and DECT applications. Low power consumption is achieved by the following approaches: 1) the non-recursive architecture for comb decimation filter is employed; 2) unnecessary computation is eliminated with polyphase implementation of each stage; 3) each polyphase component is implemented with data-broadcast structure, and multiplications are simplified to a few of shifts and adds then substructure sharing techniques is applied to minimize the number of shifts and adds; 4) 5x(n) is realized with a ($w$-1)-bit adder instead of a ($w$+3)-bit adder.

## ACKNOWLEDGMENTS

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## Publications:

Professor Hannu Tenhunen recent **research interest and publications activities** have been in areas:

- Interconnect centric and robust/interference free design of electronic systems, architectures and methods
- Design of embedded and integrated systems towards signal processing, communication, and internet-of-things applications
- Flexible electronic systems and intelligent integration to paper and pulp based substrates and packages
- 3D integration technologies and modelling & design of 3D circuits and systems using through-silicon-via (TSV)
- VLSI applications in personal communication and fundamental design constraints and future paradigms necessary to harvest the technology potential
- Platform based design methods and architectures based network-on-chip architectures
- Embedded dependable systems based on agent controlled autonomic systemic architectures (HW/SW)
- VLSI Design and Circuits, especially towards DSP

- IC Mixed Signal Circuits and Systems including sigma-delta A/D and D/A
- Integrated Heterogeneous Sensible Systems
- Technology policies and educational strategies in area of rapidly evolving ICT technology.

He holds in these areas 2 thesis, 9 international patents in multiple countries, 127 reviewed journal and book publications, 656 reviewed international conference publications, and 172 unreviewed or local conference and workshop publications and presentations (not including all).

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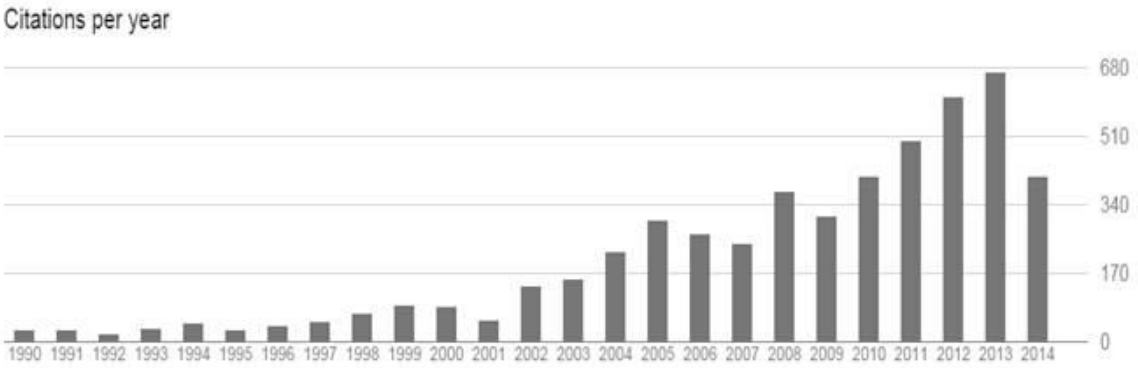


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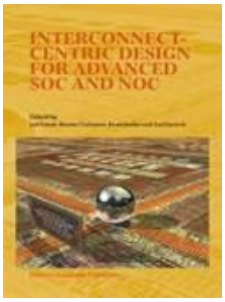


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2. H. Tenhunen, innovation Platform: Local governance for Knowledge and Innovation Community Node, invited keynote talk in Complex EIT Workshop, June 2008

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49. H. Tenhunen: Microelectronics: Revolution of Technology, invited presentation in Studia Generalia, University of Helsinki, Finland, April 1989

50. H. Tenhunen: CAE for ASIC System Design; invited presentation in ASIC-89 industrial course, Helsinki University of Technology, Finland, March 1989

51. H. Tenhunen: National Microelectronics Program 1987 -1989; presentation in National IC Design Workshop, Finland, April 1989

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70. H. Tenhunen; Kemi 2000 Programme, Kemi Technology Seminar, September 1991

71. H. Tenhunen: Microelectronics and ASIC Education for Polytechnics, invited presentation in Polytechnic Teacher Seminar, October 1991

72. H. Tenhunen; Fast Prototyping in DSP System Design, invited tutorial presentation in Electronic System Design Workshop, Stockholm, April 1992.

73. H. Tenhunen; Fast Prototyping - A Myth in Real Life, in NORSILC Workshop, FPGA Technologies, Lund, May 1992

74. H. Tenhunen; Nordic Cooperation in Microelectronic Research, in 2nd Estonian-Finnish Workshop on Digital Systems and Signal Processing, January 1992, Tallinn, Estonia.

75. H. Tenhunen; Industry /University Cooperation in Microelectronics Research, in NUTEK Workshop on Microelectronics System Research, Stockholm, February 1992.

76. D. Kerek, H. Olson & H. Tenhunen; Design of Walkstation Radio, in Walkstation Workshop, March 1994, Sweden.

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89. B. Oelmann & H. Tenhunen “Comparison of Self-Timed and Synchronous High-Speed VLSI/ULSI Circuits Using System-Level Performance Modelling”, PS-7, GigaHertz Conference, Gothenburg, 1995.

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91. M. Mokhtari, T. Juhola, G. Schuppener, H. Tenhunen “2GS/s, 4 Bit Flash A/D Converter in the P28 Technology”, PS-11, GigaHertz Conference, Gothenburg, 1995.

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93. P. Zhu, H. Tenhunen “A 100 MHz Switched-Current Sigma-Delta Modulator for A/D Converter in 0,6 um Cmos Technology”, PS-14, GigaHertz Conference, Gothenburg, 1995.

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96. H. Tenhunen, N. Tan, “Sigma-Delta”- Course for Ericsson, Stockholm, 1995.

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141. H. Tenhunen: High Frequency Packaging Technology, invited seminar presentation at Ericsson Radio System AB, Stockholm, 1998

142. H. Tenhunen: Codesign of Electronic Products, Ericsson seminar on Elektronik Produktframtakning, February 1996

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144. L-R. Zheng & H. Tenhunen: Single Level Integrated Packaging Modules for RF and HF Applications, in Nya Miljöanpassade Byggsätt för Elektronikproduktion Workshop, Stockholm, January 1999

145. H. Tenhunen: MEDIA: Strategic Research in Network Systems for Multimedia Mobile Computing, opening presentation in MEDIA workshop, February 1999

146. P. Ericsson & H. Tenhunen: Sampled RF.CMOS frontends, presentation in INWITE workshop, December 1998, Helsinki, Finland

147. L. Bingxin, L-R. Zheng & H. Tenhunen: Mixed Signal Coupling in Integrated Circuits for Sigma-Delta RF Front-ends, in INWITE workshop, December 1998, Helsinki, Finland

148. H. Tenhunen. Breeding the new generation of engineers. In National EDA-Träff, Stockholm, April 2000. Invited keynote talk.

149. H. Tenhunen, System-on-Chip Challenges, invited presentation in Electronic Design Center workshop, Stockholm, February 1998

150. H. Tenhunen, Trends in Electronic System Design, invited presentation in Mentor Graphcis workshop in EDA, Stockholm, 1996

151. H. Tenhunen: Restructruing of ASIC Design. Invited presentation in Mentor Graphics workshop on EDA, Stockholm, 1997

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