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Joy et al.

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(54) **MULTIPLE-THREAD PROCESSOR WITH IN-PIPELINE, THREAD SELECTABLE STORAGE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 211 days.

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(21) Appl. No.: **11/710,112**

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Primary Examiner—Eric Coleman

(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation of application No. 10/403,406, filed on Mar. 31, 2003, now Pat. No. 7,185,185, which is a continuation of application No. 09/309,734, filed on May 11, 1999, now Pat. No. 6,542,991.

(51) **Int. Cl.**
G06F 9/38 (2006.01)

(52) **U.S. Cl.** 712/220

(58) **Field of Classification Search** 712/220,
712/32, 215, 216, 233, 228

See application file for complete search history.

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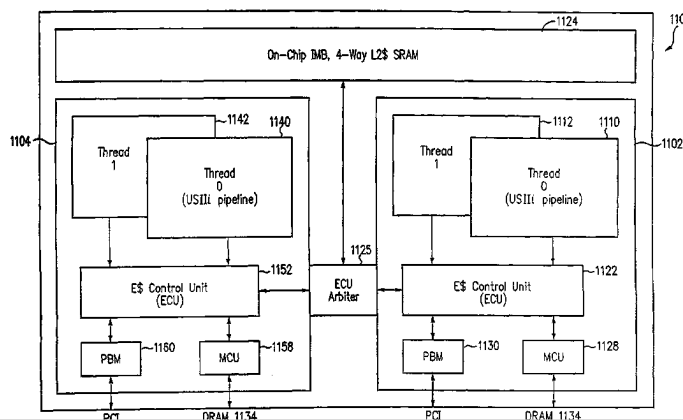
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(57) **ABSTRACT**

A processor reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time, by supporting and implementing both vertical multithreading and horizontal multithreading. Vertical multithreading permits overlapping or “hiding” of cache miss wait times. In vertical multithreading, multiple hardware threads share the same processor pipeline. A hardware thread is typically a process, a lightweight process, a native thread, or the like in an operating system that supports multithreading. Horizontal multithreading increases parallelism within the processor circuit structure, for example within a single integrated circuit die that makes up a single-chip processor. To further increase system parallelism in some processor embodiments, multiple processor cores are formed in a single die. Advances in on-chip multiprocessor horizontal threading are gained as processor core sizes are reduced through technological advancements.

1 Claim, 21 Drawing Sheets



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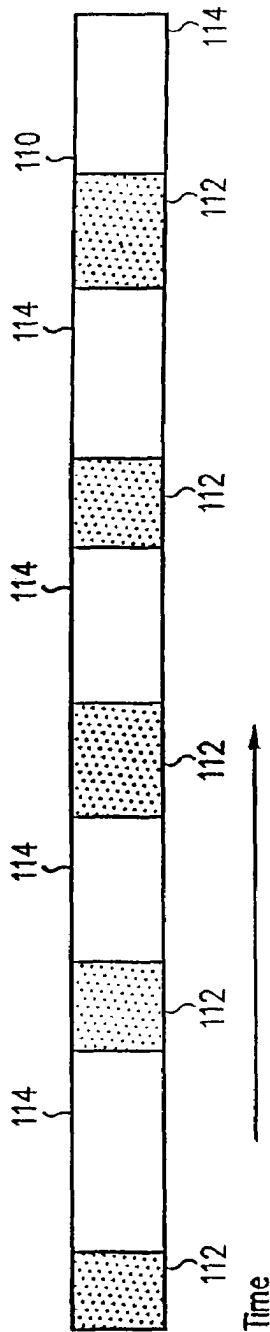


FIG. 1A

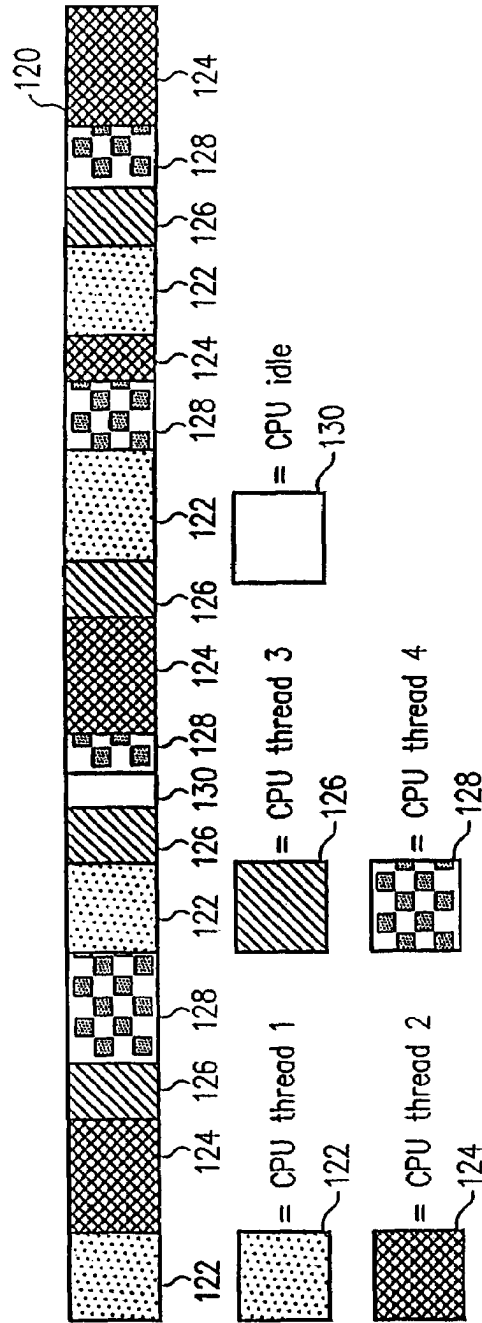


FIG. 1B

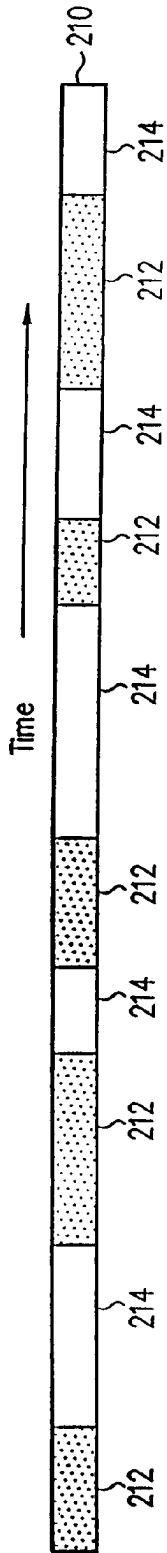


FIG. 2A

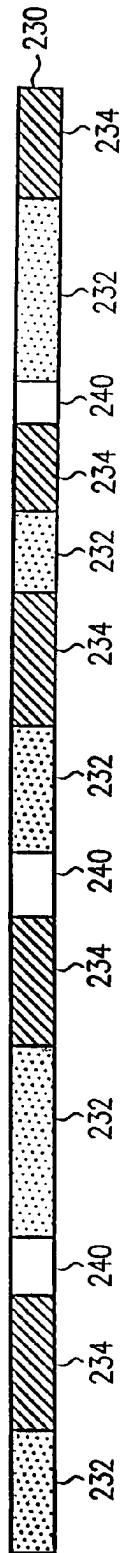


FIG. 2B

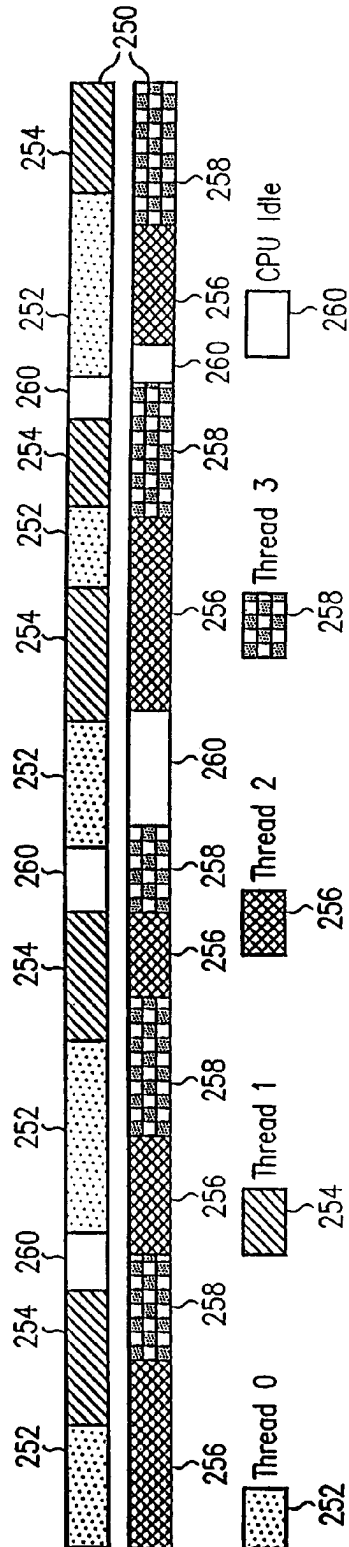


FIG. 2C

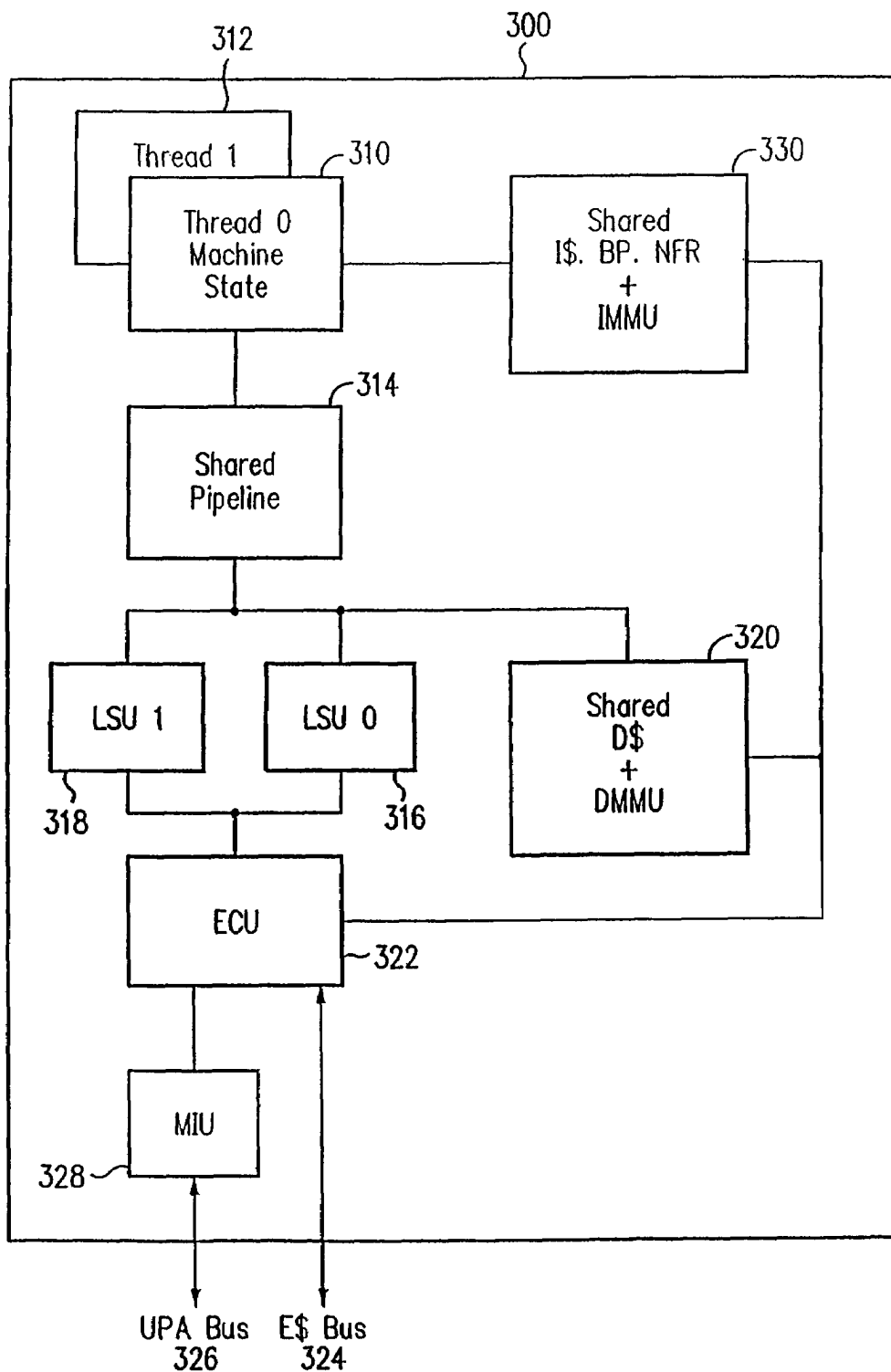


FIG. 3

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