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**Babaian et al.**

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(54) **SINGLE-CHIP MULTIPROCESSOR WITH  
CLOCK CYCLE-PRECISE PROGRAM  
SCHEDULING OF PARALLEL EXECUTION**

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**Related U.S. Application Data**

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(51) **Int. Cl.**  
**G06F 9/45** (2006.01)  
**G06F 9/30** (2006.01)

(52) **U.S. Cl.** ..... **717/161**; 717/150; 717/153;  
717/159; 712/220; 712/228

(58) **Field of Classification Search** ..... None  
See application file for complete search history.

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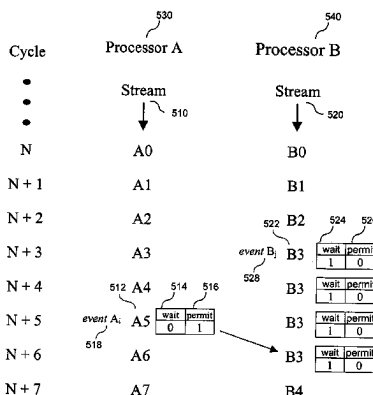
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(57) **ABSTRACT**

A single-chip multiprocessor system and operation method of this system based on a static macro-scheduling of parallel streams for multiprocessor parallel execution. The single-chip multiprocessor system has buses for direct exchange between the processor register files and access to their store addresses and data. Each explicit parallelism architecture processor of this system has an interprocessor interface providing the synchronization signals exchange, data exchange at the register file level and access to store addresses and data of other processors. The single-chip multiprocessor system uses ILP to increase the performance. Synchronization of the streams parallel execution is ensured using special operations setting a sequence of streams and stream fragments execution prescribed by the program algorithm.

**17 Claims, 12 Drawing Sheets**



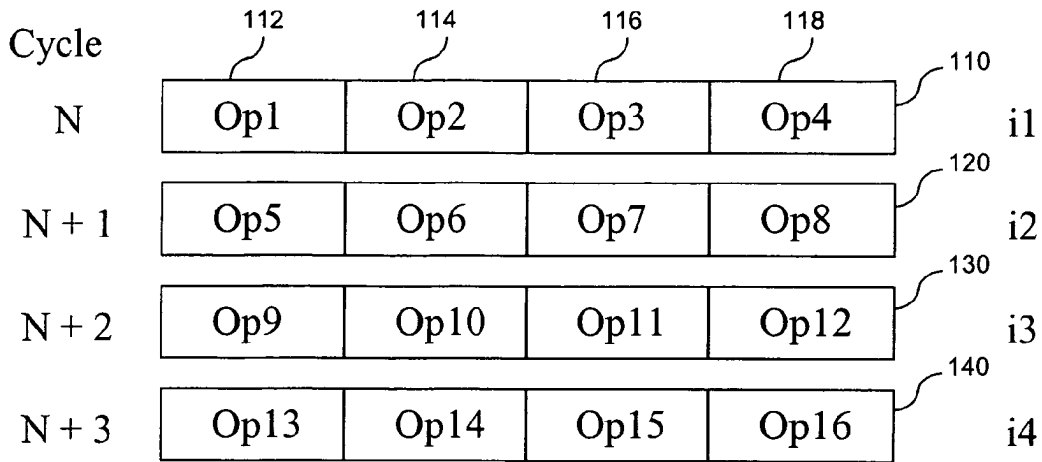


Fig. 1

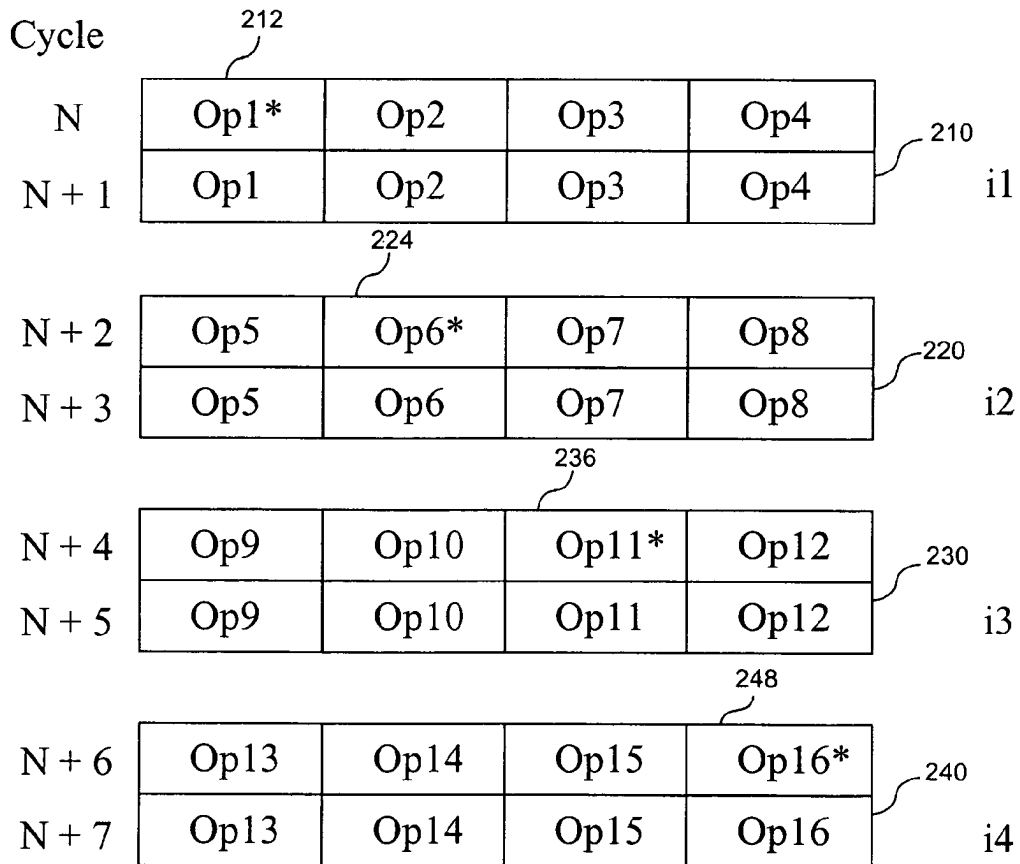


Fig. 2

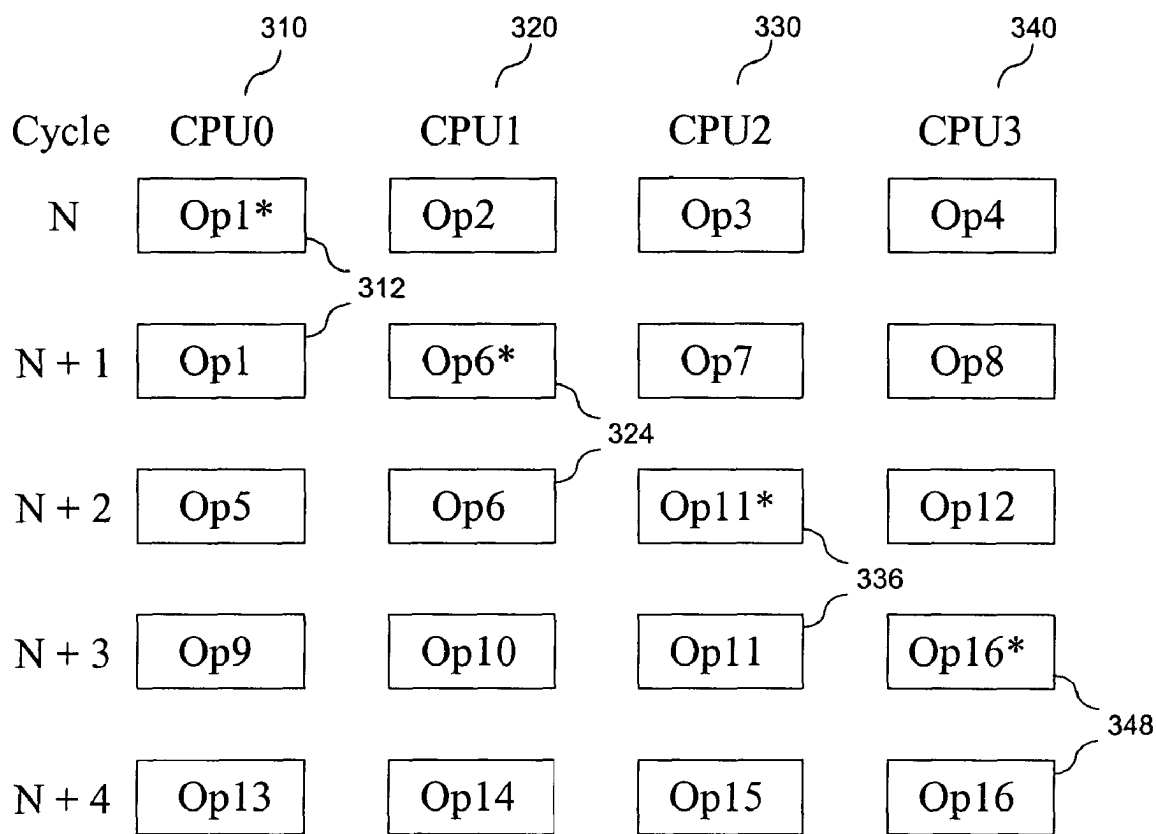


Fig. 3

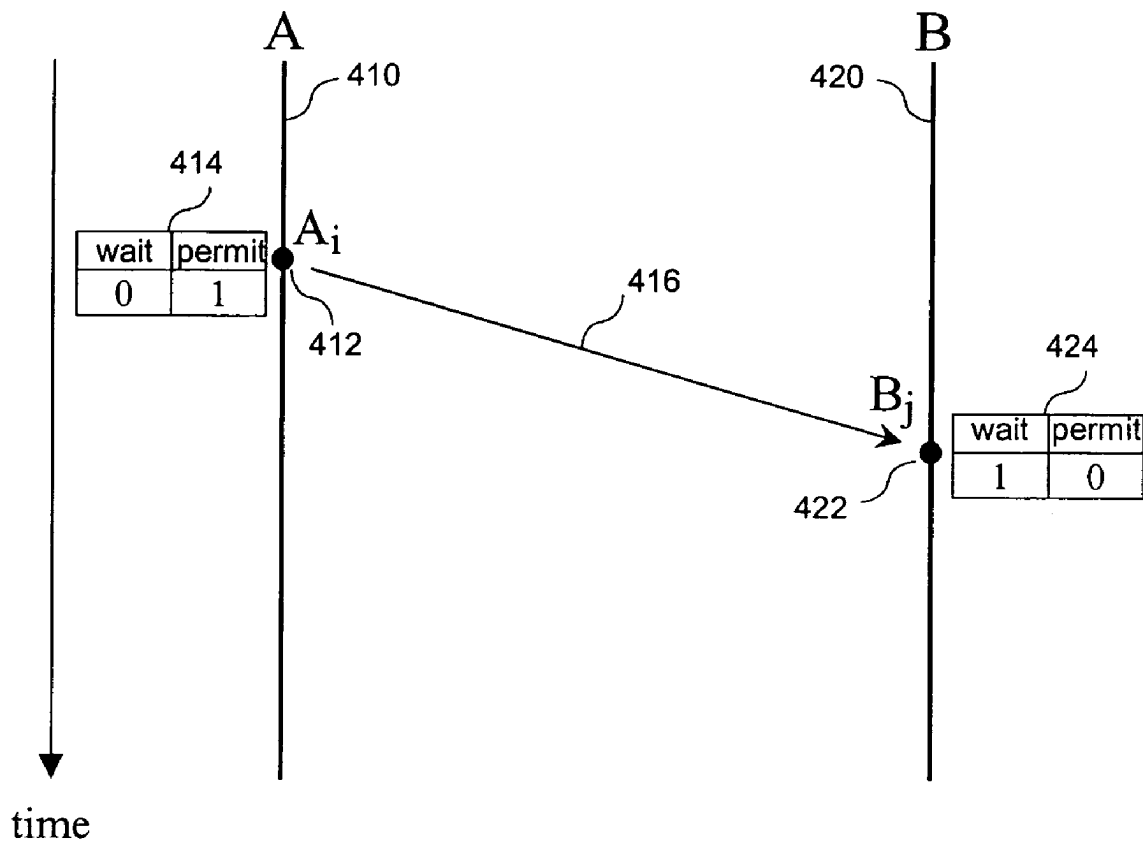


Fig. 4

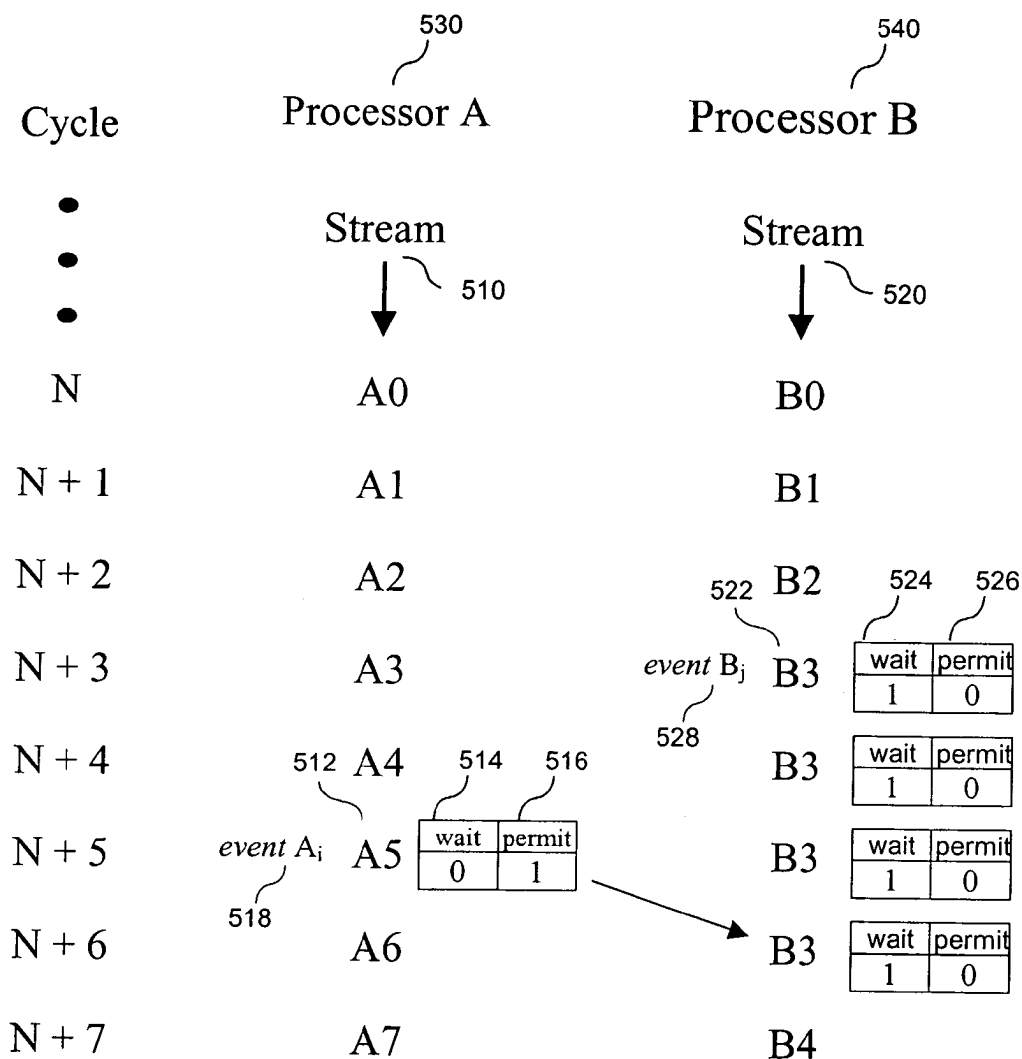


Fig. 5

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