MP 4.2 A DECT Transceiver Chip Set Using SiGe Technology

Matthias Bopp, Martin Alles, Meinolf Arens, Dirk Eichel, Stephan Gerlach, Rainer Götzfried, Frank Gruson, Michael Kocks, Gerald Krimmer, Reinhard Reimann, Bernd Roos, Martin Siegle, Jürgen Zieschang

TEMIC Semiconductor GmbH, Heilbronn, Germany

A fully-integrated RF-transceiver for DECT comprises two bipolar ICs including power amplifier, low-noise amplifier and VCO. Non-blind-slot and multi-slot capability is achieved by closed-loop modulation. The complete transceiver, which operates from 2.7 to 5V, avoids mechanical tuning, and requires <50 external components.

The complete RF transceiver, including VCO and synthesizer, is integrated on one chip. A second IC, implemented in SiGe-technology, includes a low-noise amplifier in the receive path as well as a power amplifier for the transmit path and a driver for an external PIN diode switch (Figure 4.2.1). High integration level of both ICs in TQFP48 and PSSOP16 packages allows use of a compact 2-layer PC board using cost-effective FR4 material and only one component side. Furthermore, the transceiver does not require any mechanical tuning in production by providing bus-controlled electronic tuning. It operates from 2.7 to 5V, avoiding negative supply voltage and supports simple power management by means of integrated regulators and multiple power-down modes. Also, the generation of the analog control signal for applied power ramping of the TDMA signal is integrated.

The transmit path starts with the fully-integrated FIR baseband filter. This Gaussian filter shapes the digital data stream precisely to keep adjacent channel emissions low (Figure 4.2.5). The integrated VCO with on-chip inductors operates at double the frequency of the DECT band around 3.8GHz. Its approximately -132dBc phase noise 5MHz offset meets the DECT specification at this critical point. The narrow-band spectrum is shown in Figure 4.2.2. This VCO is directly modulated by the Gaussian baseband signal and is subsequently divided by a factor of 2 to the final frequency band of DECT. Thus feedback from PA-driver and PA to the VCO is minimized.

Closed-loop modulation avoids distortion of the transmitted data stream by PLL operation without opening the loop. The principle of this circuit is illustrated in Figure 4.2.3. The binary data stream of the transmit data from the baseband chip is distributed to an integrated Gaussian baseband filter and to a modulation compensation circuit, a digital integrator. It derives the digital sum variation (i.e., the low frequency content) of the digital data stream. The reference signal of the PLL phase detector is shifted by a phase shifter, which is controlled by the modulation compensation block. Thus the phase detector of the PLL will not see any change of phase of its input signals and the PLL is not removing the modulation of the directly modulated VCO, hence working still in closed loop. Loop bandwidth is high enough to allow PLL settling times <25μs resulting in a cost-effective non-blind-slot solution. The quality of the closed loop modulated signal can be seen in the demodulated transmit signal eye diagram of Figure 4.2.4. Even for long sequences of 1s and 0s, the eye is open. Thus multislot operation is possible. Up to 23 slots can be collocated for a highly asymmetrical datalink as desirable in many data applications.

The transceiver IC-modulated output signal spectrum at 1.9GHz without external filtering is shown in Figure 4.2.5. The 0dBn output level is amplified to 26dBm by the SiGe power amplifier. The power amplifier has 33dB small-signal gain, 38% max PAE and 26.6dBm saturated output power at 3V supply (Figure 4.2.6). The signal passes the PIN-diode switch and the only dielectric RF bandpass filter of the system. At the antenna, the output level is 24dBm.

The receiver is based on a single-conversion superheterodyne concept. Coming from the antenna input with a characteristic impedance of 50Ω the received signal passes through a dielectrical bandpass filter. This preselector provides far-off selectivity and improves image rejection. The following PIN diode switch implemented with a λ/4-transmission line combines low insertion loss and minimum current consumption in receive mode. Next, the signal is amplified in the LNA with 19dB gain and 1.7dB noise figure (Figure 4.2.7). No external matching circuitry is necessary and the high reverse isolation of ~50dB reduces the local oscillator leakage to the antenna and simplifies PC board design. The LNA output signal is passed to the image-rejection mixer in the transceiver IC. The mixer cells are double-balanced and the 90° phase shift on the LO side is accomplished inherently by dividing the VCO signal down by a factor of two using both master and slave outputs. The RC-CR phase shifters at the IF side are fully integrated and the symmetrical output signal is coupled to a fully-symmetrical SAW filter (Figure 4.2.8). The mixer features 25dB image rejection and converts the signal down to 110MHz single IF, is chosen for availability of various low-cost filters. No second front-end filter is needed to achieve 70dB overall image rejection. The large-signal compatibility is given in Figure 4.2.9. Next, the signal is passed to the IF amplifier and FM demodulator. The quadrature demodulator tank circuit is tuned internally by an integrated varactor via bus control. Finally the demodulated signal is baseband filtered, buffered and passed to the baseband processing IC. A received signal strength indicator (RSSI) signal is derived in the IF chain. The overall dynamic range of the RSSI measured at the IF input is approx. 90dB to guarantee 60dB minimum RSSI dynamic range of the complete receiver and allow the application of SAW-filters with insertion losses from 6 to 17dB as well as provide margin for production tolerances.

The transceiver chip is fabricated in a bipolar process. The front-end IC is produced in SiGe1 technology, including npn HBTs with and without selectively implanted collector on the same wafer. In addition, spiral inductors, nitride capacitors, three types of poly resistors, a LPNP, RF- and DC-ESD protection and varactor diodes are incorporated in the technology (Table 4.2.1). The SiGe HBTs have 30GHz f_T with 6V BVCEO and 50GHz f_T with 3V BVCEO. The maximum f_T and f_{max} are at current densities of 0.3mA/μm^2 and 0.65mA/μm^2 for the non-SIC and the SIC devices, respectively. Due to the high base doping the early voltage is above 50V.

Packaging technologies with the chipscale technology will reduce cost (Figure 4.2.10). Another possible direction is a true one-chip RF transceiver including PA and LNA in a SiGe BiCMOS technology.

Acknowledgements:
The authors thank the team in layout, technology (H. Dietrich, U. Seiler, A. Schüppen and D. Zerrweck) and application support.

References:
[1] TEMIC Semiconductor, Datasheets:
"DECT RF / IF IC U2761B," Rev.A4, 10. March 1998.
"DECT PLL / TX IC U2785B," Rev.A4, 13. Oct. 1998.
"DECT SiGe Front End IC U7004B," Rev.A5, 10. June 1998.
[2] R. Götzfried, F. Beisswanger, and S. Gerlach, "Design of RF Integrated Circuits Using SiGe Bipolar Technology," IEEE J. Solid-State Circuits, vol. 33, pp. 1417-1422, Sept. 1998.
[3] A. Schüppen, H. Dietrich, S. Gerlach, H. Höhnemann, J. Arndt, U. Seiler, R. Götzfried, U. Erben, and H. Schumacher, "SiGe-technology and Components for Mobile Communication Systems," in Bipolar/BiCMOS Circuits Technol. Meeting, Minneapolis, MN, Sept. 1996, pp. 130-133.
[4] J. Sevenhans, B. Verstraeten, G. Fletcher, H. Dietrich, W. Rabe, J. L. Bacq, J. Varin, and J. Dulongpont, "Silicon Germanium and Silicon Bipolar RF Circuits for 2.7V Single Chip Radio Transceiver Integration," proceedings of IEEE 1998 CICC, p. 409 to 412.
[5] J. Sevenhans et al., "An Analog Radio Front-end Chip Set for a 1.9GHz Mobile Radio Telephone Application," proceedings of ISSCC1994, p. 44-45.

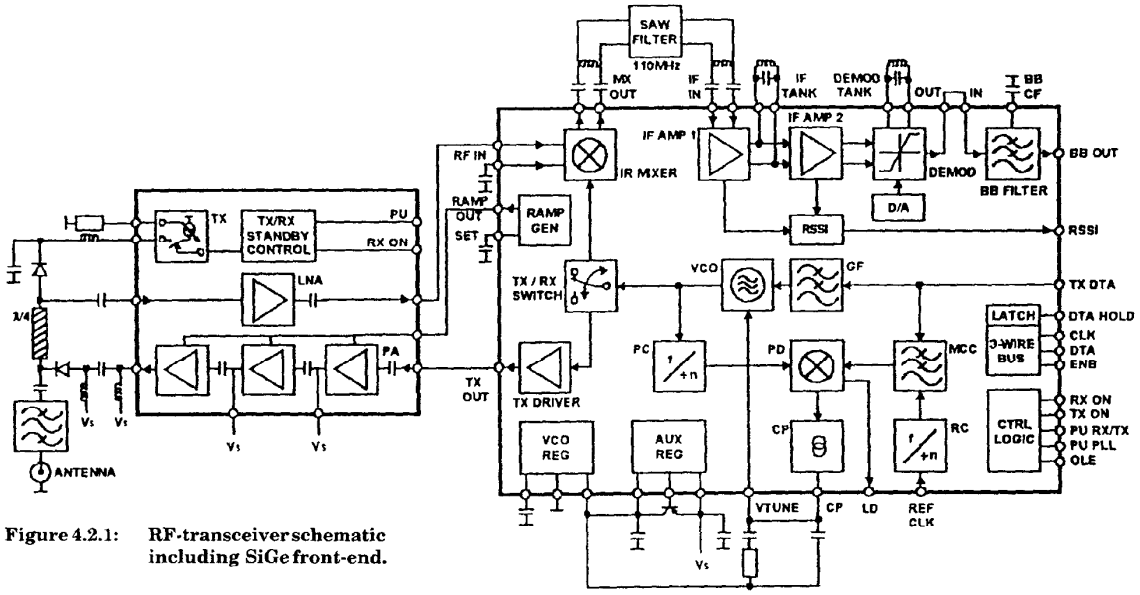

Figure 4.2.1: **RF-transceiver schematic including SiGe front-end.**

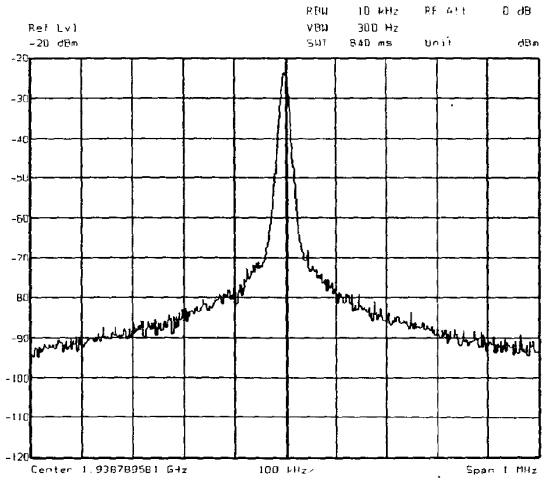

Figure 4.2.2: **Integrated VCO phase noise spectrum.**

Device	Parameter	SiGe1	UHF5S
npn	min. emitter	0.8x1.6 μm^2	0.75x2.0μm^2
np (non-SIC)	f_T (GHz)	30	15
npn (SIC) f_T (GHz)	50	30	
Lpnp	h_{FE}	10	40
Vpnp	f_T (GHz)	n.a.	2
I2L		n.a.	available
MIM capacitor	$f_F / \mu m^2$	1.1	n.a.
Poly resistor	Ω/sq	4.5 / 110 / 400	100 / 825
Spiral inductor	L / nH	0.5...20	0.5...20
Diode		varactor	varactor
ESD		RF / DC	DC

n.a. = not available

Table 4.2.1: **Technology overview.**

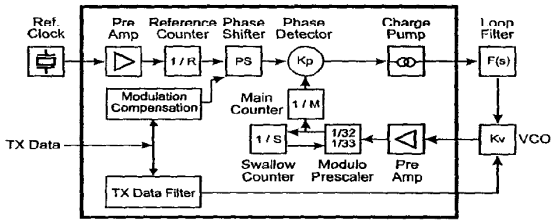

Figure 4.2.3: **Closed loop modulation concept.**

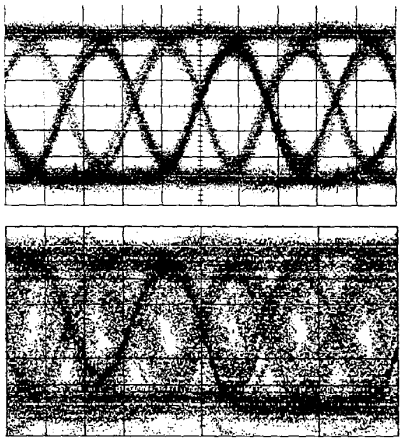

Figure 4.2.4: **Closed-loop modulation eye pattern with modulation compensation circuit enabled and disabled.**

Figure 4.2.5, Figure 4.2.6, Figure 4.2.7, Figure 4.2.8, Figure 4.2.9, and Figure 4.2.10: **See page 447.**

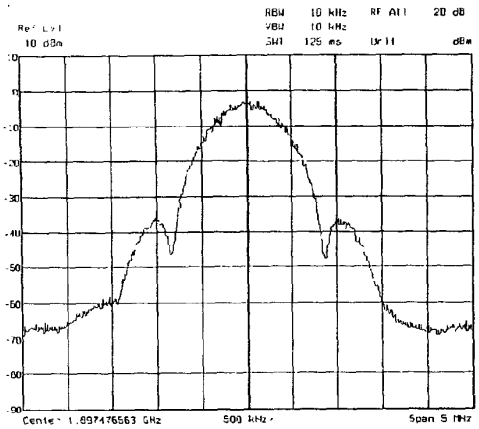

Figure 4.2.5: Transceiver IC transmit spectrum.

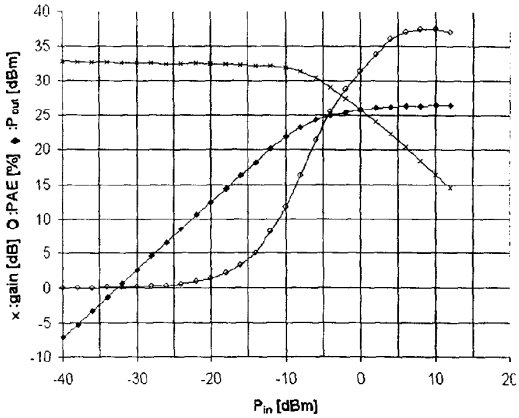

Figure 4.2.6: PA of SiGe frontend : Gain, Pout, PAE vs. Pin. at Vcc = 3V).

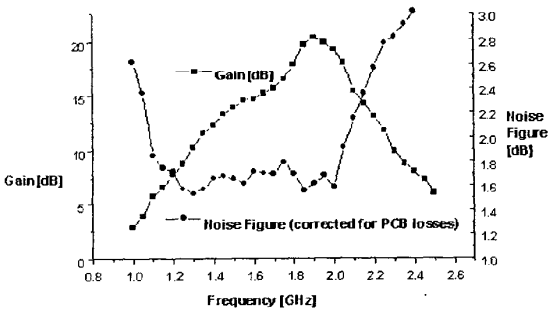

Figure 4.2.7: LNASiGe frontend : Gain, NF vs. Frequency.

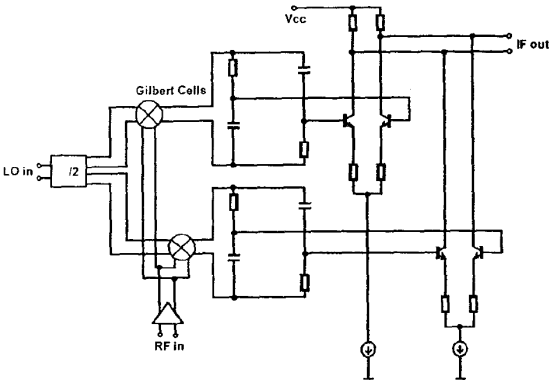

Figure 4.2.8: IR-mixer schematic.

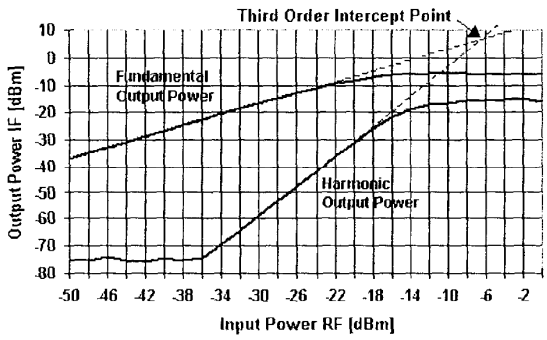

Figure 4.2.9: IR-mixer large-signal compatibility.

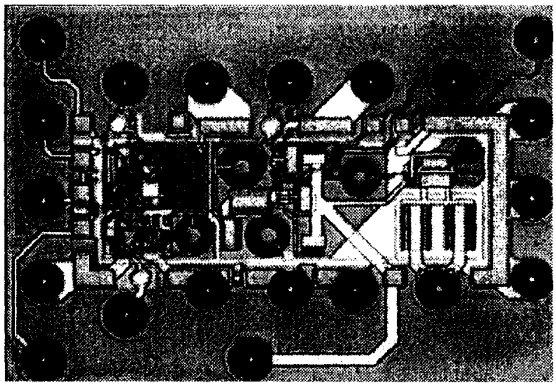

Figure 4.2.10: SiGe frontend IC in chip scale package