Super Sequencer™ with Margining Control and Auxiliary ADC Inputs

ADM1066

FEATURES

- Complete supervisory and sequencing solution for up to 10 supplies
- 10 supply fault detectors enable supervision of supplies to
  - <0.5% accuracy at all voltages at 25°C
  - <1.0 % accuracy across all voltages and temperatures
- 5 selectable input attenuators allow supervision
  - Supplies up to 14.4 V on VH
  - Supplies up to 6 V on VP1 to VP4
- 5 dual-function inputs, VX1 to VX5
  - High impedance input to supply fault detector with thresholds between 0.573 V and 1.375 V
  - General-purpose logic input
- 10 programmable output drivers, PDO1 to PDO10
  - Open collector with external pull-up
  - Push/pull output, driven to VDDCAP or VPn
  - Open collector with weak pull-up to VDDCAP or VPn
  - Internally charge-pumped high drive for use with external N-FET (PDO1 to PDO6 only)
- Sequencing engine (SE) implements state machine control of PDO outputs
  - State changes conditional on input events
  - Enables complex control of boards
  - Power-up and power-down sequence control
  - Fault event handling
  - Interrupt generation on warnings
  - Watchdog function can be integrated in SE
  - Program software control of sequencing through SMBus
- Complete voltage-margining solution for 6 voltage rails
- 6 voltage output 8-bit DACs (0.300 V to 1.551 V) allow voltage adjustment via dc-to-dc converter trim/feedback node
- 12-bit ADC for readback of all supervised voltages
- 2 auxiliary (single-ended) ADC inputs
- Reference input (REFIN) has 2 input options
  - Driven directly from 2.048 V (±0.25%) REFOUT pin
  - More accurate external reference for improved ADC performance
- Device powered by the highest of VPn or VH for improved redundancy
- User EEPROM: 256 bytes
- Industry-standard 2-wire bus interface (SMBus)
- Guaranteed PDO low with VH, VPn = 1.2 V
- 40-lead 6 mm × 6 mm LFCSP
- 48-lead 7 mm × 7 mm TQFP

For more information about the ADM1066 register map, refer to the AN-698 Application Note.

FUNCTIONAL BLOCK DIAGRAM

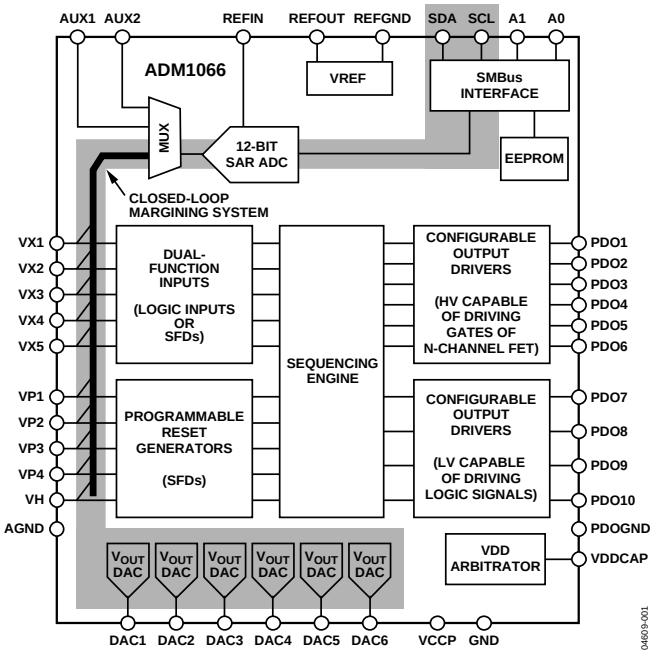

Figure 1.

APPLICATIONS

- Central office systems
- Servers/routers
- Multivoltage system line cards
- DSP/FPGA supply sequencing
- In-circuit testing of margined supplies

GENERAL DESCRIPTION

The ADM1066 is a configurable supervisory/sequencing device that offers a single-chip solution for supply monitoring and sequencing in multiple-supply systems. In addition to these functions, the ADM1066 integrates a 12-bit ADC and six 8-bit voltage output DACs. These circuits can be used to implement a closed-loop margining system that enables supply adjustment by altering either the feedback node or reference of a dc-to-dc converter using the DAC outputs.

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Rev. B

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REVISION HISTORY

5/06—Rev. A to Rev. B

1/05—Rev. 0 to Rev. A

10/04—Revision 0: Initial Version

GENERAL DESCRIPTION

(continued from Page 1)

Supply margining can be performed with a minimum of external components. The margining loop can be used for in-circuit testing of a board during production (for example, to verify the board's functionality at −5% of nominal supplies), or can be used dynamically to accurately control the output voltage of a dc-to-dc converter.

The device also provides up to 10 programmable inputs for monitoring under, over, or out-of-window faults on up to 10 supplies. In addition, 10 programmable outputs can be used as logic enables. Six of them can also provide up to a 12 V output for driving the gate of an N-channel FET, which can be placed in the path of a supply.

The logical core of the device is a sequencing engine. This state-machine-based construction provides up to 63 different states. This design enables very flexible sequencing of the outputs, based on the condition of the inputs.

The device is controlled via configuration data that can be programmed into an EEPROM. The whole configuration can be programmed using an intuitive GUI-based software package provided by Analog Devices, Inc.

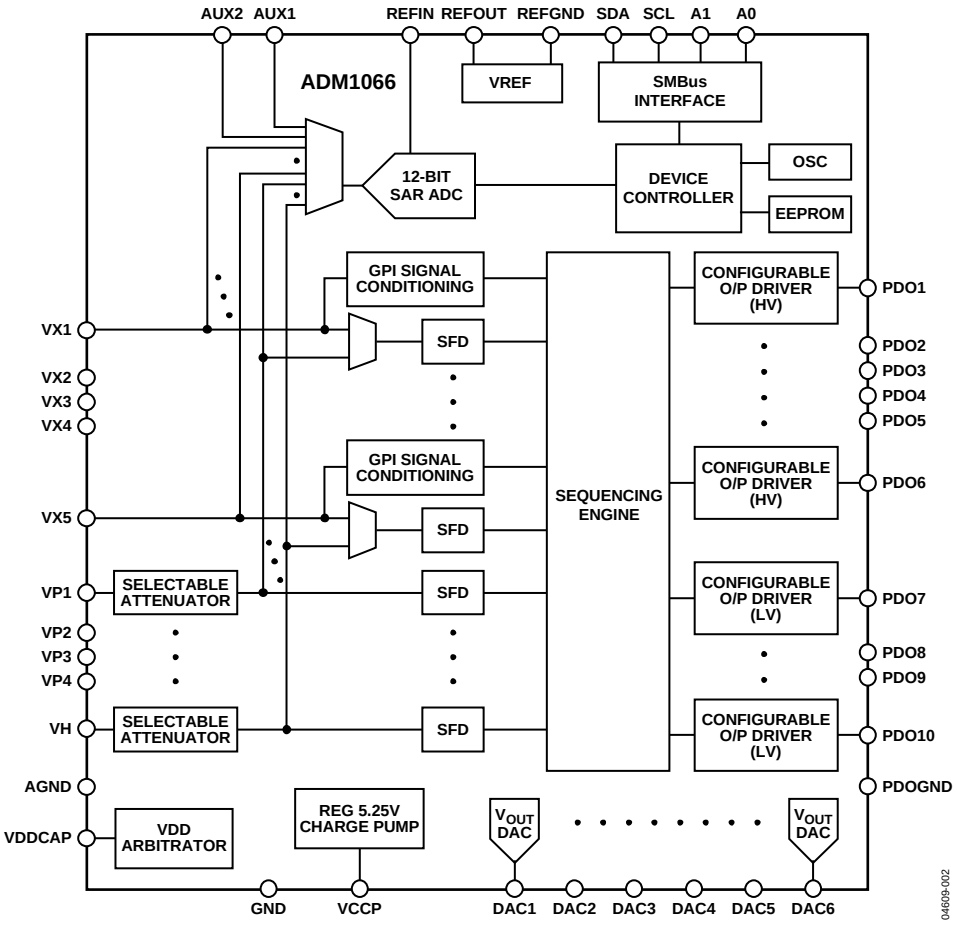

Figure 2. Detailed Block Diagram

SPECIFICATIONS

VH = 3.0 V to 14.4 V[1], VPn = 3.0 V to 6.0 V[1], T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY ARBITRATION					
VH, VPn	3.0			V	Minimum supply required on one of VPn, VH
VP			6.0	V	Maximum VDDCAP = 5.1 V, typical
VH			14.4	V	VDDCAP = 4.75 V
VDDCAP	2.7	4.75	5.4	V	Regulated LDO output
C_{VDDCAP}	10			µF	Minimum recommended decoupling capacitance
POWER SUPPLY					
Supply Current, I_{VH}, I_{VPn}		4.2	6	mA	VDDCAP = 4.75 V, PDO1 to PDO10 off, DACs off, ADC off
Additional Currents					
All PDO FET Drivers On		1		mA	VDDCAP = 4.75 V, PDO1 to PDO6 loaded with 1 µA each, PDO7 to PDO10 off
Current Available from VDDCAP			2	mA	Maximum additional load that can be drawn from all PDO pull-ups to VDDCAP
DACs Supply Current		2.2		mA	6 DACs on with 100 µA maximum load on each
ADC Supply Current		1		mA	Running round-robin loop
EEPROM Erase Current		10		mA	1 ms duration only, VDDCAP = 3 V
SUPPLY FAULT DETECTORS					
VH Pin					
Input Impedance		52		kΩ	
Input Attenuator Error		±0.05		%	Midrange and high range
Detection Ranges					
High Range	6		14.4	V	
Midrange	2.5		6	V	
VPn Pins					
Input Impedance		52		kΩ	
Input Attenuator Error		±0.05		%	Low range and midrange
Detection Ranges					
Midrange	2.5		6	V	
Low Range	1.25		3	V	
Ultralow Range	0.573		1.375	V	No input attenuation error
VX Pins					
Input Impedance	1			MΩ	
Detection Ranges					
Ultralow Range	0.573		1.375	V	No input attenuation error
Absolute Accuracy			±1	%	VREF error + DAC nonlinearity + comparator offset error + input attenuation error
Threshold Resolution		8		Bits	
Digital Glitch Filter		0		µs	Minimum programmable filter length
		100		µs	Maximum programmable filter length
ANALOG-TO-DIGITAL CONVERTER					
Signal Range	0		V_{REFIN}	V	The ADC can convert signals presented to the VH, VPn, and VXn pins. VPn and VH input signals are attenuated depending on the selected range. A signal at the pin corresponding to the selected range is from 0.573 V to 1.375 V at the ADC input.
Input Reference Voltage on REFIN Pin, V_{REFIN}		2.048		V	
Resolution		12		Bits	
INL			±2.5	LSB	Endpoint corrected, V_{REFIN} = 2.048 V

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