

[54] **CONTROLLER FOR A SYNCHRONOUS DRAM THAT MAXIMIZES THROUGHPUT BY ALLOWING MEMORY REQUESTS AND COMMANDS TO BE ISSUED OUT OF ORDER**

FOREIGN PATENT DOCUMENTS

549139 6/1993 European Pat. Off. .

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[21] Appl. No.: 437,975

[22] Filed: **May 10, 1995**

[51] Int. Cl.⁶ **G06F 13/00**

[52] U.S. Cl. **395/481**; 364/DIG. 1; 365/233; 395/432; 395/477; 395/478; 395/485; 395/494; 395/496

[58] Field of Search 365/233; 395/432, 395/477, 478, 481, 485, 494, 496

Primary Examiner—Frank J. Asta
 Attorney, Agent, or Firm—Burns, Doane, Swecker & Mathis

[57] **ABSTRACT**

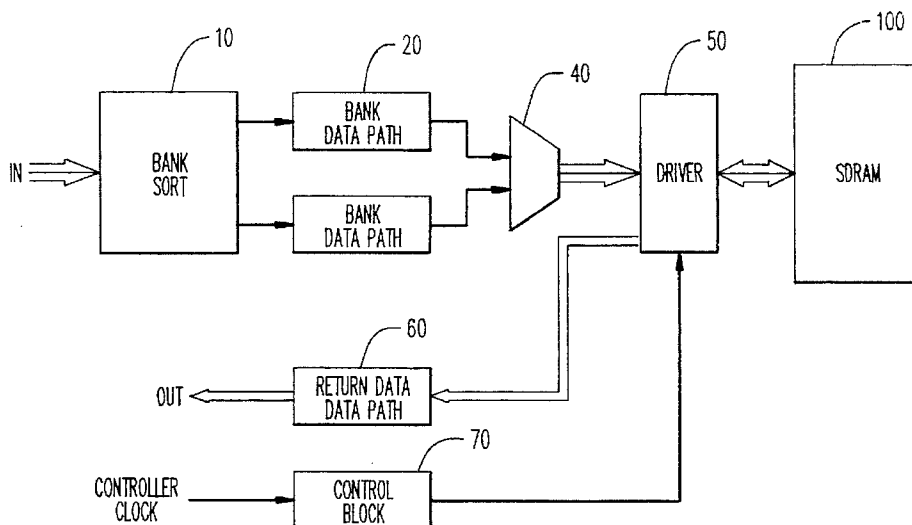
A controller for a synchronous DRAM is provided for maximizing throughput of memory requests to the synchronous DRAM. The controller maintains the spacing between the commands to conform with the specifications for the synchronous DRAMs while preventing gaps from occurring in the data slots to the synchronous DRAM. Furthermore, the controller allows memory requests and commands to be issued out of order so that the throughput may be maximized by overlapping required operations which do not specifically involve data transfer. To achieve this maximized throughput, memory requests are tagged for indicating a sending order. Thereafter, the memory requests may be arbitrated when conflicting memory requests are queued and this arbitration process is then decoded for simultaneously updating scheduling constraints. The memory requests may be further qualified based on the scheduling constraints and a command stack of memory request is then developed for modifying update queues. The controller also functions by receiving a controller clock signal and generating an SDRAM clock signal by dividing this controller clock signal.

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20 Claims, 6 Drawing Sheets



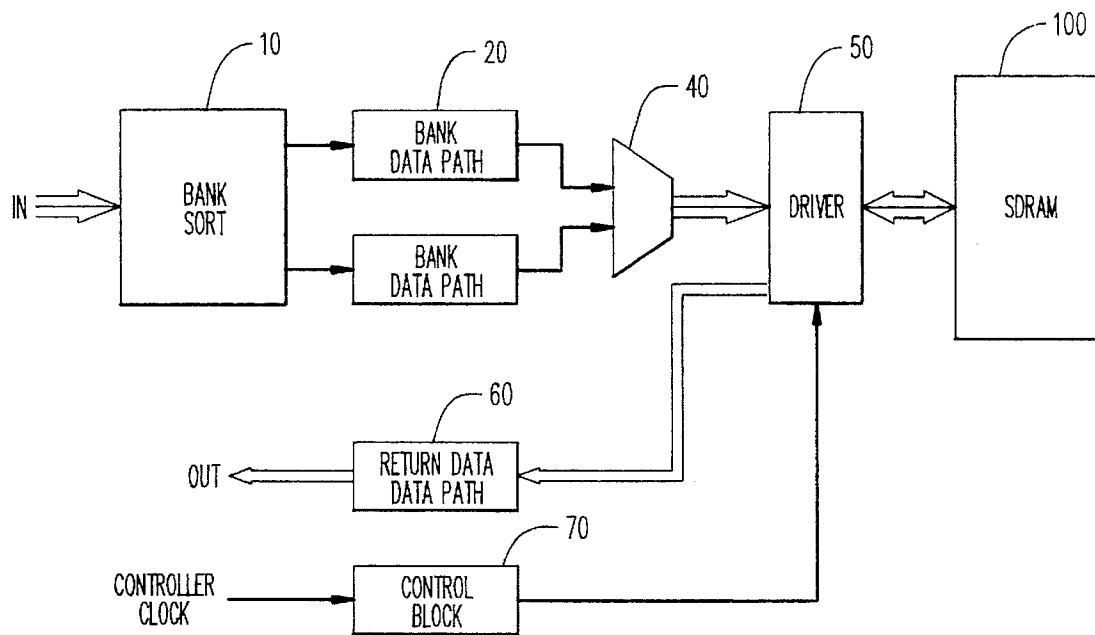


FIG. 1

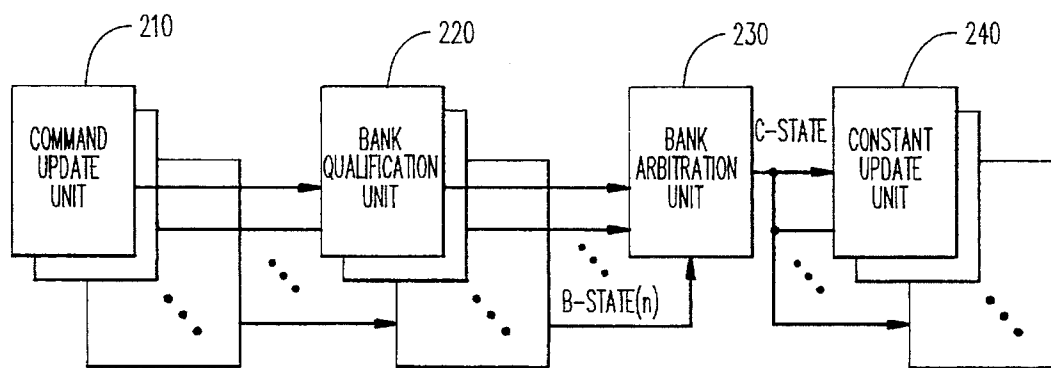


FIG. 2

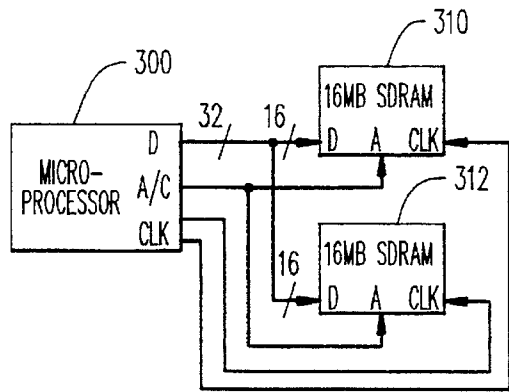


FIG. 3(a)

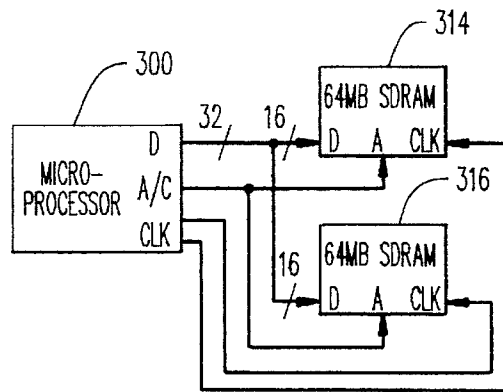


FIG. 3(b)

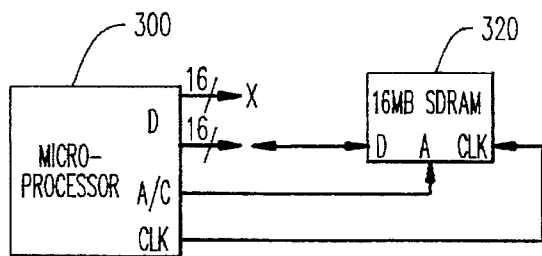


FIG. 3(c)

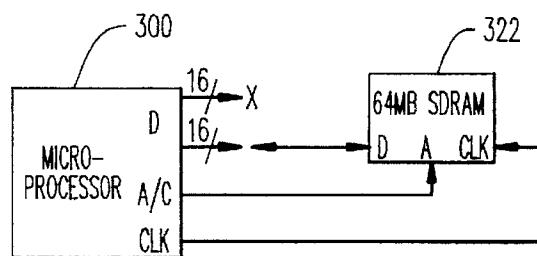


FIG. 3(d)

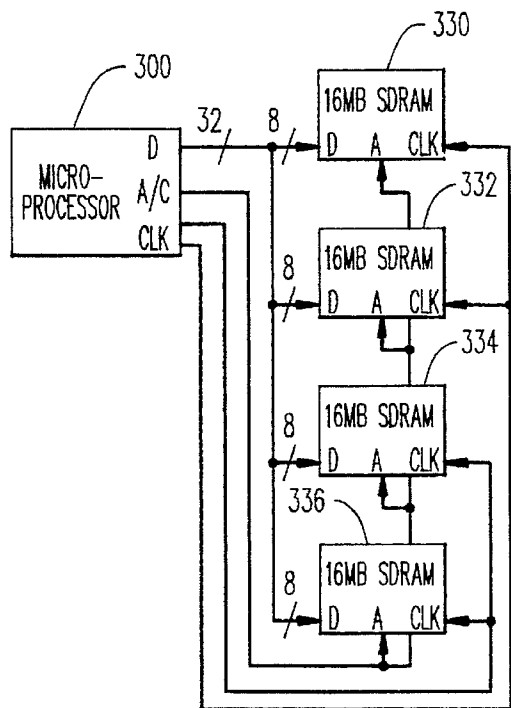


FIG. 3(e)

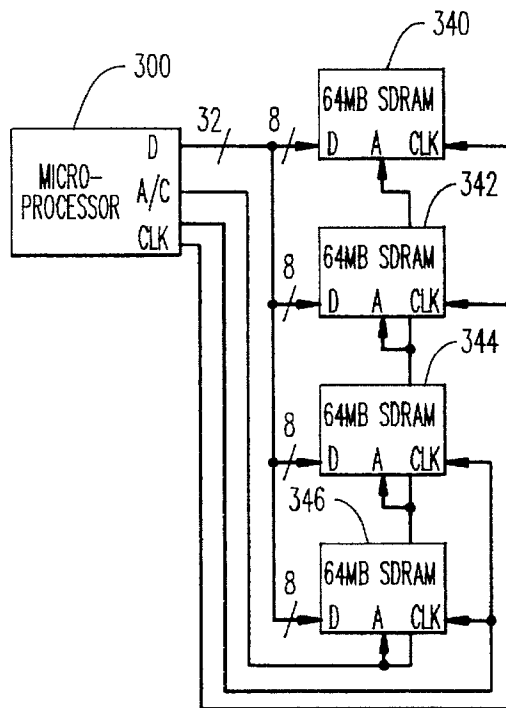


FIG. 3(f)

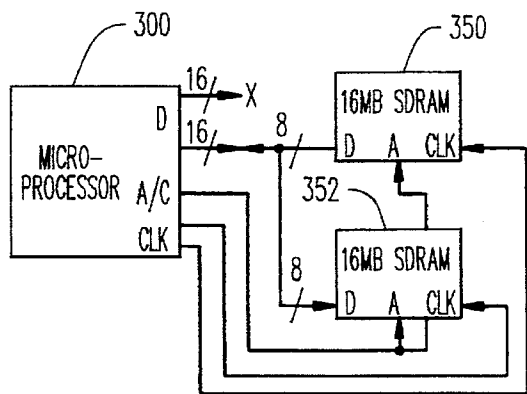


FIG. 3(g)

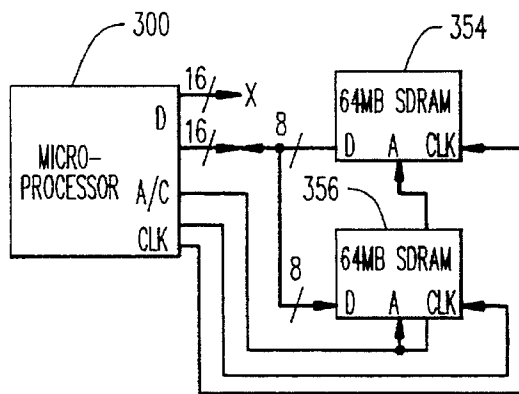


FIG. 3(h)

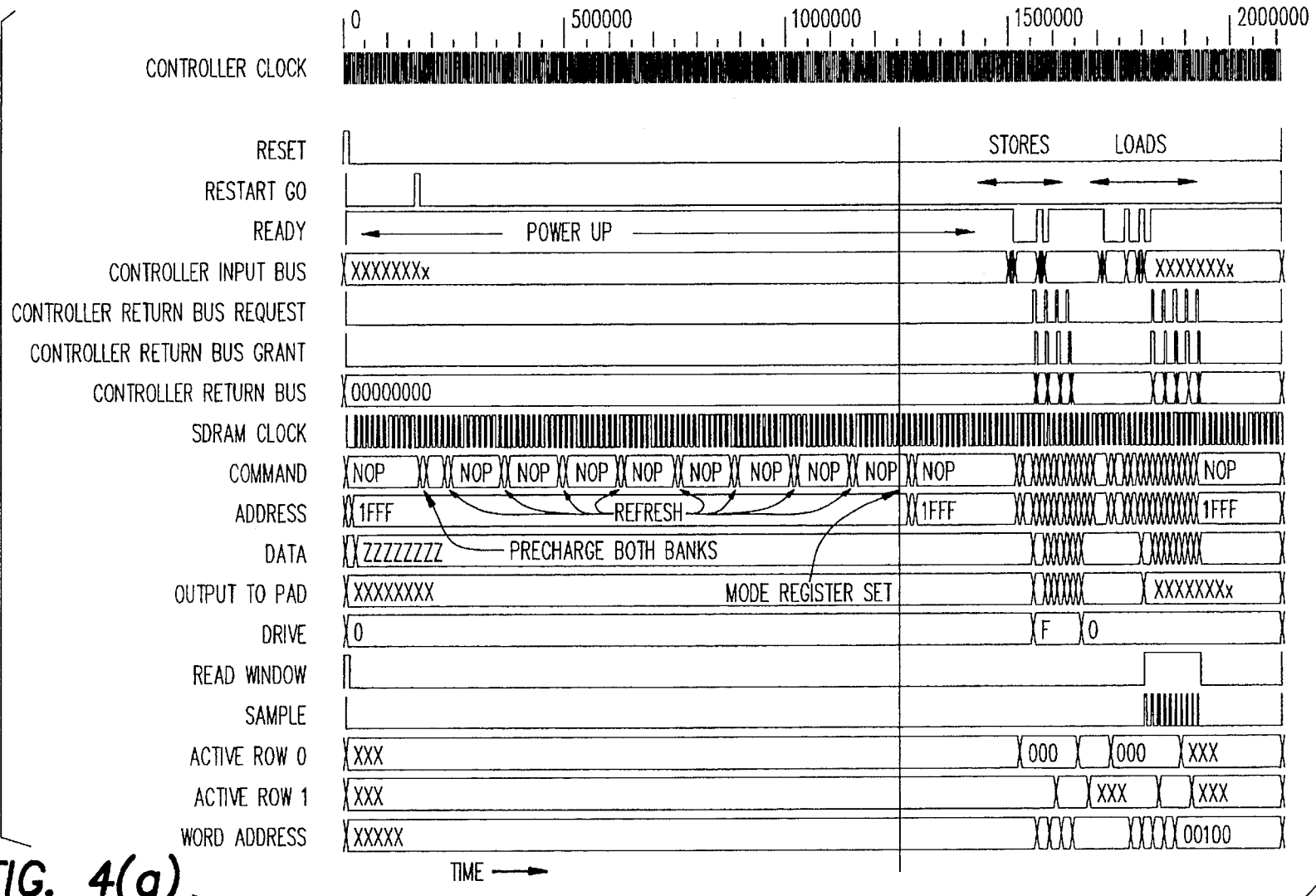


FIG. 4(a)

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