

[54] SEMICONDUCTOR MEMORY DEVICE HAVING A SLEEP MODE 5,262,998 11/1993 Mnich et al. 365/227
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[57] ABSTRACT

The present invention provides a computer memory device having a sleep mode characterized by extremely low current consumption and relatively large turn on delay. The invention includes circuitry for disabling current sinking elements internal to said device in response to a sleep signal. In one embodiment, the invention includes circuitry for disconnecting the bit lines and memory cell loads of a nonvolatile static random access memory (nvSRAM) array from a source of power in response to a sleep signal. This embodiment is capable of first transferring the data stored in a volatile portion of the array to a nonvolatile portion of the array before entering sleep mode to prevent loss of the data.

[21] Appl. No.: 413,360

[22] Filed: Mar. 30, 1995

[51] Int. Cl.⁶ C11C 7/00

[52] U.S. Cl. 365/227; 365/229

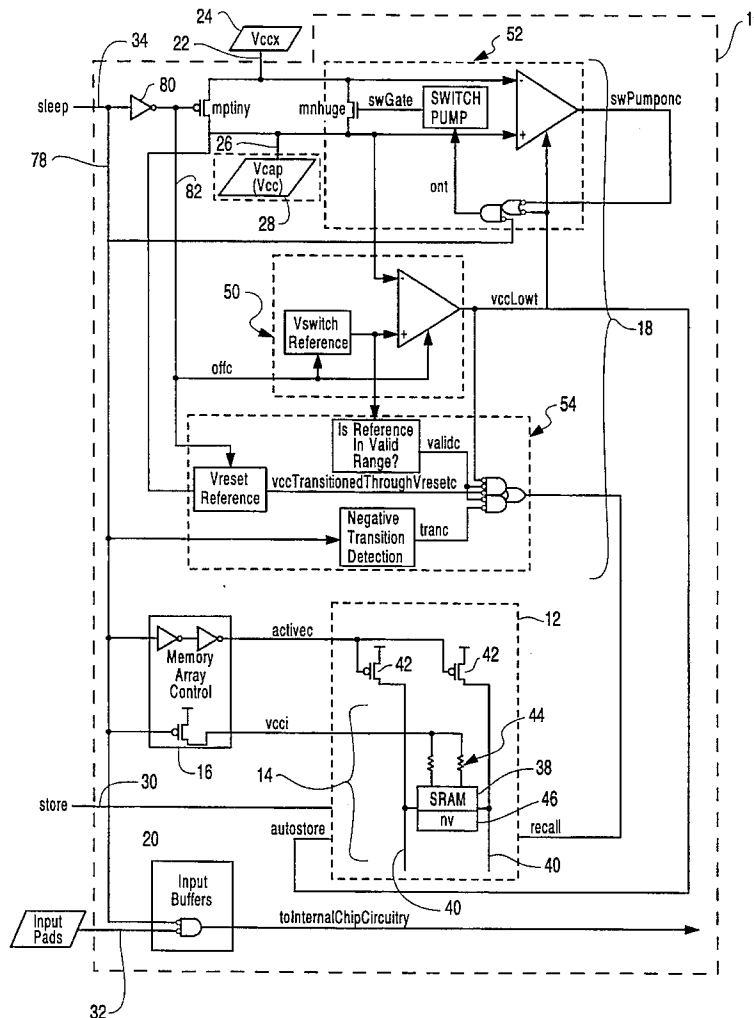
[58] Field of Search 365/226, 227, 365/228, 229

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30 Claims, 4 Drawing Sheets



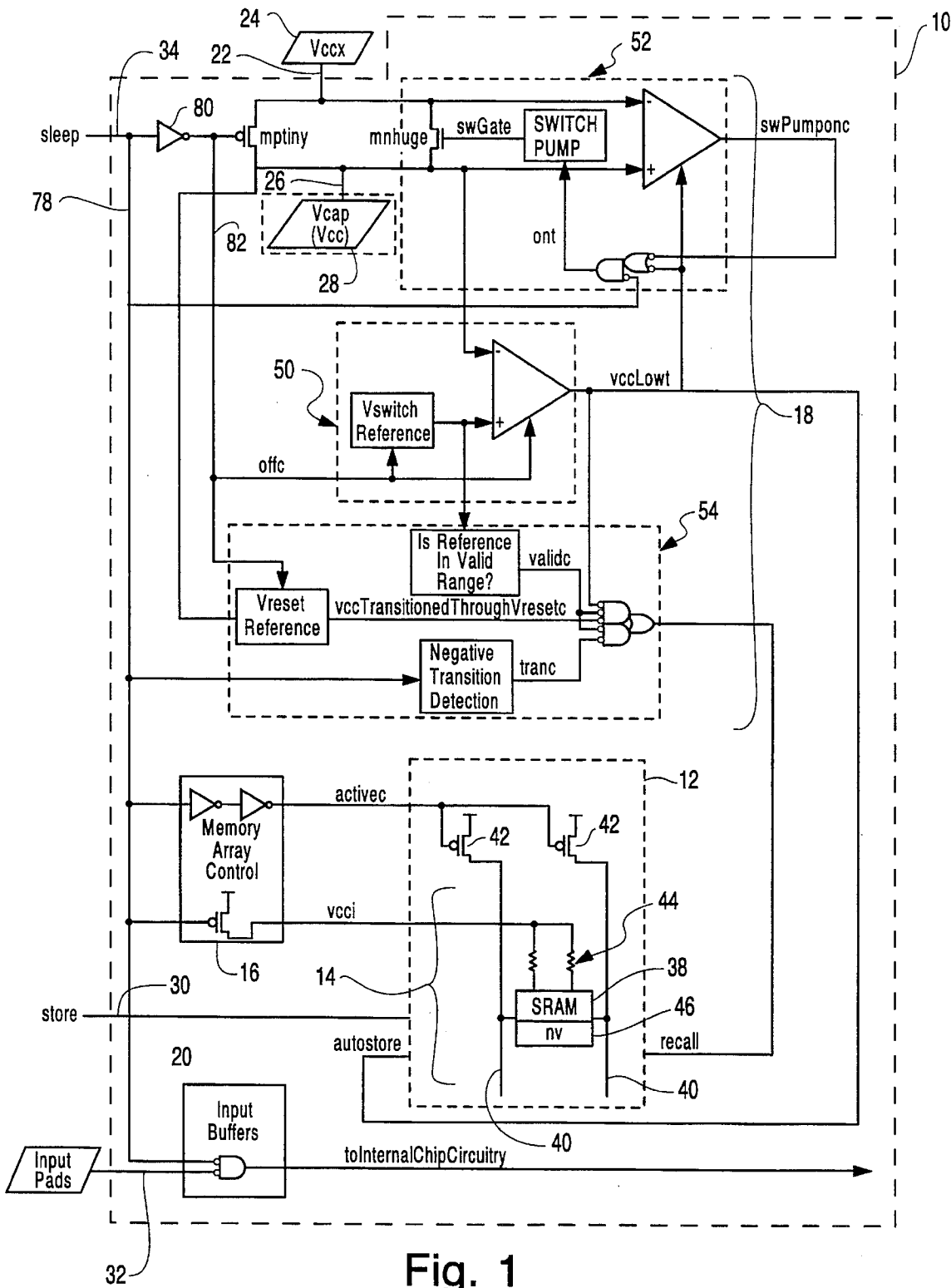


Fig. 1

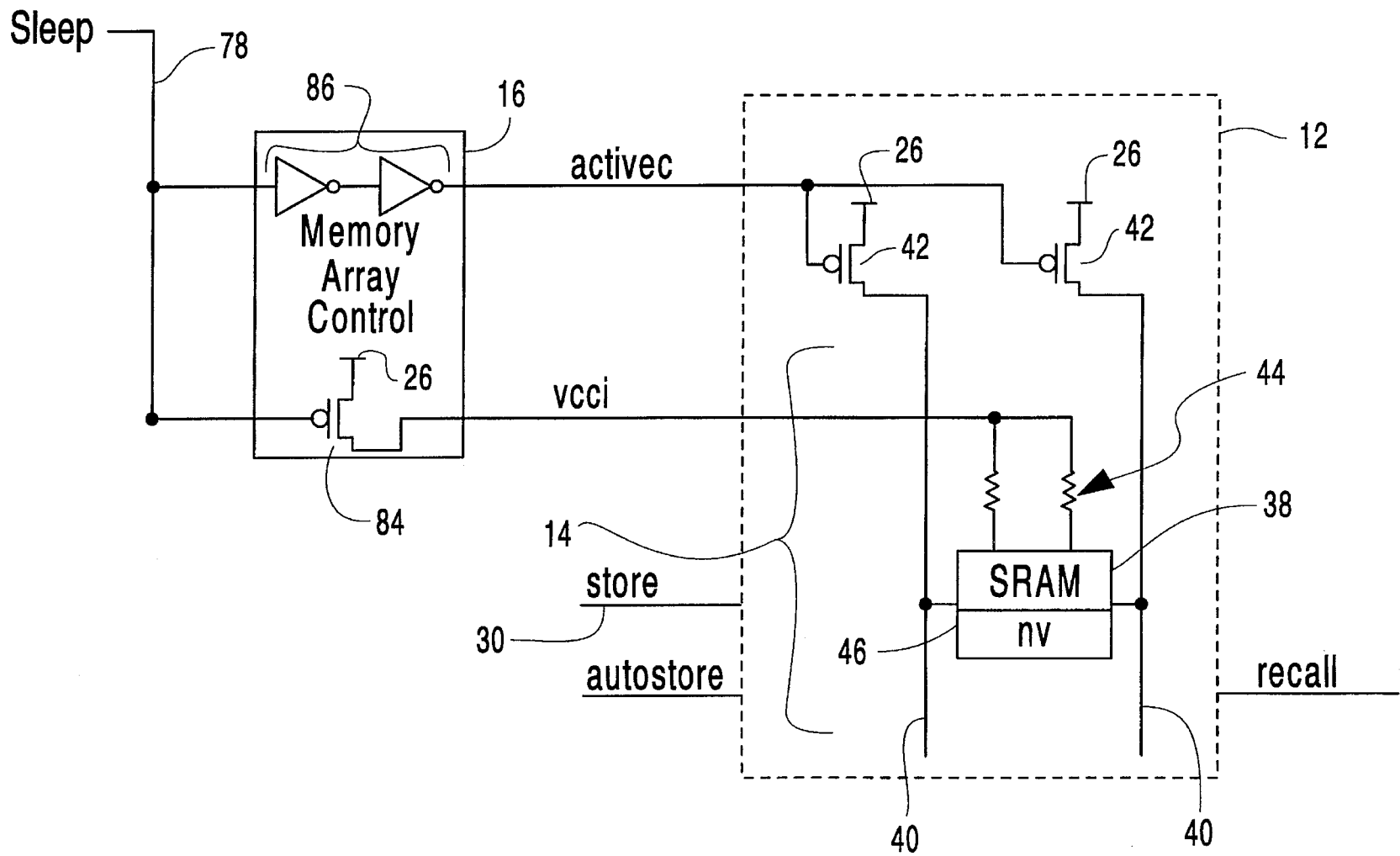


Fig. 2

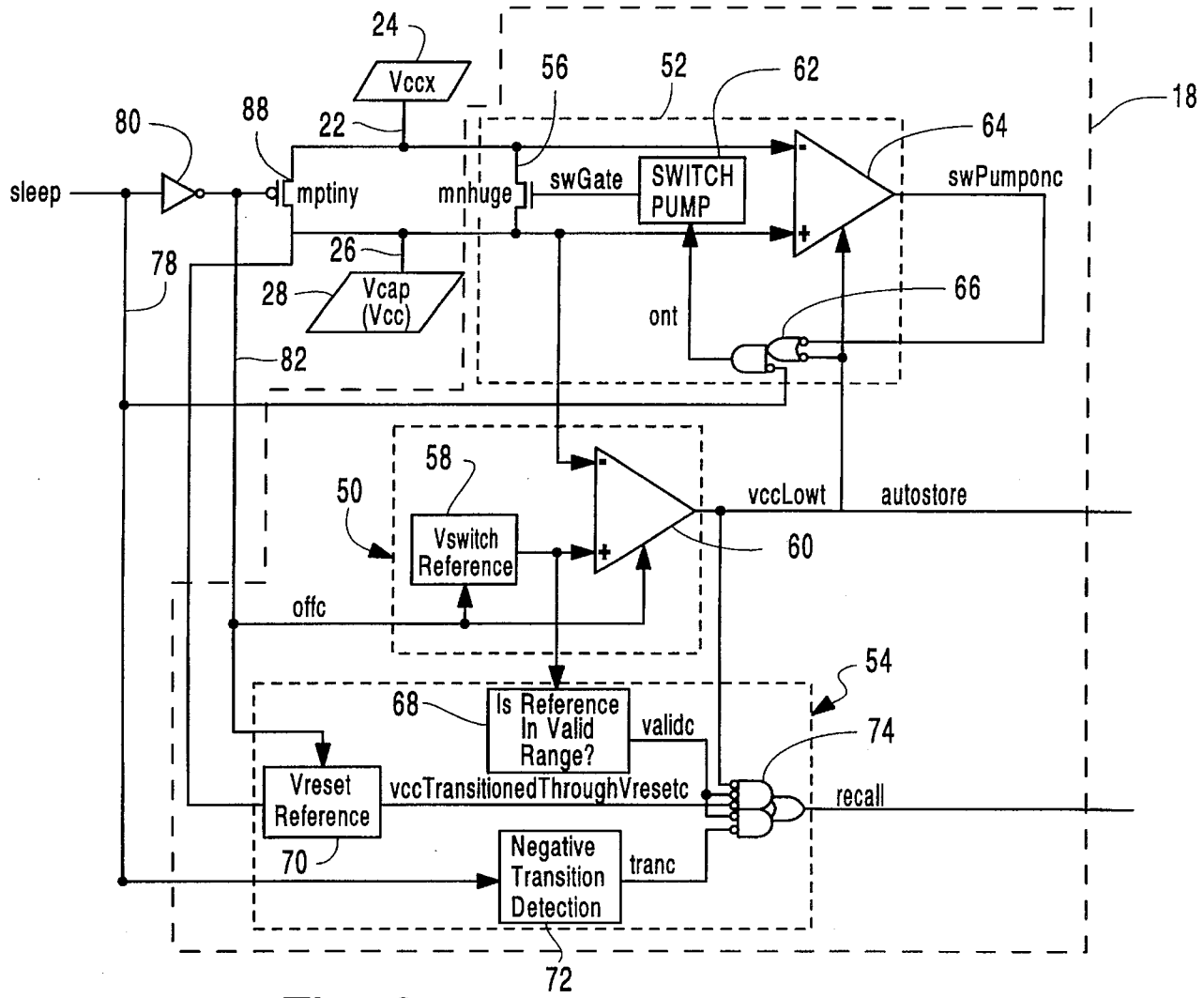


Fig. 3

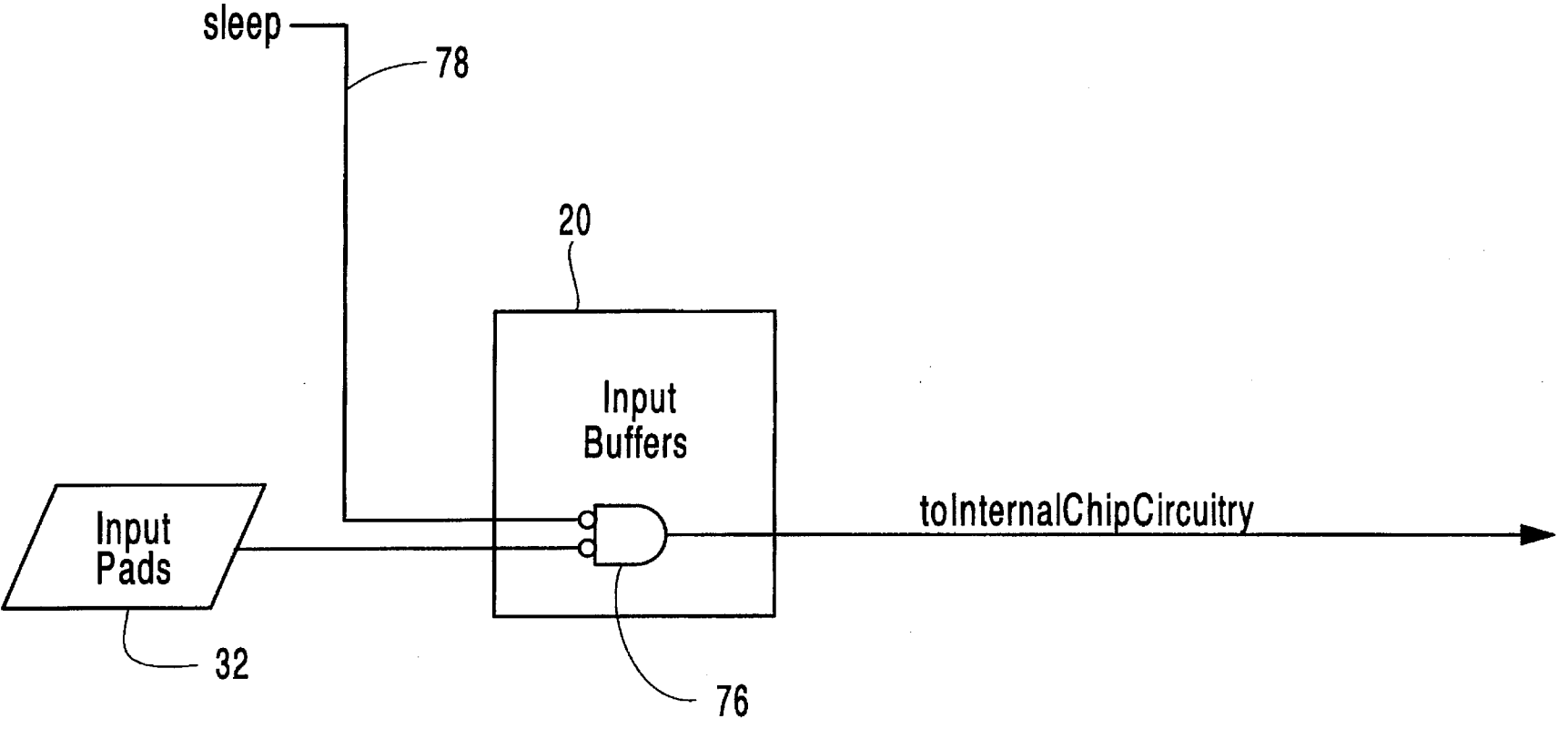


Fig. 4

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