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Shearon et al.

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(54) **INTEGRATED CIRCUIT FOR GENERATING A PLURALITY OF DIRECT CURRENT (DC) OUTPUT VOLTAGES**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 559 days.

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(65) **Prior Publication Data**

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Related U.S. Application Data

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(51) **Int. Cl.**

H02M 3/158 (2006.01)

(52) **U.S. Cl.** **323/266; 323/267; 323/901**

(58) **Field of Classification Search** **307/82, 307/29, 77, 65; 363/65, 49, 21.01, 267, 901, 363/266, 271**

See application file for complete search history.

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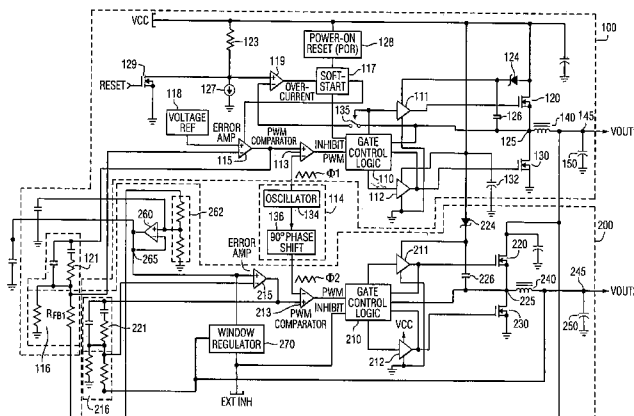
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(57) **ABSTRACT**

A cascaded DC-DC converter architecture has an upstream converter stage and a downstream converter stage, which derives its input voltage from the upstream stage. Cascading the two converter stages enables functionality of control and monitoring (including soft start and overcurrent detection) circuitry of the upstream stage to be used for the downstream stage, to reduce chip area, cost, and complexity. A voltage window regulator in the downstream converter ensures that, during shutdown, its output voltage will be maintained within a prescribed window of its regulated output voltage, so that no soft start delay is needed when the second converter stage is turned back on.

9 Claims, 3 Drawing Sheets



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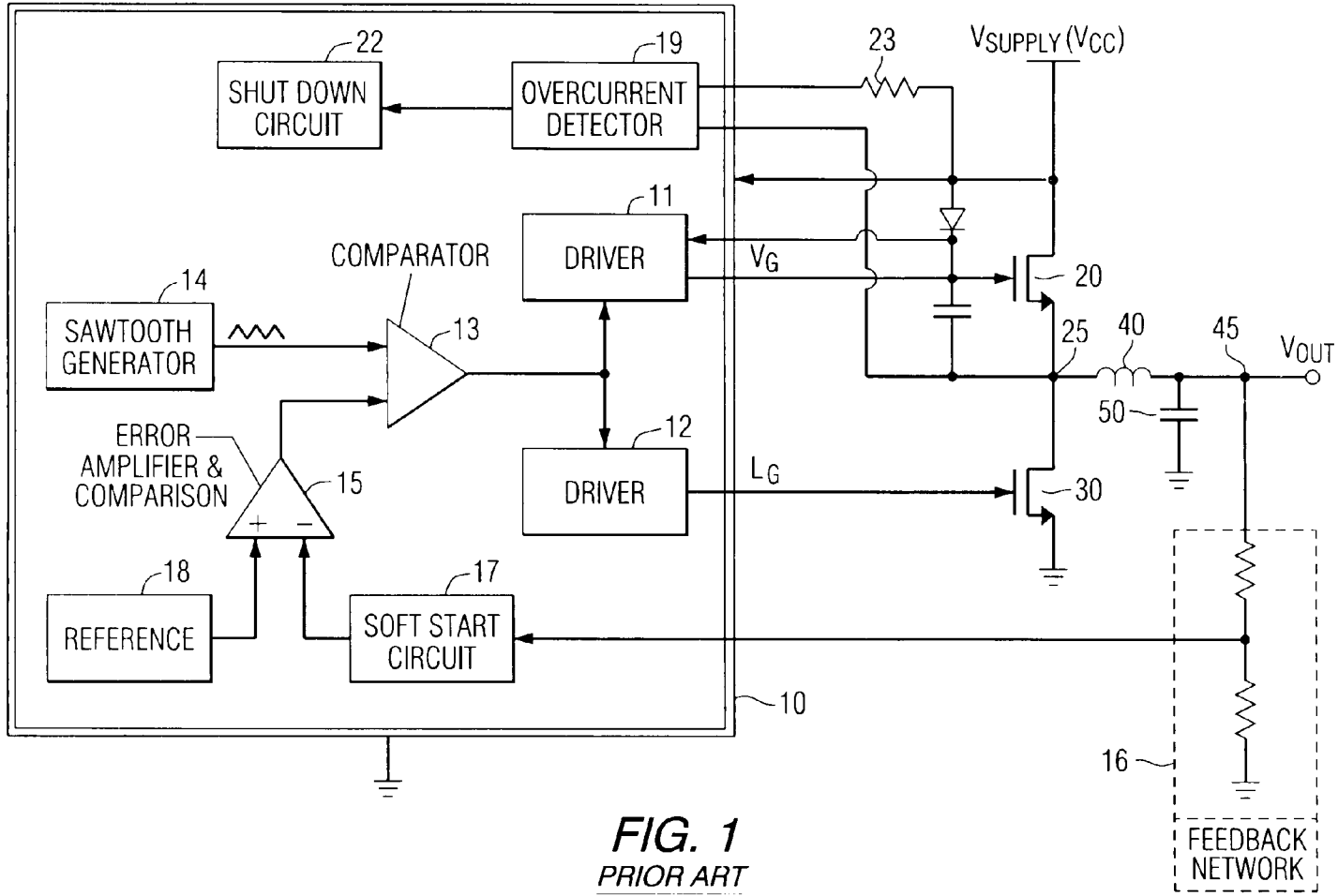


FIG. 1
PRIOR ART

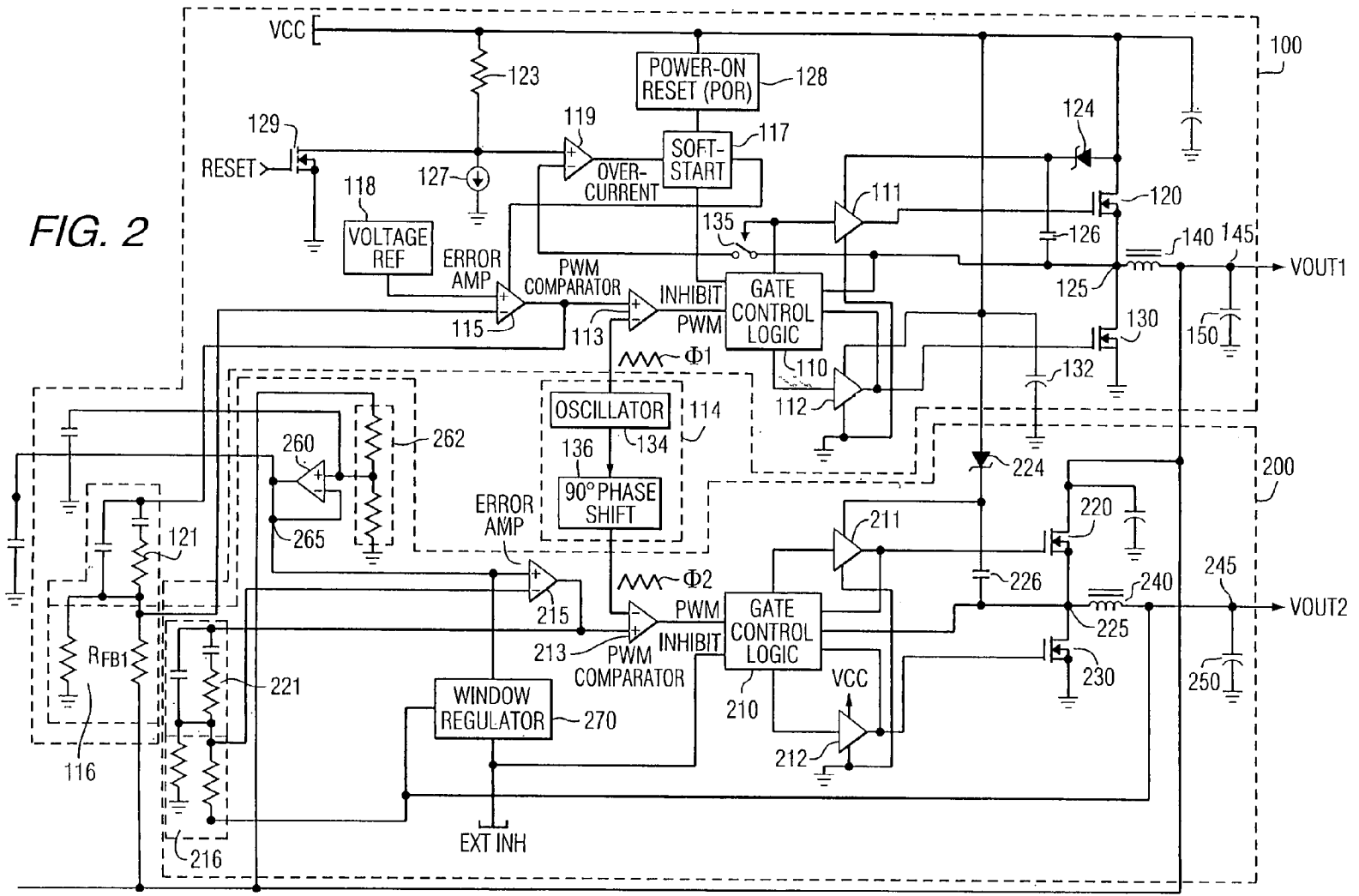


FIG. 2

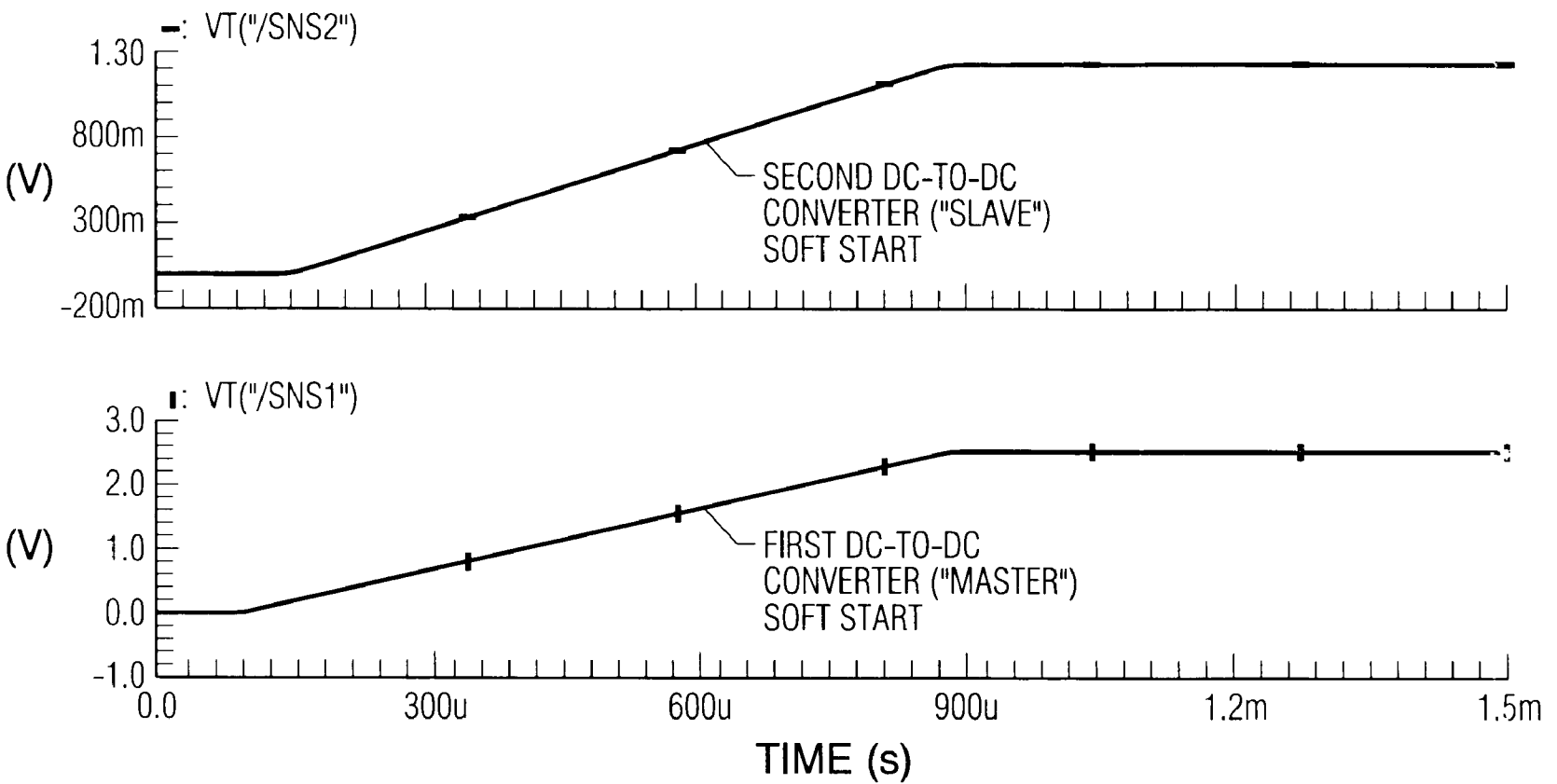


FIG. 3

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