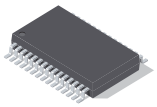


SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

FEATURES

- Wide Input Voltage Range: 4.5-V to 28-V
- Selectable Dual and DDR Modes
- Selectable Fixed Frequency Voltage Mode
- Integrated Selectable Output Discharge
- Advanced Power Good Logic Monitors both Channels
- Selectable Autoskip Mode
- Integrated Boot Strap Diodes
- 180° Phase Shift Between Channels
- Integrated 5-V, 60-mA Regulator
- Input Feedforward Control
- 1% Internal 0.85-V Reference
- $R_{DS(on)}$ Overcurrent Detection (4200 ppm/°C)
- Integrated OVP, UVP and Power Good Timers
- 30-pin TSSOP Package

APPLICATIONS

- Notebook Computers System Bus and I/O
- DDR I or DDR II Termination

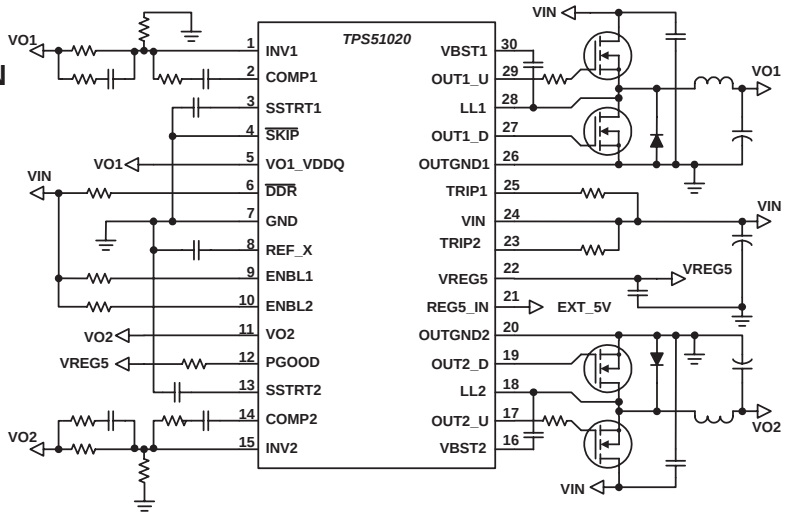
DESCRIPTION

The TPS51020 is a multi-function dual-synchronous step-down controller for notebook system power. The part is specifically designed for high performance, high efficiency applications where the loss associated with a current sense resistor is unacceptable. The TPS51020 utilizes feed forward voltage mode control to attain high efficiency without sacrificing line response. Efficiency at light load conditions can be maintained high as well by incorporating autoskip operation. A selectable, Suspend to RAM (STR) supported, DDR option provides a one chip solution for all switching applications from 5-V/3.3-V supply to a complete DDR termination solution.

ORDERING INFORMATION

TA	PLASTIC TSSOP (DBT)
−40°C to 85°C	TPS51020DBT
	TPS51020DBTR (T&R)

SIMPLIFIED APPLICATION DIAGRAM



UDG−03144

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted. All voltage values are with respect to the network ground terminal unless otherwise noted. (1)

		TPS51020	UNIT
Input voltage range	VBST1, VBST2	−0.3 to 35	V
	VBST1, VBST2 (with respect to LL)	−0.3 to 7	
	VIN, TRIP1, TRIP2, ENBL1, ENBL2, $\overline{DDR}$	−0.3 to 30	
	$\overline{SKIP}$, INV1, INV2	−0.3 to 7	
Ouput voltage range	OUT1_U, OUT2_U	−1 to 35	
	OUT1_U, OUT2_U (with respect to LL)	−0.3 to 7	
	LL1, LL2	−1 to 30	
	REF_X	−0.3 to 15	
	PGOOD, VO1_VDDQ, VO2, OUT1_D, OUT2_D, COMP1, COMP2, VREG5, SSTRT1, SSTRT2	−0.3 to 7	
	OUTGND1, OUTGND2	−0.3 to 0.3	
Output current range	VREG5	70	mA
	REF_X	7	
Operating free-air temperature range, T_A		−40 to 85	°C
Storage temperature range, T_{stg}		−55 to 150	
Junction temperature range, T_J		−40 to 125	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

RECOMMENDED OPERATING CONDITIONS

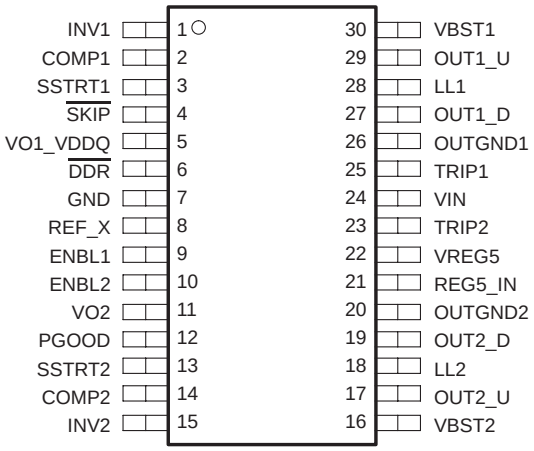
		MIN	TYP	MAX	UNIT
Supply voltage, VIN		4.5		28	V
Supply voltage, VBST1, VBST2		4.5		33	
I/O Voltage	ENBL1, ENBL2, $\overline{DDR}$, TRIP1, TRIP2	−0.1		28	
	OUT1_U, OUT2_U	−0.8		33	
	OUT1_U, OUT2_U (with respect to LL)	−0.1		5.5	
	LL1, LL2	−0.8		28	
	REF_X	−0.1		12	
	SSTRT1, SSTRT2, COMP1, COMP2	−0.1		5.5	
	$\overline{SKIP}$, INV1, INV2	−0.1		5.5	
	PGOOD VO1_VDDQ, VO2	−0.1		5.5	
	OUT1_D, OUT2_D, VREG5	−0.1		5.5	
Source current	VREG5			60	mA
	REF_X			5	
Operating free-air temperature, T_A		−40		85	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
30-pin DBT	874 mW	7.0 mW/°C	454 mW

TSSOP (0.5 mm)
DBT PACKAGE
(TOP VIEW)



ELECTRICAL CHARACTERISTICS

T_A = −40°C to 85°C, 4.5 V < V_{IN} < 20 V, C_{VIN} = 0.1 µF, C_{VREG5} = 2.2 µF, C_{REF_X} = 0.01 µF, PGOOD = 0.2 V, ENBLx = $\overline{DDR}$ = VIN, INVx = COMPx, RSSTRTx = OPEN, TRIP1 = TRIP2 = VIN, LLx = GND, VBSTx = LLx+5, $C_{(OUTx\_U,\ OUTx\_D)}$=1 nF, REG5_IN = 0V, GND = OUTGNDx = 0 V, VO1_VDDQ = VO2 = 0 V (unless otherwise stated)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENTS							
I_{VIN}	V_{IN} supply current	REG5V_IN = OPEN, OSC = OFF	TRIPx = VIN,		1.4	2.2	mA
$I_{VIN(STBY)}$	V_{IN} standby current	ENBLx = 0 V, REG5V_IN = OPEN,	$\overline{DDR}$ = VIN, OSC = OFF		350	550	µA
$I_{VIN(SHDN)}$	V_{IN} shutdown current	ENBLx = $\overline{DDR}$ = 0 V, REG5V_IN = OPEN			0.05	1.00	
$I_{VIN(REG5)}$	V_{IN} supply current, REG5_IN as 5-V input current	REG5V_IN = 5 V,	OSC = OFF		200	500	
I_{REG5}	REG5_IN input supply current	REG5V_IN = 5 V,	OSC = OFF		1.0	1.7	mA
I_{VBSTx}	VBST supply current	ENBLx = $\overline{DDR}$ = VIN			0.05	1.00	µA
I_{VBSTx}	VBST shutdown current	ENBLx = $\overline{DDR}$ = 0 V			0.05	1.00	
VREG5 INTERNAL REGULATOR							
V_{VREG5}	VREG5 voltage	I_{OUT} = 0 A		4.8	5.0	5.2	V
V_{LD5}	Load regulation	0 mA ≤ I_{OUT} ≤ 50 mA,	V_{IN} = 12 V		0.6%	2.5%	
V_{LN5}	Line regulation	I_{OUT} = 20 mA,	7 V≤V_{IN} ≤ 28 V		0.4%	2.0%	
V_{THL}	UVLO threshold voltage	High to low		3.45	3.65	3.85	V
$V_{HYS(UV)}$	UVLO hysteresis			100	200	300	mV
$V_{TH(SW)}$	Switchover voltage	REG_IN voltage		4.2	4.5	4.8	V
$V_{HYS(SW)}$	Switchover hysteresis			50		250	mV

ELECTRICAL CHARACTERISTICS (continued)

T_A = −40°C to 85°C, 4.5 V < V_{IN} < 20 V, C_{VIN} = 0.1 µF, C_{VREG5} = 2.2 µF, C_{REF_X} = 0.01 µF, PGOOD = 0.2 V, ENBLx = $\overline{DDR}$ = VIN, INVx = COMPx, RSSTRTx = OPEN, TRIP1 = TRIP2 = VIN, LLx = GND, VBSTx = LLx+5, $C_{(OUTx\_U, OUTx\_D)}$=1 nF, REG5_IN = 0V, GND = OUTGNDx = 0 V, VO1_VDDQ = VO2 = 0 V (unless otherwise stated)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REF_X REFERENCE VOLTAGE							
V_{REF10}	10-V reference voltage	V_{IN} = 14 V,	I_{OUT} = 0 A	8.5	10.0	11.0	V
V_{LD10}	Load regulation	0 mA ≤ I_{OUT} ≤ 2 mA,	V_{IN} = 18 V		-12%	-20%	
V_{LN10}	Line regulation	I_{OUT} = 100 µA,	14 V≤V_{IN} ≤28 V			5%	
V_{REFVTT}	VTT reference voltage	$\overline{DDR}$ = 0 V wrt VO1_VDDQ input divided by 2 V_{VO1} = 2.5 V				1.5%	
V_{REFVTT}	VTT reference load regulation	0 mA ≤ I_O ≤ 3 mA				0.75%	
POWERGOOD COMPARATORS							
$V_{THDUAL(PG)}$	PGOOD threshold (dual mode)	Undervoltage PGOOD		765	786	808	mV
		Overvoltage PGOOD		892	920	945	
$V_{THDDR(PG)}$	PGOOD threshold (DDR)	Undervoltage PGOOD, VO1_VDDQ = 2.5 V		1.12	1.14	1.16	V
		Overvoltage PGOOD, VO1_VDDQ = 2.5 V		1.28	1.31	1.33	
$T_{PG(del)}$	PGOOD delay time	INVx > undervoltage PGOOD, Delay time from SSTRTx > 1.5 V to PGOOD going high			2048		clks
DIGITAL CONTROL INPUTS							
V_{IH}	High-level input voltage, logic	$\overline{DDR}$, ENBL1, ENBL2, $\overline{SKIP}$		2.2			V
V_{IL}	Low-level input voltage, logic	$\overline{DDR}$, ENBL1, ENBL2, $\overline{SKIP}$				0.3	
I_{INLEAK}	Logic input leakage current	$\overline{DDR}$, ENBL1, ENBL2, $\overline{SKIP}$= 5 V				|1.0|	µA
VO1_VDDQ and VO2							
R_{VOUT}	VOx sink impedance	V_{VOUTx} = 0.5 V,	fault engaged		6	10	Ω
V_{VOUTOK}	VOx low restart voltage	Fault condition removed, restart		0.25	0.32	0.40	V
$V_{VO2LEAK}$	VOx input leakage current	$\overline{DDR}$= VIN,	VOx = 5 V			|1.0|	µA
R_{VOUT}	VO1_VDDQ input impedance	$\overline{DDR}$= 0			1.5		MΩ
UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
$V_{OVPDUAL}$	OVP trip output threshold (dual)	Sensed at INVx		945	970	1010	mV
V_{OVPDDR}	OVP trip output threshold (DDR)	VO1_VDDQ = 2.5 V		1.31	1.36	1.41	V
$T_{OVP(del)}$	OVP propagation delay time(1)				20		µs
$V_{UVPDUAL}$	UVP trip output threshold (dual)	Sensed at INVx		510	553	595	mV
V_{UVPDDR}	UVP trip output threshold (DDR)	VO1_VDDQ = 2.5 V		750	813	875	
$T_{UVP(del)}$	UVP propagation delay time				4096		clks
OVERCURRENT and INPUT VOLTAGE UVLO PROTECTION							
$I_{TRIPSNK}$	TRIPx sink current	V_{TRIPx} = V_{IN} − 100 mV,	T_A = 25°C	11	13	15	µA
$I_{TRIPSRC}$	TRIPx source current	V_{TRIPx} = 100 mV,	T_A = 25°C	10	13	16	
TC_{ITRIP}	TRIP current temperature coeficient(1)	T_A = 25°C			4200		ppm/°C
V_{OCPHI}	High-level OCP comparator offset voltage(1)				0	|3.0|	mV
V_{OCPLO}	Low-level OCP comparator offset voltage(1)				0	|5.0|	
$V_{VINUVLO}$	VIN UVLO trip threshold	REF5V_IN = 4.8 V		3.7	3.9	4.1	V
V_{VINHYS}	VIN UVLO trip hysteresis			100	200	300	mV

ELECTRICAL CHARACTERISTICS (continued)

T_A = −40°C to 85°C, 4.5 V < V_{IN} < 20 V, C_{VIN} = 0.1 µF, C_{VREG5} = 2.2 µF, C_{REF_X} = 0.01 µF, PGOOD = 0.2 V, ENBLx = $\overline{DDR}$ = VIN, INVx = COMPx, RSSTRTx = OPEN, TRIP1 = TRIP2 = VIN, LLx = GND, VBSTx = LLx+5, $C_{(OUTx\_U, OUTx\_D)}$=1 nF, REG5_IN = 0V, GND = OUTGNDx = 0 V, VO1_VDDQ = VO2 = 0 V (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
0.85-V REFERENCE CONTROL LOOP						
V_{REFCH1}	Error amplifier reference, channel 1 initial accuracy	Measure COMP1, COMP1= INV1, T_A = 25°C	0.84	0.85	0.86	V
V_{REFTC1}	Error amplifier reference, channel 1 change with accuracy			0.5%		
V_{REFLN1}	Error amplifier reference, channel 1 change with line			0.1%		
V_{CHMM}	Channel 2 to channel 1 voltage mismatch			0	|5.0|	mV
CONTROL LOOP: SKIP HYSTERSTIC COMPARATOR AND ZERO CURRENT COMPARATOR						
V_{LLHYS}	Skip hysteresis comparator hysteresis(1)		1	2	3	mV
V_{LLOFF}	Lload hysteresis comparator offset(1)			0	1	
V_{ZOFF}	Zero current comparator offset(1)			10	18	
T_{HLTOLL}	PWM skip delay time			8		clks
T_{HLTOHL}	Skip to PWM delay time			1		
CONTROL LOOP ERROR AMPLIFIER						
I_{EASRC}	COMPx source current		0.2	0.9		mA
I_{EASNK}	COMPx sink current		0.2	0.7		
F_{UGB}	Unity gain bandwidth(1)			2.5		MHz
A_{OL}	Open loop gain(1)			80		dB
CMR_{COMP}	COMPx voltage range(1)(6)		0.4		VREG5−3	V
$I_{INVLEAK}$	INVx input current				|0.5|	µA
CONTROL LOOP: DUTY CYCLE, VOLTAGE RAMP, CHANNEL PHASE AND PWM DELAY PATH						
DC_{MAX}	Maximum duty cycle	f_{OSC} = 270 kHz(3)	86%	88%		
		f_{OSC} = 360 kHz	84%	85%		
		f_{OSC} = 450 kHz(2)	80%	82%		
PH_{CH}	Channel to channel phase difference(5)	PWM phase reversal only		180		°
T_{MIN}	OUTX_U minimum pulse width(1)			100		ns
TIMERS: INTERNAL OSCILLATOR(4)						
$f_{OSC(hi)}$	Fast oscillator frequency initial accuracy(2)	R_{SSTRTx} = OPEN		450		kHz
$f_{OSC(lo)}$	Slow oscillator frequency initial accuracy	R_{SSTRTx} = 1MΩ or V_{SSTRT} = 3 V		270		
$f_{OSC(tc)}$	Oscillator frequency over line and temperature	Trimmed for 360 kHz	306	360	414	

(1) Ensured by design. Not production tested.
(2) Maximum 450-kHz frequency can be achieved when both channels are enabled.
(3) 270 kHz is the default frequency during start-up for both channels.
(4) See Table 1.
(5) See PWM detailed description

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