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(54) **APPARATUS AND METHOD FOR POWER MANAGEMENT OF MEMORY CIRCUITS BY A SYSTEM OR COMPONENT THEREOF**

ation No. 11/524,811, filed on Sep. 20, 2006, now Pat. No. 7,590,796, which is a continuation-in-part of application No. 11/461,439, filed on Jul. 31, 2006, now Pat. No. 7,580,312.

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(57) **ABSTRACT**

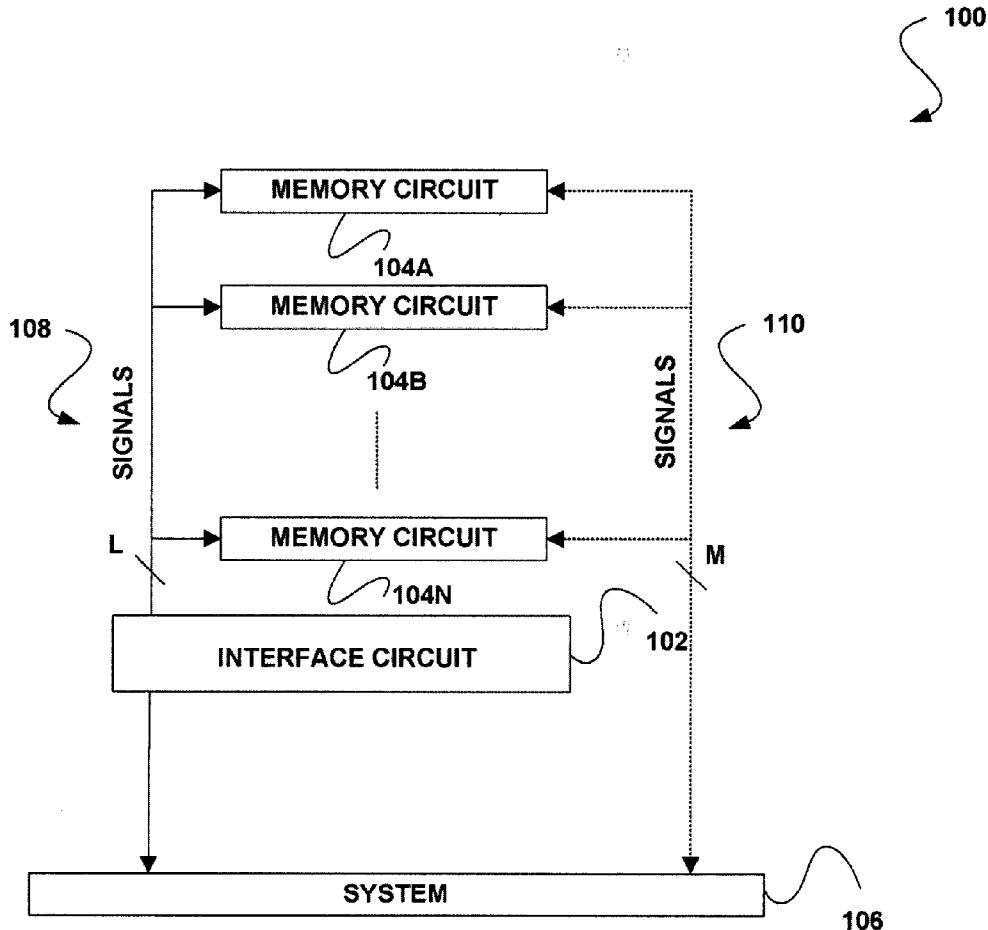
(21) Appl. No.: **12/816,756**

An apparatus and method are provided for communicating with a plurality of physical memory circuits. In use, at least one virtual memory circuit is simulated where at least one aspect (e.g. power-related aspect, etc.) of such virtual memory circuit(s) is different from at least one aspect of at least one of the physical memory circuits. Further, in various embodiments, such simulation may be carried out by a system (or component thereof), an interface circuit, etc.

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Related U.S. Application Data

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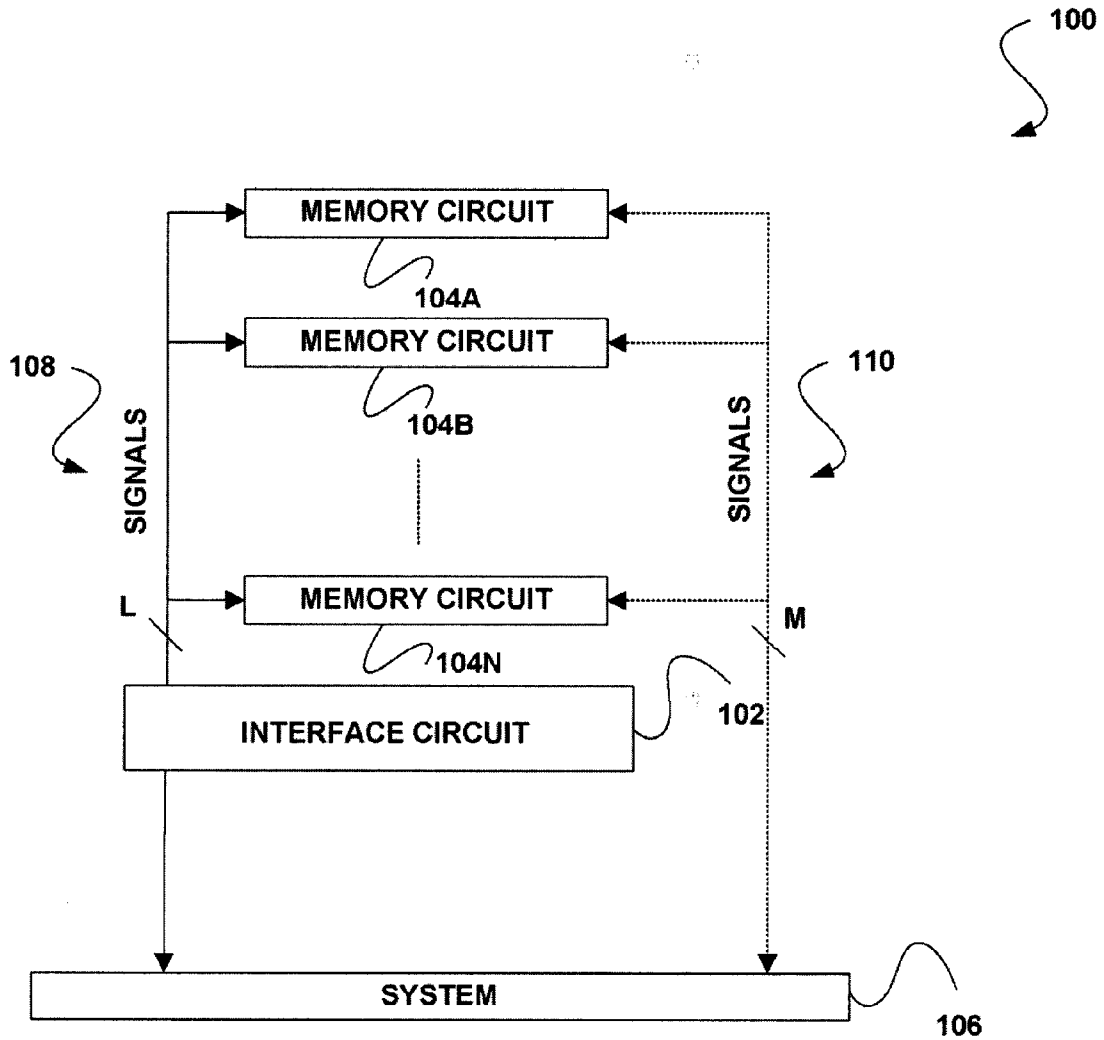


FIGURE 1

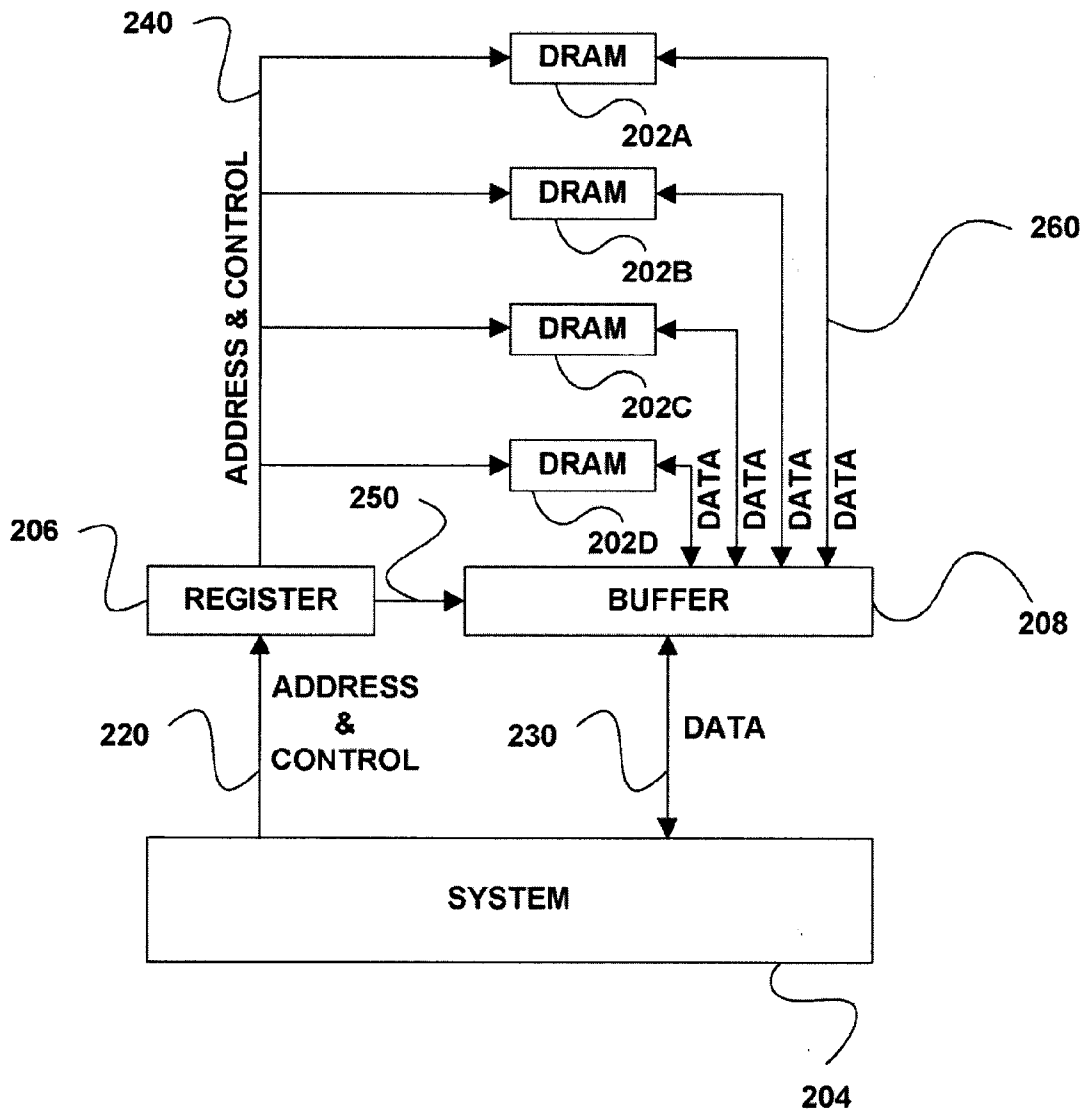


FIGURE 2

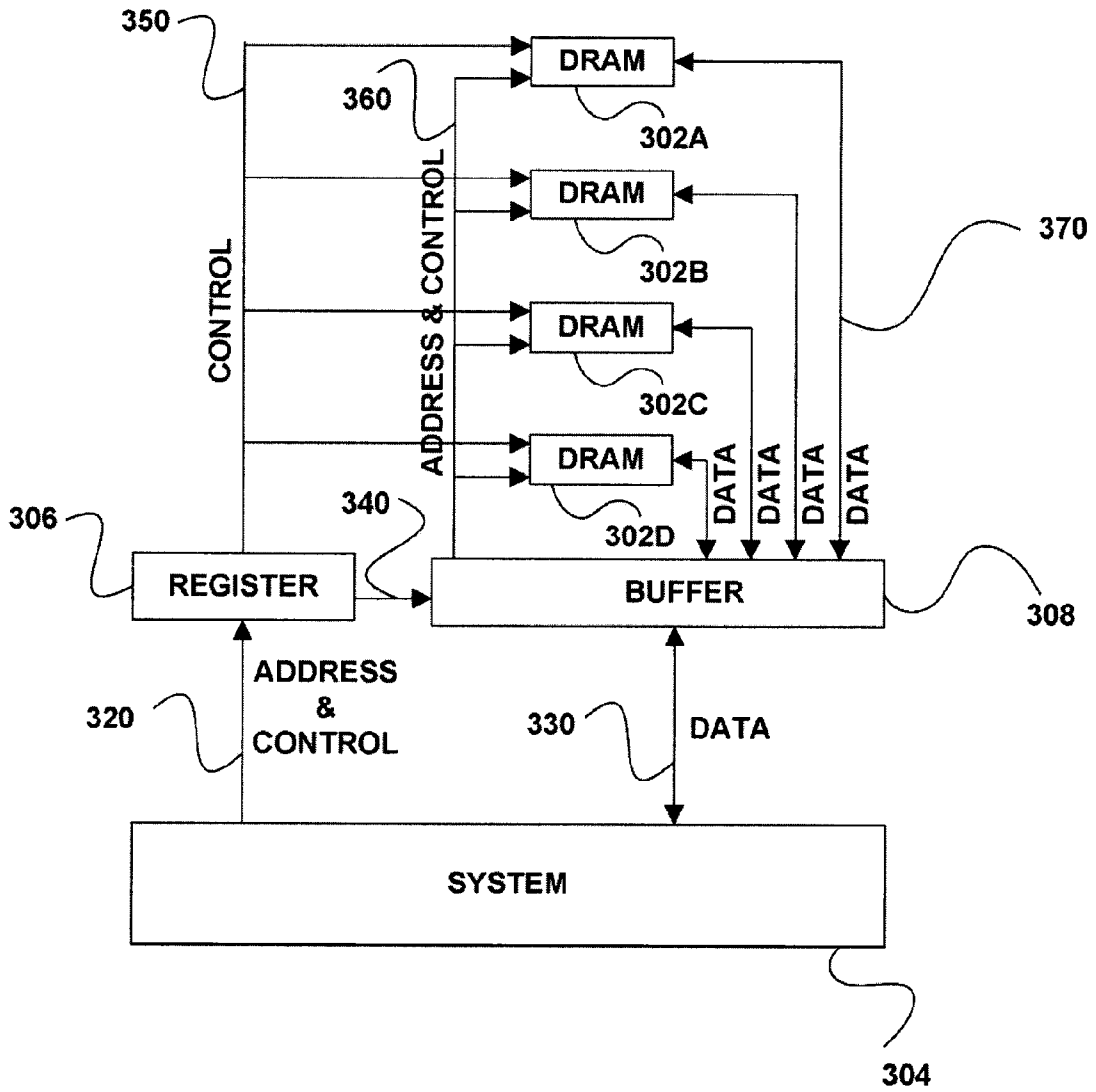


FIGURE 3

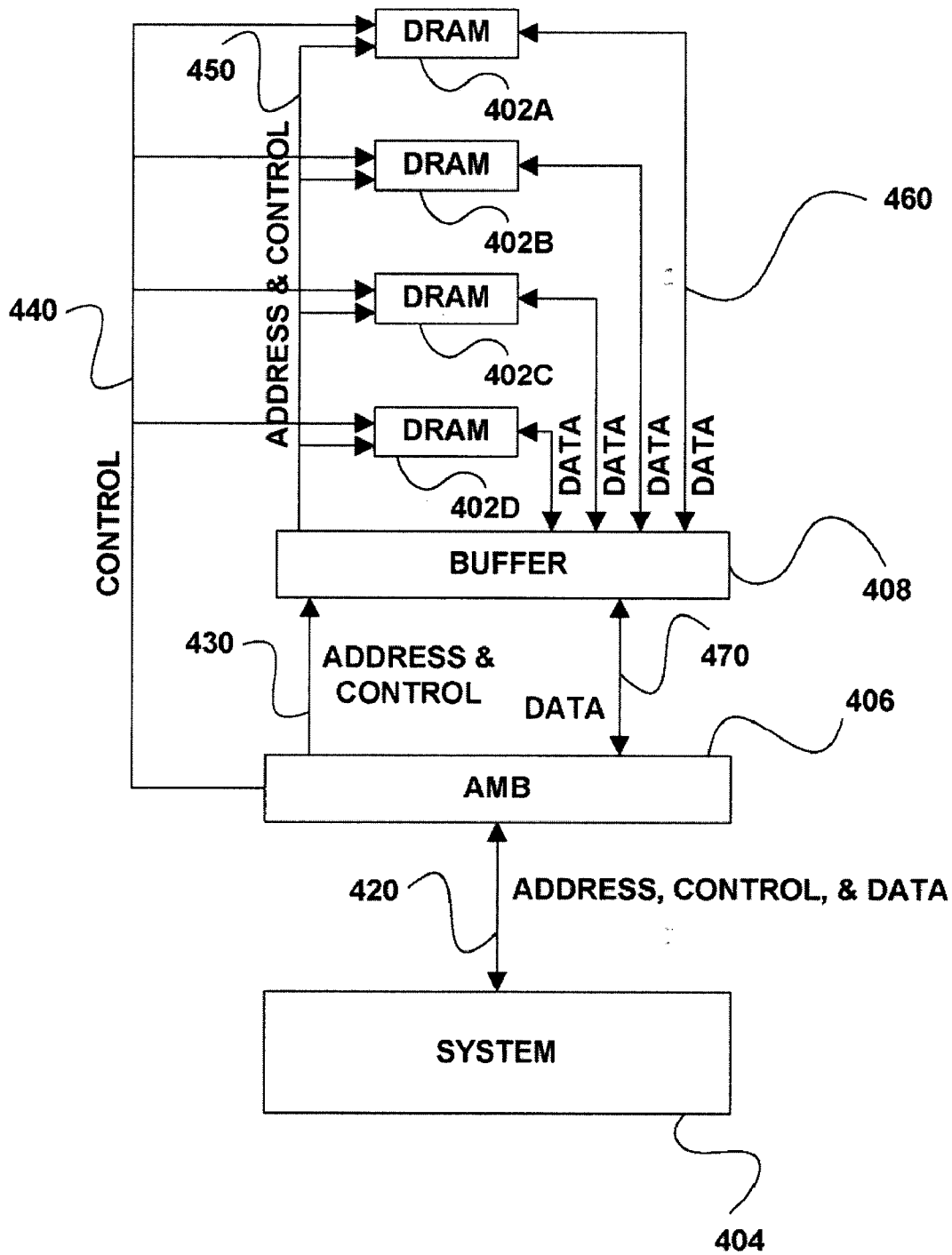


FIGURE 4

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