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(54) **APPARATUS AND METHOD FOR SWITCHING AN APPARATUS TO A POWER SAVING MODE**

(75) Inventors: **Edoardo Prete**, Munich (DE); **Hans-Peter Trost**, Munich (DE); **Anthony Sanders**, Haar (DE); **Dirk Scheideler**, Munich (DE); **Georg Braun**, Holzkirchen (DE); **Steve Wood**, Munich (DE); **Richard Johannes Luyken**, Munich (DE)

(73) Assignee: **Qimonda AG**, Munich (DE)

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(58) **Field of Classification Search** 713/300, 713/323, 320; 711/170, 106, 5, 167; 365/221
See application file for complete search history.

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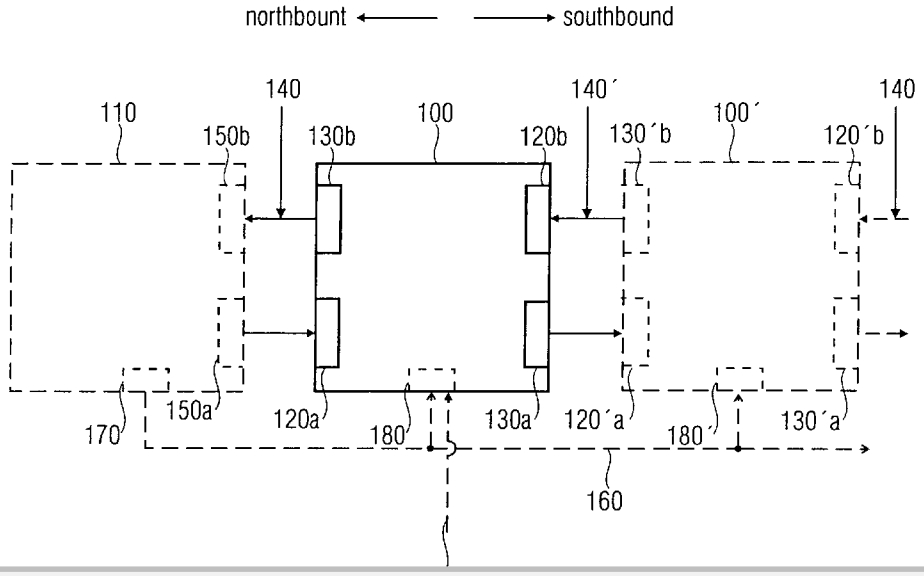
Primary Examiner—Thomas Lee
Assistant Examiner—Vincent T Tran
(74) *Attorney, Agent, or Firm*—Slater & Matsil, L.L.P.

(57) **ABSTRACT**

An apparatus being connectable as a latch stage into a asynchronous latch chain comprises a reception interface, wherein upon receipt of the first signal at the reception interface, the apparatus switches to one of the first power saving mode and a second power saving mode, depending on the second signal at the reception interface and wherein the apparatus offers a first power consumption and a first wake-up time in the first power saving mode, and a second power consumption and a second wake-up time in the second power saving mode.

33 Claims, 2 Drawing Sheets



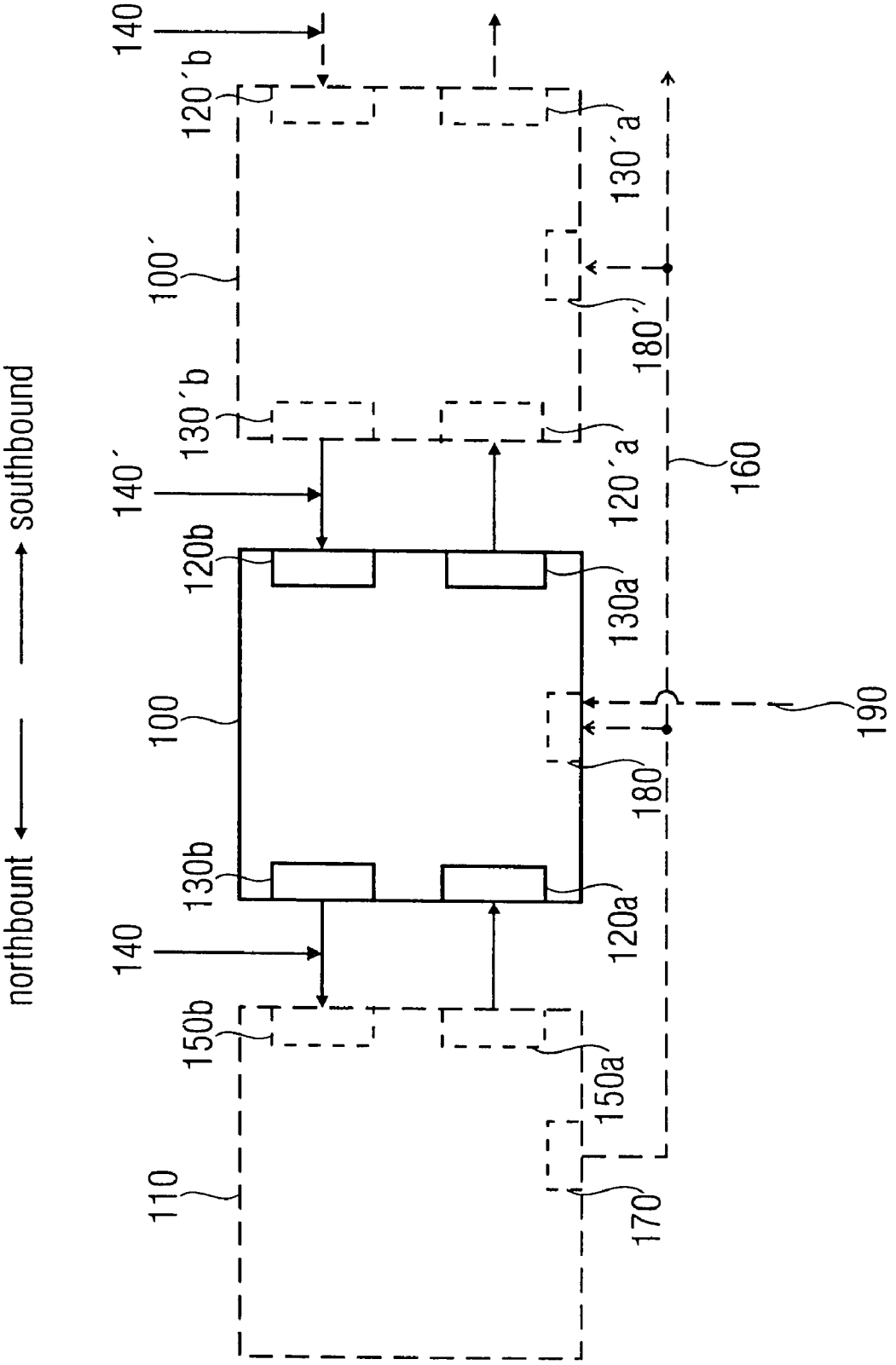


FIG 1

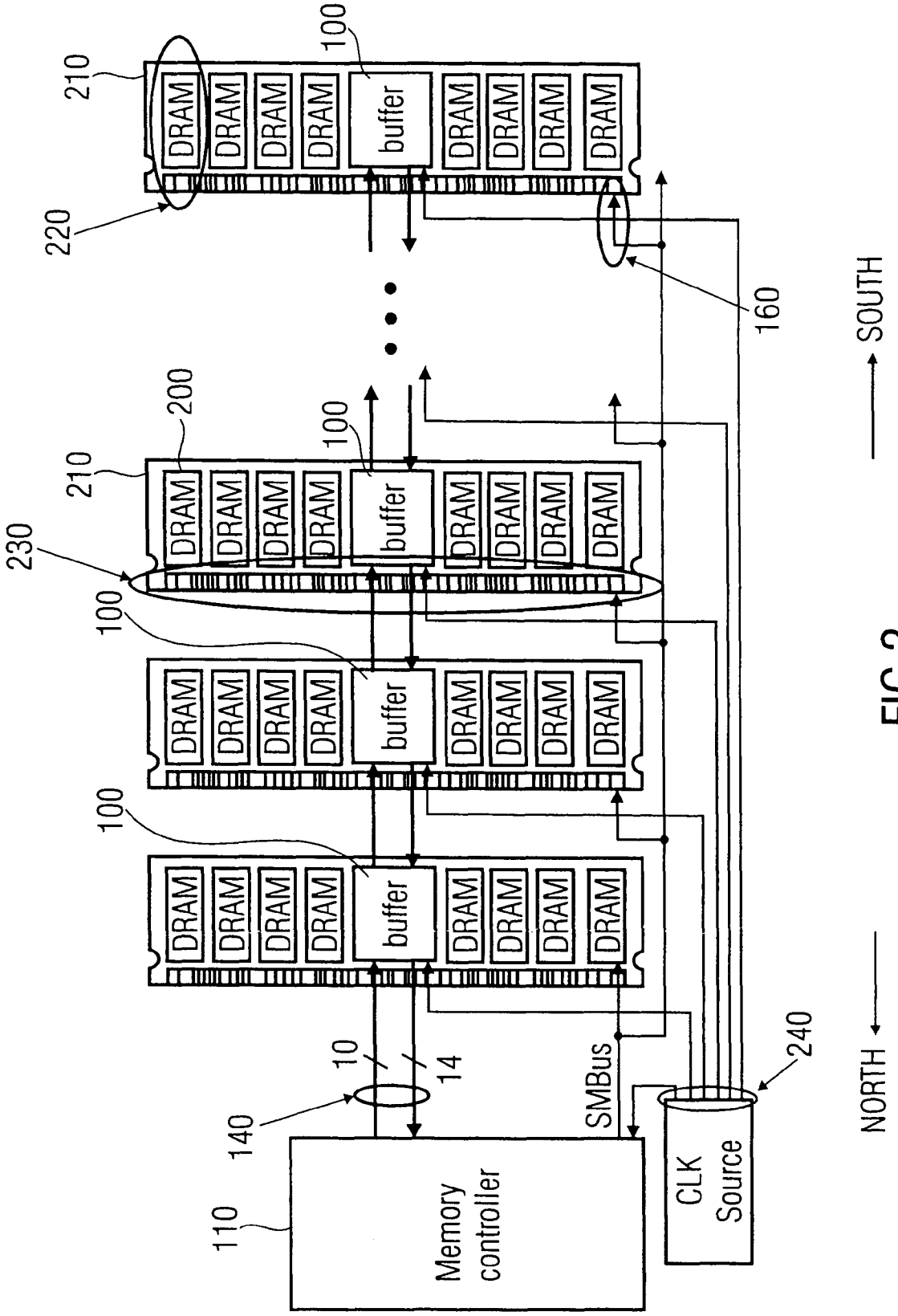


FIG 2

APPARATUS AND METHOD FOR SWITCHING AN APPARATUS TO A POWER SAVING MODE

TECHNICAL FIELD

The present invention relates to an apparatus and method for switching an apparatus to a power saving mode, for instance to an apparatus being connectable, as a latch stage into an asynchronous latch chain, for instance, a memory buffer for a memory bus in a memory system.

BACKGROUND

Modern computer systems offer a significant amount of computing power, as well as a large memory capacity, which enables fast and highly complex computations, as well as fast handling and processing of data. However, in modern computer systems, a key issue is the power management and power consumption. For instance, in the field of mobile computing, the available power is limited by the accumulators and/or the batteries available. Moreover, in the field of stationary computers, power consumption is a great issue, as the power dissipated has to be transported away from the components preventing overheating of the respective circuitries and components.

Many computer systems and components of computer systems offer a power saving mode, in which components of the computer system are turned off or shut down. An example for a computer system or a subsystem of a computer system offering such a power saving mode is the memory system, which is employed in personal computers (PC), servers and workstations. One memory system employed in the mentioned computer systems is referred to as the so-called fully buffered DIMM system or a FBDIMM system (FBDIMM=Fully Buffered Dual Inline Memory Module; DIMM=Dual Inline Memory Module).

Today's concept, especially for high-speed interfaces in FBDIMM systems, however, offers only a single mode to reduce the power consumption of the system. Therefore, a compromise between the power saving and the time needed to switch back from the power saving mode to an active mode, or a normal mode of operation, has to be made since this time is crucial for the system performance.

In other words, measures taken to reduce the power consumption exhibits a strong negative influence on the performance of the computer system, especially the computing power and the available and effective bandwidth of bus structures, which are required for the transport of data between different components of the computer system, for instance, between a processor and the memory. In this context analog circuits used in interfaces exhibit, for example, a large power saving potential but suffer from the fact that they need a long time to recover again since, for instance, control loops and other feedback loops are needed to reach and maintain a stable working point and a stable working condition, before these interfaces can provide a reliable and fast data communication between the components attached.

SUMMARY OF THE INVENTION

An embodiment of an apparatus being connectable, as a latch stage into an asynchronous latch chain comprises a reception interface, wherein upon receipt of a first signal at the reception interface the apparatus switches to one of the

wherein the apparatus offers a first power consumption and a first wake-up time in the first power saving mode and a second power consumption and a second wake-up time in the second power saving mode.

An embodiment of an apparatus being connectable, as a latch stage into an asynchronous latch chain comprises a reception interface, wherein upon receipt of a first signal at the reception interface the apparatus switches to one of the first power saving mode and a second power saving mode, depending on the second signal at the reception interface, wherein the apparatus offers a first power consumption and a first wake-up time in the first power saving mode and a second power consumption and a second wake-up time in the second power saving mode, wherein the first power consumption is higher than the second power consumption and wherein the first wake-up time is shorter than the second wake-up time.

According to a further embodiment of the present invention, a memory system comprises a memory controller, a plurality of memory modules coupled to the memory controller in an asynchronous latch chain configuration, the plurality of memory modules comprising a first memory module and a second memory module, wherein the first memory module is positioned nearer to the memory controller than the second memory module within the asynchronous latch chain, wherein the first memory module offers a first power consumption and a first wake-up time in a first power saving mode, wherein the second memory module offers a second power consumption and second wake-up time in a second power saving mode, wherein each memory module of the plurality of memory modules comprises a reception interface, wherein upon receipt of a first signal from the memory controller at the reception interface, the first memory module switches to the first power saving mode and the second memory module switches to the second power saving mode, wherein the first power consumption is higher than the second power consumption and wherein the first wake-up time is shorter than the second wake-up time.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention are described hereinafter, making reference to the attached drawings.

FIG. **1** shows a schematic block diagram of an embodiment of an apparatus according to a first embodiment of the present invention; and

FIG. **2** shows a schematic block diagram of a second embodiment of an apparatus and an embodiment of a memory system according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

FIGS. **1** and **2** show block diagrams of an embodiment of an apparatus being connectable as a latch stage into an asynchronous latch chain and an embodiment of a memory system. Before a second embodiment of the present invention is described with respect to FIG. **2**, a first embodiment of an apparatus being connectable as a latch stage into an asynchronous latch chain is explained with respect to the schematic representation of an embodiment of the apparatus and an embodiment of a memory system shown in FIG. **1**.

FIG. **1** shows an embodiment of an apparatus **100** integrated into an embodiment of a memory system according to

apparatus **100'** and a memory controller **110** forming an asynchronous latch chain or a daisy chain as will be explained below.

In a so-called daisy chain configuration, components of the daisy chain, which are also referred to as latch stages of the asynchronous latch chain, communicate only with their direct neighbors, for instance, via a wiring scheme comprising interfaces and signal lines of a bus structure. Hence, only neighboring devices are directly coupled to each other. Furthermore, usually in a daisy chain no web like structures are formed and the coupling of the devices does not loop back, for instance, from the first device to the last device in the daisy chain.

In other words, a typical daisy chain configuration in electrical and electronic engineering is a wiring scheme in which, for example, a first device is coupled or wired to a second device, the second device is coupled to a third device, the third device is coupled to a fourth device, and so on. However, the connections of this daisy chain usually do not form webs or loop backs, as discussed above.

In many daisy chain configurations, each of the devices, therefore, comprises circuits working as repeaters or amplifiers to counteract the natural attenuation of the signals when they are transmitted from one device to the next device. In the case of digital signals being exchanged between the different components of a daisy chain, the digital signals may be transferred via an electrical bus as, for instance, in the case of memory devices. In these cases, however, a bus termination might be advisable to implement to prevent reflections and other disturbances of the signals. However, in the case of digital signals, the digital signals may be electrically regenerated or recreated in each device in the daisy chain, as long as they are not modified.

In other words, a signal transmitted over the bus is passed along through each device's interface circuits instead of being transmitted to all devices (simultaneously) by the devices sharing the same bus. Hence, for instance, transmitting a signal from the first device in the daisy chain to the third device in the daisy chain requires the second device to receive the signal from the first device and to forward or to regenerate the signal to be transmitted to the third device of the daisy chain.

Especially in the field of memory devices, the first or central device in the daisy chain is very often the memory controller **110**. Especially in the field of memory devices, the communication in the direction of the memory controller or towards the memory controller **110** is referred to as "northbound" while the opposite direction, the communication from the memory controller to the further devices in the daisy chain is usually referred to as "southbound".

Although embodiments of the present invention are not limited to an application in the field of memory devices, this terminology is adapted in the framework of the present application, as it allows a simple designation of a direction of the communication in the daisy chain or in an asynchronous latch chain.

Turning back to FIG. **1**, the apparatus **100** comprises four sub-interfaces **120***a*, **120***b*, **130***a* and **130***b*. To be more precise, sub-interface **120***a* is part of a reception interface of the apparatus **100**, which is dedicated to receiving northbound signals on a bus **140** coupling the apparatus **100** and the memory controller **110**. The second sub-interface **120***b*, which is dedicated for receiving northbound signal from the further apparatus **100'** which is coupled to the apparatus **100** by a bus **140'**. Both buses **140** and **140'** comprise in the

Accordingly, the apparatus **100** further comprises, apart from the sub-interface **120***a* coupled to the southbound bus structure of the bus **140**, the further sub-interface **130***a* coupled to the southbound bus structure of the bus **140'**. With respect to the northbound communication and the northbound bus structures of the buses **140** and **140'** the apparatus **100** comprises apart from the interface **120***b* coupled to the northbound bus structure of the bus **140'**, the further sub-interface **130***b* coupled to the northbound bus structure of the bus **140**.

While the two sub-interfaces **120***a* and **120***b* are dedicated to receiving signals southbound via the bus **140** and northbound via the bus **140'**, respectively, the sub-interfaces **130***a* and **130***b* are dedicated to transmitting or sending signals over the southbound bus structure of the bus **140'** and the northbound bus structure of the bus **140**, respectively.

As a consequence, the two sub-interfaces **120***a* and **120***b* are part of a reception interface of the apparatus **100**, while the sub-interfaces **130***a* and **130***b* are part of a transmission interface of the apparatus **100**. The further apparatus **100'** of the memory system shown in FIG. **1** comprises also four sub-interfaces **120'***a*, **120'***b*, **130'***a* and **130'***b*, which are dedicated for receiving or sending signals via the buses **140'** and **140"**, coupled to the further apparatus **100'**. Compared to the apparatus **100**, the bus **140'** is coupled to the sub-interfaces **120'***a* and **130'***b* of the further apparatus **100'**, while the bus **140"** is coupled to the sub-interfaces **130'***a* and **120'***b*.

The embodiment of the memory system shown in FIG. **1** further comprises the memory controller **110**, which is coupled to the embodiment of the apparatus **100** via the bus **140**. The southbound bus structure of the bus **140** is coupled to a sub-interface **150***a* of the memory controller **110** while the northbound bus structure of the bus **140** is coupled to a sub-interface **150***b* of the memory controller **110**. The sub-interface **150***a* is, therefore, adapted for transmitting or sending signals via the southbound bus structure of the bus **140** to the sub-interface **120***a* of the apparatus **100**, which is adapted for receiving the signals. Accordingly, the sub-interface **150***b* of the memory controller **110** is adapted to receiving signals sent via the northbound bus structure of the bus **140**, provided by the sub-interface **130***b* of the apparatus **100**.

As a further option, the memory controller **110**, the apparatus **100** and the further apparatus **100'** can be coupled to a signal line **160**, which can, for instance, be an individual signal line or part of a unidirectional or bidirectional bus. The signal line **160** is coupled to an optional interface **170** of the memory controller **110** and two interfaces **180** and **180'** of the apparatus **100** and the further apparatus **100'** respectively. The signal line **160** can, for instance, be employed by the memory controller **110** to provide the apparatuses **100** and **100'** with commands, data, status requests and other signals, so that the interfaces **180** and **180'** of the apparatus **100** and the further apparatus **100'** are capable of receiving signals from the memory controller. In this case, the interfaces **180** and **180'** are also part of the reception interfaces of the apparatus **100** and the further apparatus **100'**, respectively.

The reception interface of the apparatus **100** comprises all interfaces, connectors, (mechanical) jumpers, switches (DIP switches) and terminals, which are designated for and/or capable of receiving signals. In the embodiment of a memory system shown in FIG. **1**, the reception interface of the apparatus **100** comprises the sub-interfaces **120***a* and **120***b* and, if present, the optional interface **180**.

Accordingly, the transmission interface, also referred to as the sending interface of the apparatus **100**, comprises the sub-interfaces **130***a* and **130***b*, as well as, if the interface **180**

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