Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 151145

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Netlist, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	/Noel B. Whitley/	Date (Optional)	12/5/17
Name	Noel B. Whitley		
Title	VP, IP & Licensing		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (06-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 14/489269 filed on September 17, 2014.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Jeffrey C. Solomon Date (Optional) :

Signature: Jeffrey C Solomon

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

PTO/AIA/01 (06-12)
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LEGAL NAME OF INVENTOR

Inventor: Scott H. Milton Date (Optional): 10/17/2014

Signature: Scott H. Milton

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

PTO/AIA/01 (06-12)
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LEGAL NAME OF INVENTOR

Inventor: Hyun Lee Date (Optional) :

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Jayesh Bhakta Date (Optional): 9-17-2014

Signature: Jayesh Bhakta

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Chi-She Chen Date (Optional): Oct-17-2014

Signature: Chi-She Chen

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

PTO/AIA/96 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Hyun Lee et al.

Application No./Patent No.: Attached Application Filed/Issue Date: 03-23-2018

Titled: FLASH-DRAM HYBRID MEMORY MODULE

Netlist, Inc., a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 034531, Frame 0385, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Khaled Shami/	03-23-2018
Signature	Date
Khaled Shami	38,745
Printed or Typed Name	Title or Registration Number

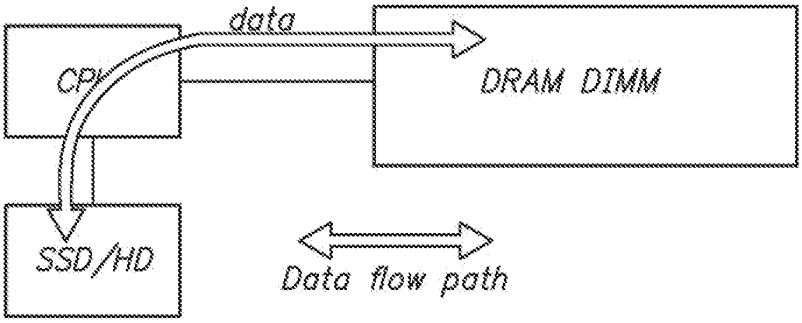


FIG. 1
(PRIOR ART)

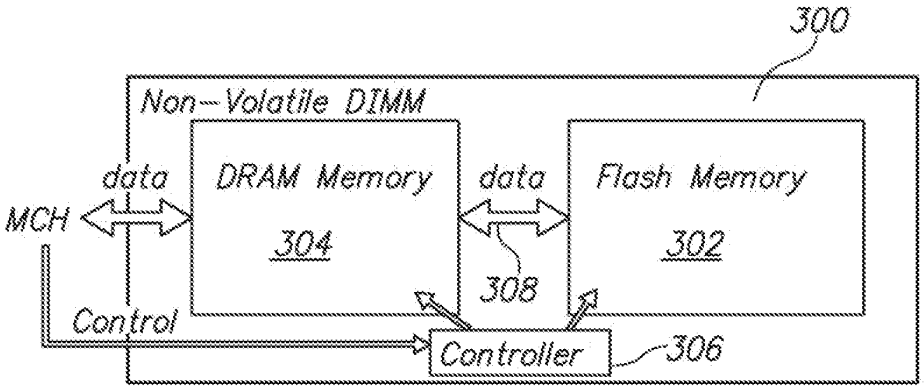
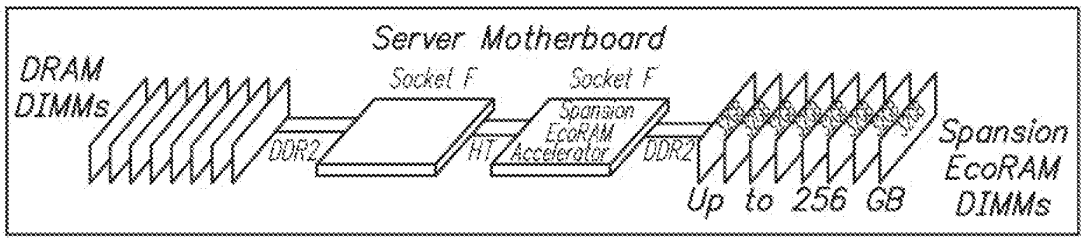


FIG. 3A

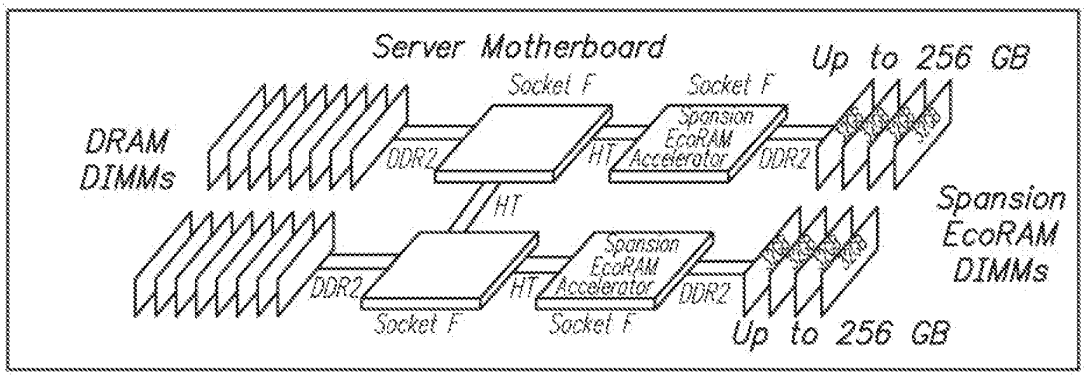
Spansion EcoRAM Configurations

256GB Spansion EcoRAM Solution – Single Accelerator



256GB Single Accelerator Spansion EcoRAM Solution

256GB Spansion EcoRAM Solution – Dual Accelerator



256GB Single Accelerator Spansion EcoRAM Solution

FIG. 2
(PRIOR ART)

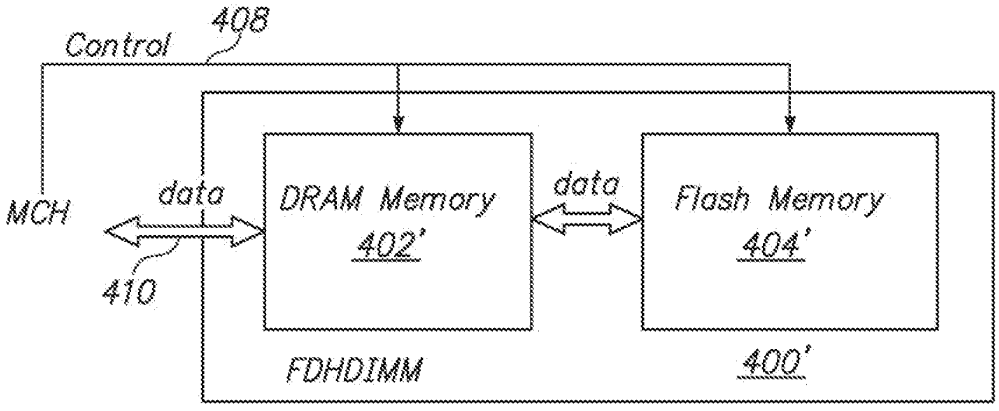


FIG. 4B

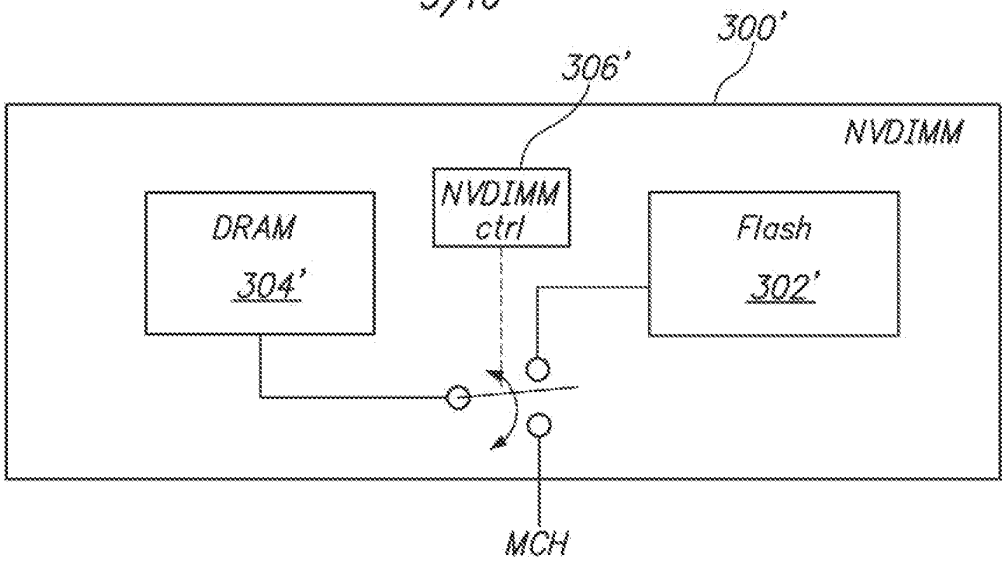

300'
306'
NVDIMM
NVDIMM ctrl
DRAM
304'
Flash
302'
MCH

FIG. 3B

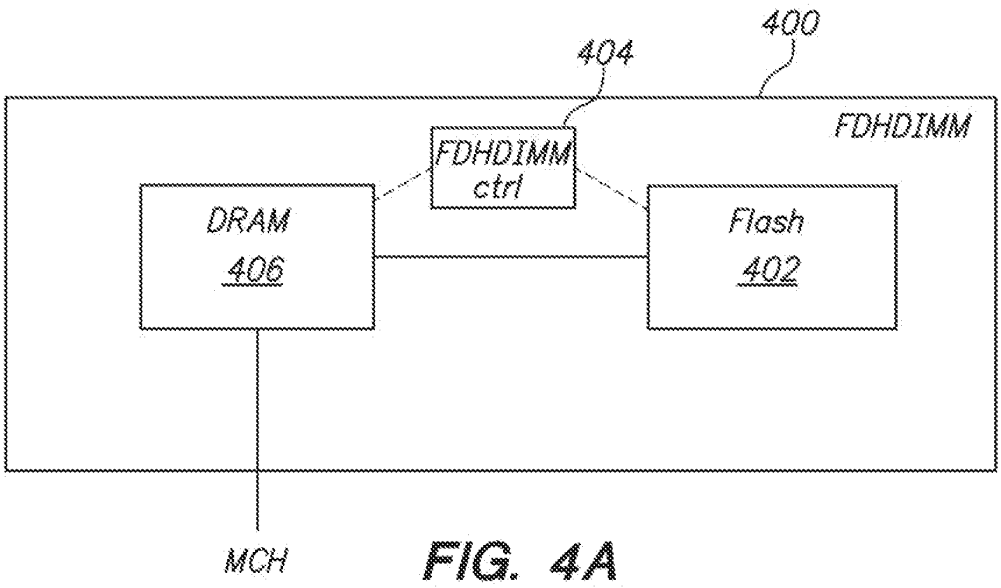

400
404
FDHDIMM
FDHDIMM ctrl
DRAM
406
Flash
402
MCH

FIG. 4A

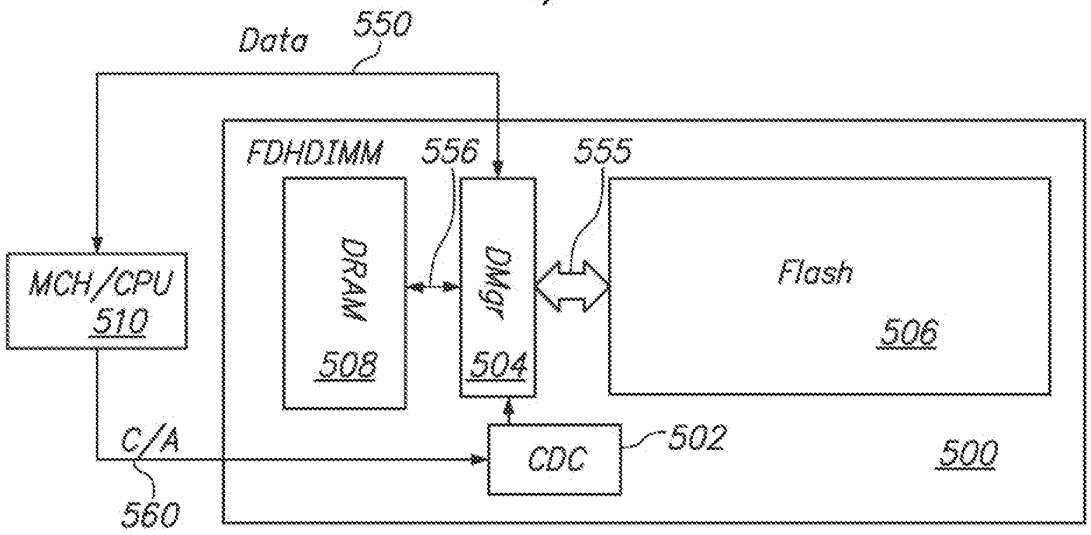

Data
550
FDHDIMM
556
555
DRAM
508
DMgr
504
Flash
506
MCH/CPU
510
C/A
560
CDC
502
500

FIG. 5A

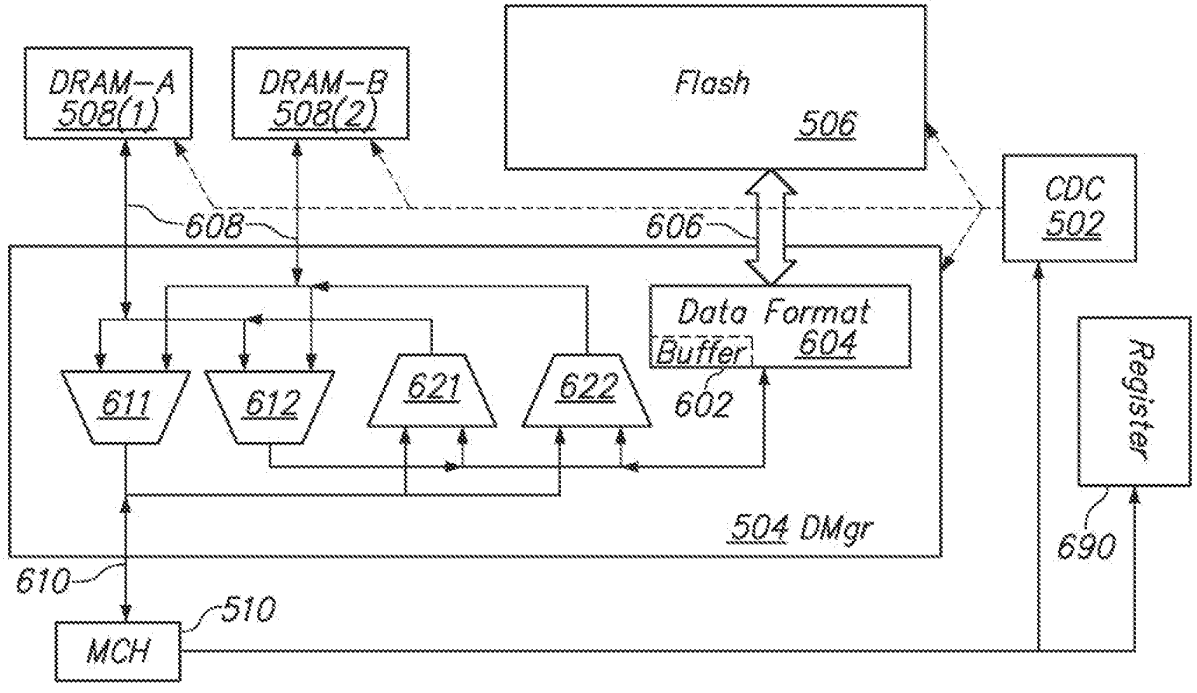

DRAM-A
508(1)
DRAM-B
508(2)
Flash
506
CDC
502
608
606
Data Format
Buffer
604
602
611
612
621
622
504 DMgr
Register
690
610
MCH
510

FIG. 6

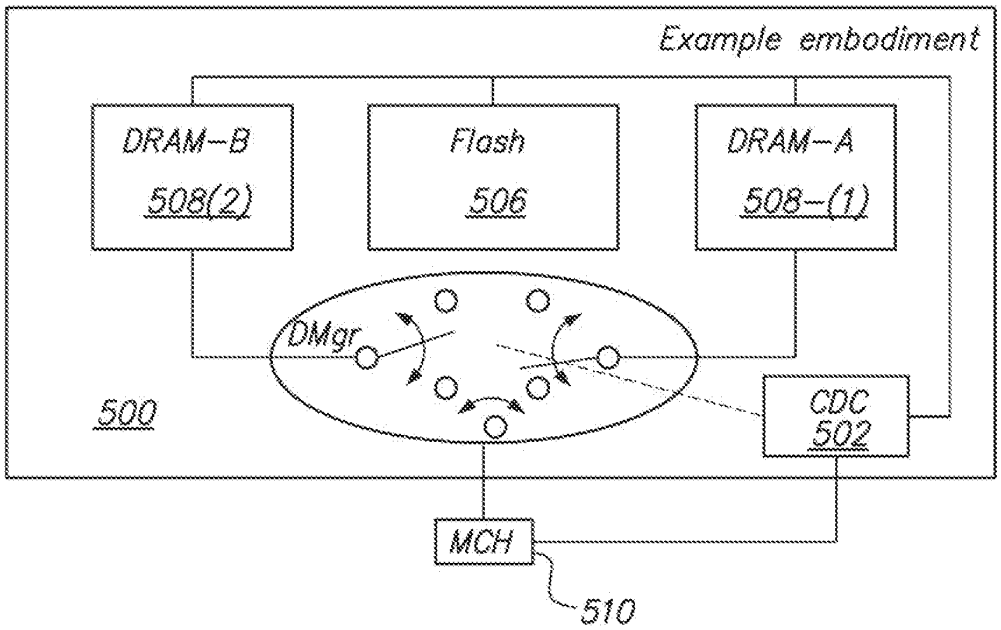

Example embodiment
DRAM–B
508(2)
Flash
506
DRAM–A
508–(1)
DMgr
500
CDC
502
MCH
510

FIG. 5B

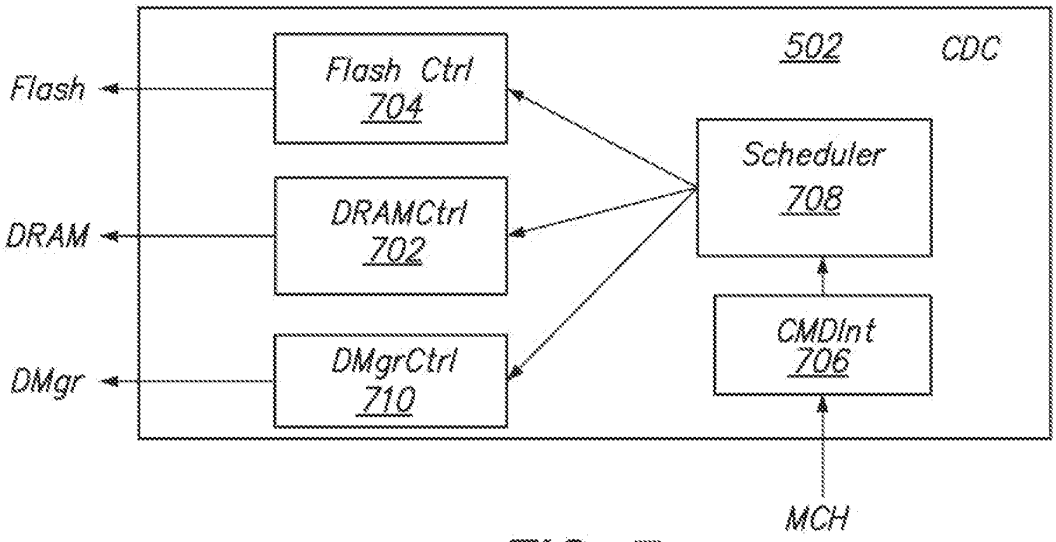

502
CDC
Flash
Flash Ctrl
704
DRAM
DRAMCtrl
702
DMgr
DMgrCtrl
710
Scheduler
708
CMDInt
706
MCH

FIG. 7

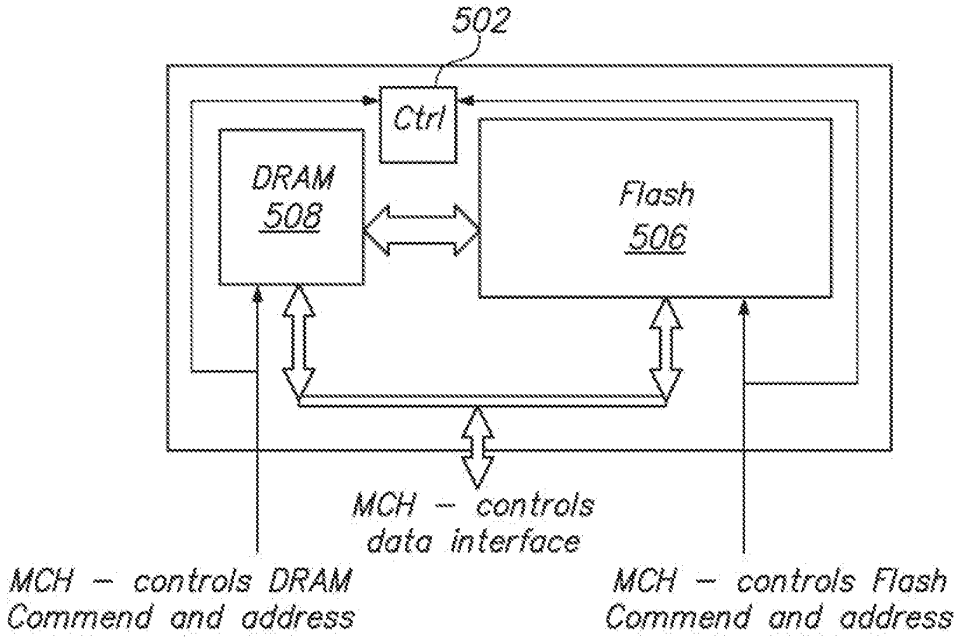

502
Ctrl
DRAM
508
Flash
506
MCH – controls
data interface
MCH – controls DRAM
Commend and address
MCH – controls Flash
Commend and address

FIG. 8A

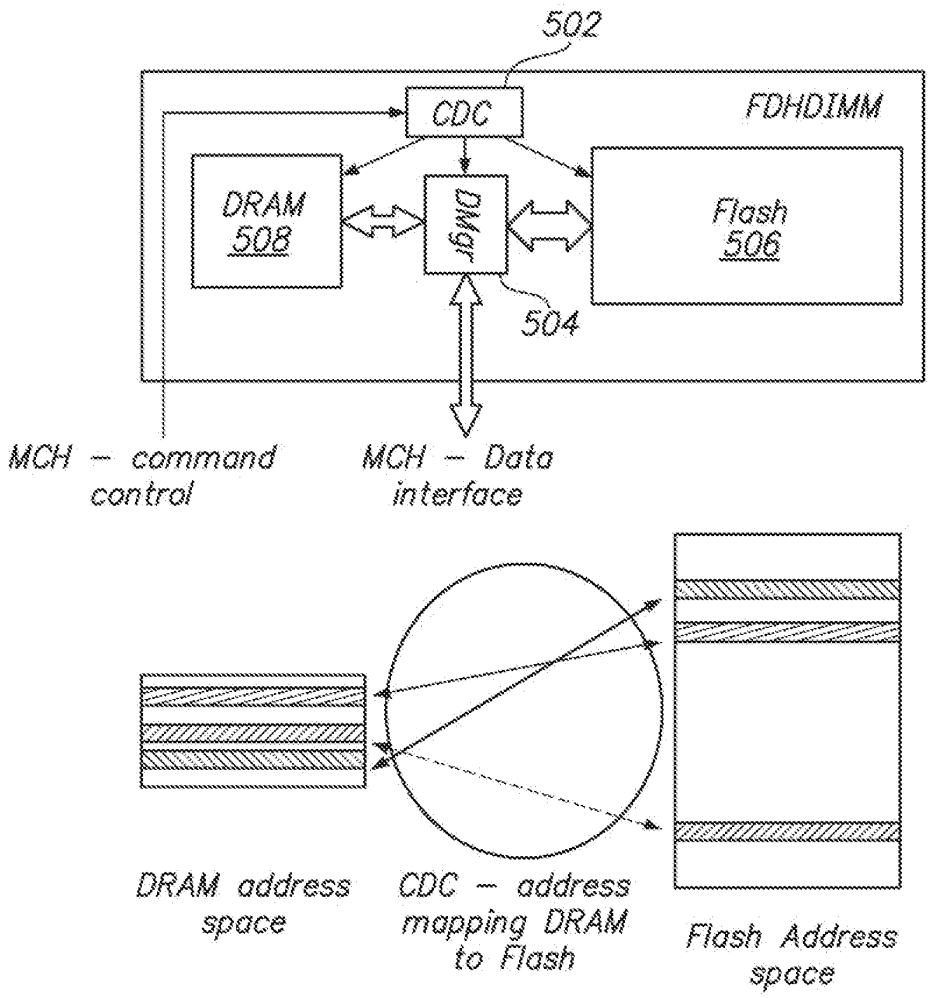

502
CDC
FDHDIMM
DRAM
508
DMgr
Flash
506
504
MCH – command control
MCH – Data interface
DRAM address space
CDC – address mapping DRAM to Flash
Flash Address space

FIG. 8B

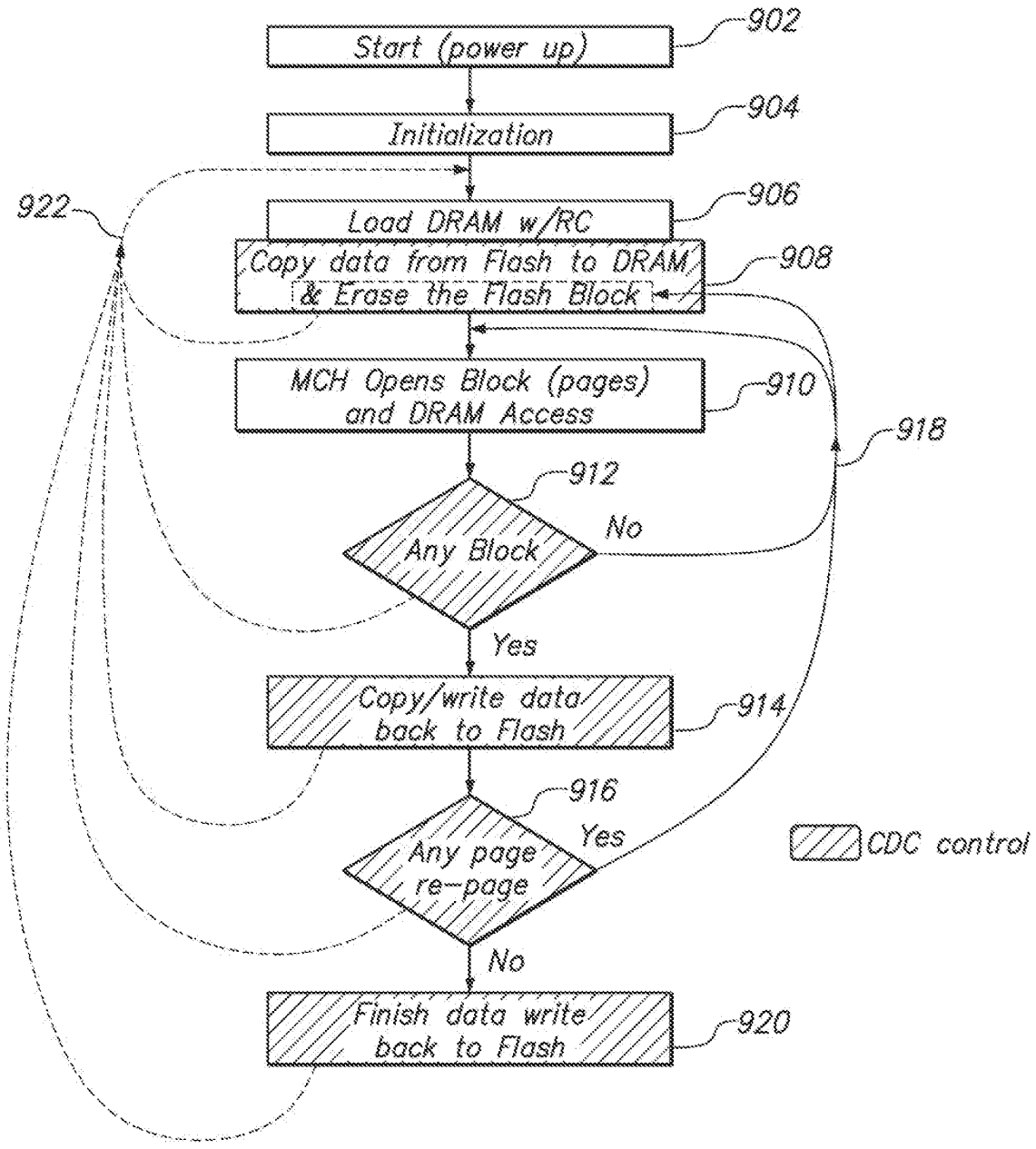

Start (power up)
902
Initialization
904
Load DRAM w/RC
906
Copy data from Flash to DRAM & Erase the Flash Block
908
MCH Opens Block (pages) and DRAM Access
910
Any Block
912
No
Yes
Copy/write data back to Flash
914
Any page re-page
916
Yes
No
Finish data write back to Flash
920
922
918
CDC control

FIG. 9

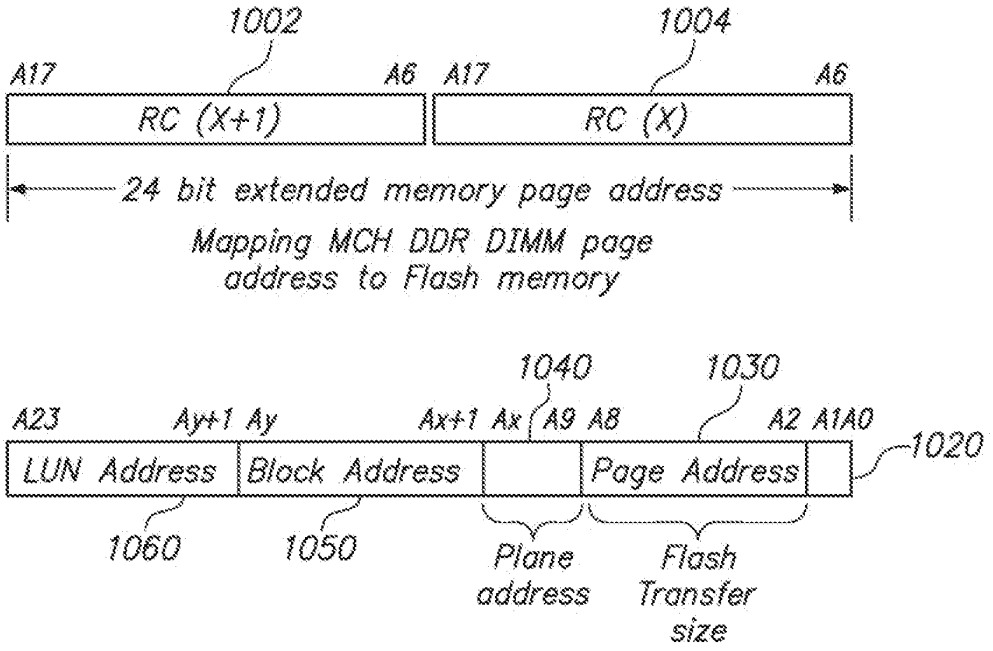

1002
1004
A17
A6
A17
A6
RC (X+1)
RC (X)
24 bit extended memory page address
Mapping MCH DDR DIMM page address to Flash memory
1040
1030
A23
Ay+1 Ay
Ax+1 Ax
A9 A8
A2 A1A0
1020
LUN Address
Block Address
Page Address
1060
1050
Plane address
Flash Transfer size

FIG. 10

DRAM density (GB)	# of blocks per bank	Flash wr-time to rd-time ratio	Avg block use time (sec)	Flash write time (sec)	Max allowed Closed Blk in queue to be written back to Flash
1	250	55	1.00E-03	2.00E-02	0
1	250	55	1.00E-02	2.00E-02	2
1	250	55	2.00E-02	2.00E-02	5
1	250	55	5.00E-02	2.00E-02	11
2	500	55	1.00E-03	2.00E-02	0
2	500	55	1.00E-02	2.00E-02	5
2	500	55	2.00E-02	2.00E-02	9
2	500	55	5.00E-02	2.00E-02	23
4	1000	55	1.00E-03	2.00E-02	1
4	1000	55	1.00E-02	2.00E-02	9
4	1000	55	2.00E-02	2.00E-02	18
4	1000	55	5.00E-02	2.00E-02	45

FIG. 11

FLASH-DRAM HYBRID MEMORY MODULE

PRIORITY CLAIM

[0001] This application is a continuation of U.S. Patent Application No. 14/840,865, filed August 31, 2015, titled "FLASH-DRAM HYBRID MEMORY MODULE," which is a continuation of U.S. Patent No. 9,158,684, issued October 13, 2015, titled, "FLASH-DRAM HYBRID MEMORY MODULE", which is a continuation of U.S. Patent No. 8,874,831, issued, October 28, 2014, titled , "FLASH-DRAM HYBRID MEMORY MODULE", which claims the benefit of provisional patent application serial no. 61/512,871, filed July 28, 2011, and is a continuation-in-part of US Patent No. 8,301,833, issued October 30, 2012, which is a continuation of U.S. patent application serial no. 12/131,873, filed June 2, 2008, which claims the benefit of U.S. provisional patent application serial no. 60/941,586, filed June 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

[0002] The present disclosure relates generally to computer memory devices, and more particularly, to devices that employ different types of memory devices such as combinations of Flash and random access memories.

BACKGROUND

[0003] As technology advances and the usage of portable computing devices, such as tablet notebook computers, increases, more data needs to be transferred among data centers and to/from end users. In many cases, data centers are built by clustering multiple servers that are networked to increase performance.

[0004] Although there are many types of networked servers that are specific to the types applications envisioned, the basic concept is generally to increase server performance by dynamically allocating computing and storage resources. In recent years, server technology has evolved to be specific to particular applications such as 'finance transactions' (for example, point-of-service, inter-bank transaction, stock market transaction), 'scientific computation' (for example, fluid dynamic for automobile and ship design, weather prediction, oil and gas expeditions), 'medical diagnostics' (for example, diagnostics based on the fuzzy logic, medical data processing), 'simple information sharing and searching' (for example, web search, retail store website, company home page), 'email' (information distribution and archive), 'security service', 'entertainment' (for example, video-on-demand), and so on. However, all of these applications suffer from the same information transfer bottleneck due to the inability of a high speed CPU (central processing unit) to efficiently transfer data in and out of relatively slower speed storage or memory subsystems, particularly since data transfers typically pass through the CPU input/output (I/O) channels.

[0005] The data transfer limitations by the CPU are exemplified by the arrangement shown in FIG. 1, and apply to data transfers between main storage (for example the hard disk (HD) or

solid state drive (SSD) and the memory subsystems (for example DRAM DIMM (Dynamic Random Access Memory Dual In-line Memory Module) connected to the front side bus (FSB)). In arrangements such as that of FIG. 1, the SSD/HD and DRAM DIMM of a conventional memory arrangement are connected to the CPU via separate memory control ports (not shown). FIG. 1 specifically shows, through the double-headed arrow, the data flow path between the computer or server main storage (SSD/HD) to the DRAM DIMMs. Since the SSD/HD data I/O and the DRAM DIMM data I/O are controlled by the CPU, the CPU needs to allocate its process cycles to control these I/Os, which may include the IRQ (Interrupt Request) service which the CPU performs periodically. As will be appreciated, the more time a CPU allocates to controlling the data transfer traffic, the less time the CPU has to perform other tasks. Therefore, the overall performance of a server will deteriorate with the increased amount of time the CPU has to expend in performing data transfer.

[0006] There have been various approaches to increase the data transfer throughput rates from/to the main storage, such as SSD/HD, to local storage, such as DRAM DIMM. In one example as illustrated in FIG. 2, EcoRAM™ developed by Spansion provides a storage SSD based system that assumes a physical form factor of a DIMM . The EcoRAM™ is populated with Flash memories and a relatively small memory capacity using DRAMs which serve as a data buffer. This arrangement is capable of delivering higher throughput rate than a standard SSD based system since the EcoRAM™ is connected to the CPU (central processing unit) via a high speed interface, such as the HT (Hyper Transport) interface, while an SSD/HD is typically connected via SATA (serial AT attachment), USB (universal serial bus), or PCI Express (peripheral component interface express). For example, the read random access throughput rate of EcoRAM™ is near 3GB/s compared with 400MB/s for a NAND SSD memory subsystem

using the standard PCI Express-based. This is a 7.5X performance improvement. However, the performance improvement for write random access throughput rate is less than 2X (197MBs for the EcoRAM vs. 104MBs for NAND SSD). This is mainly due to the fact that the write speed is cannot be faster than the NAND Flash write access time. Figure 2 is an example of EcoRAM™ using SSD with the form factor of a standard DIMM such that it can be connected to the FSB (front side bus). However, due to the interface protocol difference between DRAM and Flash, an interface device, EcoRAM Accelerator™), which occupies one of the server's CPU sockets is used, and hence further reducing server's performance by reducing the number of available CPU sockets available, and in turn reducing the overall computation efficiency. The server's performance will further suffer due to the limited utilization of the CPU bus due to the large difference in the data transfer throughput rate between read and write operations.

[0007] The EcoRAM™ architecture enables the CPU to view the Flash DIMM controller chip as another processor with a large size of memory available for CPU access.

[0008] In general, the access speed of a Flash based system is limited by four items: the read/write speed of the Flash memory, the CPU's FSB bus speed and efficiency, the Flash DIMM controller's inherent latency, and the HT interconnect speed and efficiency which is dependent on the HT interface controller in the CPU and Flash DIMM controller chip.

[0009] The published results indicate that these shortcomings are evident in that the maximum throughput rate is 1.56 GBs for the read operation and 104 MBs for the write operation. These access rates are 25% of the DRAM read access speed, and 1.7% of the DRAM access speed at 400MHz operation. The disparity in the access speed (15 to 1) between the read

operation and write operation highlight a major disadvantage of this architecture. The discrepancy of the access speed between this type of architecture and JEDEC standard DRAM DIMM is expected to grow wider as the DRAM memory technology advances much faster than the Flash memory.

OVERVIEW

[0010] Described herein is a memory module couplable to a memory controller of a host system. The memory module includes a non-volatile memory subsystem, a data manager coupled to the non-volatile memory subsystem, a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager, and a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller.

[0011] Also described herein is a method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems. The method includes receiving control information from the memory controller, wherein the control information is received using a protocol of the volatile memory subsystem. The method further includes identifying a data path to be used for transferring data to or from the memory module using the received control information, and using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory

subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path.

[0012] Also described herein is a memory module wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring, and data error correction in response to receiving at least one of a control signal and control information from the controller.

[0013] Also described herein is a memory module wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller.

[0014] Also described herein is a memory module wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer.

[0015] Also described herein is a memory module wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module.

[0016] Also described herein is a memory module wherein the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0017] Also described herein is a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0018] Also described herein is a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0019] Also described herein is a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0020] Also described herein is a memory module wherein the non-volatile memory subsystem comprises flash memory.

[0021] Also described herein is a memory module wherein at least one set of data ports is operated by the data manager to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0022] Also described herein is a memory module wherein the data manager and controller are configured to effect data transfer between the memory controller and the non-volatile memory subsystem in response to memory access commands received by the controller from the memory controller.

[0023] Also described herein is a memory module wherein the volatile memory subsystem is operable as a buffer for the data transfer between the memory controller and non-volatile memory.

[0024] Also described herein is a memory module wherein the data manager further includes a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

[0025] Also described herein is a memory module wherein the data manager further includes a data buffer for buffering data delivered to or from the non-volatile memory subsystem.

[0026] Also described herein is a memory module wherein the controller is operable to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0027] Also described herein is a memory module wherein the controller is configured to effect operation with the host system in accordance with a prescribed protocol.

[0028] Also described herein is a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0029] Also described herein is a memory module wherein the controller is operable to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0030] Also described herein is a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0031] Also described herein is a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0032] Also described herein is a memory module wherein the controller is operable to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0033] Also described herein is a memory module wherein the controller includes a volatile memory control module, a non-volatile memory control module, data manager control module, a command interpreter module, and a scheduler module.

[0034] Also described herein is a memory module wherein commands from the volatile memory control module to the volatile memory subsystem are subordinated to commands from the memory controller to the controller.

[0035] Also described herein is a memory module wherein the controller effects pre-fetching of data from the non-volatile to the volatile memory.

[0036] Also described herein is a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0037] Also described herein is a memory module wherein the controller is operable to initiate a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0038] Also described herein is a memory module wherein, if the closed block is re-opened, the controller is operable to abort the copy operation and to erase the target block from the non-volatile memory subsystem.

[0039] Also described herein is a method for managing a memory module wherein the transfer of data includes a bidirectional transfer of data between the non-volatile and the volatile memory subsystems.

[0040] Also described herein is a method for managing a memory module further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data.

[0041] Also described herein is a method for managing a memory module further comprising operating the data manager to control data traffic between the memory controller and at least one of the volatile and non-volatile memory subsystems.

[0042] Also described herein is a method for managing a memory module wherein data traffic control relates to any one or more of data transfer size, formatting information, direction of data flow, and the starting time of the transfer of data.

[0043] Also described herein is a method for managing a memory module wherein data traffic control by the data manager is based on instructions received from the controller.

[0044] Also described herein is a method for managing a memory module further comprising operating the data manager as a bi-directional data transfer fabric with two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0045] Also described herein is a method for managing a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0046] Also described herein is a method for managing a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0047] Also described herein is a method for managing a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0048] Also described herein is a method for managing a memory module wherein the non-volatile memory subsystem comprises Flash memory.

[0049] Also described herein is a method for managing a memory module further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0050] Also described herein is a method for managing a memory module further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller.

[0051] Also described herein is a method for managing a memory module further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem.

[0052] Also described herein is a method for managing a memory module further comprising using the controller to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0053] Also described herein is a method for managing a memory module further comprising using the controller to effect communication with a host system by the volatile memory subsystem in accordance with a prescribed protocol.

[0054] Also described herein is a method for managing a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0055] Also described herein is a method for managing a memory module further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0056] Also described herein is a method for managing a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0057] Also described herein is a method for managing a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0058] Also described herein is a method for managing a memory module further comprising using the controller to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0059] Also described herein is a method for managing a memory module wherein the controller includes a volatile memory control module, the method further comprising generating

commands by the volatile memory control module in response to commands from the memory controller, and transmitting the generated commands to the volatile memory subsystem.

[0060] Also described herein is a method for managing a memory module further comprising pre-fetching of data from the non-volatile memory subsystem to the volatile memory subsystem.

[0061] Also described herein is a method for managing a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0062] Also described herein is a method for managing a memory module further comprising initiating a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0063] Also described herein is a method for managing a memory module further comprising aborting the copy operation when the closed block of the volatile memory subsystem is re-opened, and erasing the target block in the non-volatile memory subsystem.

BRIEF DESCRIPTION OF THE DRAWINGS

[0064] The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or more examples of embodiments and, together with the description of example embodiments, serve to explain the principles and implementations of the embodiments.

[0065] In the drawings:

FIG. 1 is a block diagram illustrating the path of data transfer, via a CPU, of a conventional memory arrangement;

FIG. 2 is a block diagram of a known EcoRAM™ architecture;

FIGS. 3A and 3B are block diagrams of a non-volatile memory DIMM or NVDIMM;

FIGS. 4A and 4B are block diagrams of a Flash-DRAM hybrid DIMM or FDHDIMM;

FIG. 5A is a block diagram of a memory module 500 in accordance with certain embodiments described herein;

FIG. 5B is a block diagram showing some functionality of a memory module such as that shown in FIG. 5A;

FIG. 6 is a block diagram showing some details of the data manager (DMgr);

FIG. 7 is a functional block diagram of the on-module controller (CDC);

FIG. 8A is a block diagram showing more details of the prior art Flash-DRAM hybrid DIMM (FDHDIMM) of FIGS. 4A and 4B;

FIG. 8B is a block diagram of a Flash-DRAM hybrid DIMM (FDHDIMM) in accordance with certain embodiments disclosed herein;

FIG. 9 is a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM;

FIG. 10 is a block diagram showing an example of mapping of DRAM address space to Flash memory address space; and

FIG. 11 is a table showing estimates of the maximum allowed closed blocks in a queue to be written back to Flash memory for different DRAM densities using various average block use time.

DESCRIPTION OF EXAMPLE EMBODIMENTS

[0066] Example embodiments are described herein in the context of a system of computers, servers, controllers, memory modules, hard disk drives and software. Those of ordinary skill in the art will realize that the following description is illustrative only and is not intended to be in any way limiting. Other embodiments will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to implementations of the example embodiments as illustrated in the accompanying drawings. The same reference indicators will be used to the extent possible throughout the drawings and the following description to refer to the same or like items.

[0067] In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It will, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be

a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

[0068] In accordance with this disclosure, the components, process steps, and/or data structures described herein may be implemented using various types of operating systems, computing platforms, computer programs, and/or general purpose machines. In addition, those of ordinary skill in the art will recognize that devices of a less general purpose nature, such as hardwired devices, field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), or the like, may also be used without departing from the scope and spirit of the inventive concepts disclosed herein. Where a method comprising a series of process steps is implemented by a computer or a machine and those process steps can be stored as a series of instructions readable by the machine, they may be stored on a tangible medium such as a computer memory device (e.g., ROM (Read Only Memory), PROM (Programmable Read Only Memory), EEPROM (Electrically Eraseable Programmable Read Only Memory), Flash memory, Jump Drive, and the like), magnetic storage medium (e.g., tape, magnetic disk drive, and the like), optical storage medium (e.g., CD-ROM, DVD-ROM, paper card, paper tape and the like) and other types of program memory.

[0069] The term "exemplary" where used herein is intended to mean "serving as an example, instance or illustration." Any embodiment described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments.

[0070] Disclosed herein are arrangements for improving memory access rates and addressing the high disparity (15 to 1 ratio) between the read and write data throughput rates. In one

arrangement, a Flash-DRAM-hybrid DIMM (FDHDIMM) with integrated Flash and DRAM is used. Methods for controlling such an arrangement are described.

[0071] In certain embodiments, the actual memory density (size or capacity) of the DIMM and/or the ratio of DRAM memory to Flash memory are configurable for optimal use with a particular application (for example, POS, inter-bank transaction, stock market transaction, scientific computation such as fluid dynamics for automobile and ship design, weather prediction, oil and gas expeditions, medical diagnostics such as diagnostics based on the fuzzy logic, medical data processing, simple information sharing and searching such as web search, retail store website, company home page, email or information distribution and archive, security service, and entertainment such as video-on-demand).

[0072] In certain embodiments, the device contains a high density Flash memory with a low density DRAM, wherein the DRAM is used as a data buffer for read/write operation. The Flash serves as the main memory. Certain embodiments described herein overcome the needs of having a long separation period between an Activate command (may be referred to as RAS) and a corresponding read or write command (may be referred to as first CAS command).

[0073] In accordance with one embodiment, described with reference to FIGS. 3A and 3B, a memory system 300 includes a non-volatile (for example Flash) memory subsystem 302 and a volatile (for example DRAM) memory subsystem 304. The examples of FIGS. 3A and 3B are directed to architectures of a non-volatile DIMM (NVDIMM) NVDIMM system that may use a power subsystem (not shown) that can include a battery or a capacitor as a means for energy storage to copy DRAM memory data into Flash memory when power loss occurs, is detected, or

is anticipated to occur during operation. When normal power is restored, a restore NVDIMM operation is initiated and the data stored in the Flash memory is properly restored to the DRAM memory. In this architecture, the density of the Flash is about the same as the DRAM memory size or within a few multiples, although in some applications it may be higher. This type of architecture may also be used to provide non-volatile storage that is connected to the FSB (front side bus) to support RAID (Redundant Array of Independent Disks) based systems or other type of operations. An NVDIMM controller 306 receives and interprets commands from the system memory controller hub (MCH). The NVDIMM controller 306 control the NVDIMM DRAM and Flash memory operations. In FIG. 3A, the DRAM 304 communicates data with the MCH, while an internal bus 308 is used for data transfer between the DRAM and Flash memory subsystems. In FIG. 3B, the NVDIMM controller 306' of NVDIMM 300' monitors events or commands and enables data transfer to occur in a first mode between the DRAM 304' and Flash 302' or in a second mode between the DRAM and the MCH.

[0074] In accordance with one embodiment, a general architecture for a Flash and DRAM hybrid DIMM (FDHDIMM) system 400 is shown in FIG. 4A. The FDHDIMM interfaces with an MCH (memory controller hub) to operate and behave as a high density DIMM, wherein the MCH interfaces with the non-volatile memory subsystem (for example Flash) 402 is controlled by an FDHDIMM controller 404. Although the MCH interfaces with the Flash via the FDHDIMM controller, the FDHDIMM overall performance is governed by the Flash access time. The volatile memory subsystem (for example DRAM) 406 is primarily used as a data buffer or a temporary storage location such that data from the Flash memory 402 is transferred to the DRAM 406 at the Flash access speed, and buffered or collected into the DRAM 406, which then transfers the buffered data to the MCH based on the access time of DRAM. Similarly,

when the MCH transfers data to the DRAM 406, the FDHDIMM controller 404 manages the data transfer from the DRAM 406 to the Flash 402. Since the Flash memory access speed (both read and write) is relatively slower than DRAM, (e.g. for example a few hundred microseconds for read access), the average data throughput rate of FDHDIMM 400 is limited by the Flash access speed. The DRAM 406 serves as a data buffer stage that buffers the MCH read or write data. Thus, the DRAM 406 serves as a temporary storage for the data to be transferred from/to the Flash 402. Furthermore, in accordance with one embodiment, the MCH recognizes the physical density of an FDHDIMM operating as a high density DIMM as the density of Flash alone.

[0075] In accordance with one embodiment, a read operation can be performed by the MCH by sending an activate command (may be simply referred to as RAS, or row address strobe) to the FDHDIMM 400 to conduct a pre-fetch read data operation from the Flash 402 to the DRAM 406, with the pre-fetch data size being for example a page (1KB or 2KB, or may be programmable to any size). The MCH then sends a read command (may be simply referred to as CAS, or column address strobe) to read the data out input of the DRAM. In this embodiment, the data transfer from Flash to DRAM occurs at Flash access speed rates, while data transfer from DRAM to MCH occurs at DRAM access speed rates. In this example, data latency and throughput rates are the same as any DRAM operation as long as the read operations are executed onto the pages that were opened with the activate command previously sent to pre-fetch data from the Flash to DRAM. Thus, a longer separation time period between the RAS (e.g. Activate command) and the first CAS (column address strobe e.g. read or write command) is required to account for the time it takes to pre-fetch data from the Flash to DRAM.

[0076] An example of FDHDIMM operating as a DDR DIMM with SSD is shown in FIG. 4B, wherein the FDHDIMM 400'supports two different interface interpretations to the MCH. In the first interface interpretation, the MCH views the FDHDIMM 400' as a combination of DRAM DIMM and SSD (not illustrated). In this mode the MCH needs to manage two address spaces, one for the DRAMs 402' and one for the Flash 404'. The MCH is coupled to, and controls, both of the DRAM and Flash memory subsystems. One advantage of this mode is that the CPU does not need to be in the data path when data is moved from DRAM to Flash or from Flash to DRAM. In the second interface interpretation, the MCH views the FDHDIMM 400' as an on-DIMM Flash with the SSD in an extended memory space that is behind the DRAM space. Thus, in this mode, the MCH physically fetches data from the SSD to the DDR DRAM and then the DRAM sends the data to the MCH. Since all data movement occurs on the FDHDIMM, this mode will provide better performance than if the data were to be moved through or via the CPU.

[0077] In accordance with one embodiment and as shown in FIG. 4B, the FDHDIMM 400' receives control signals 408 from the MCH, where the control signals may include one or more control signals specifically for the DRAM 402' operation and one or more control signals specifically for the Flash 404' operation. In this embodiment, the MCH or CPU is coupled to the FDHDIMM via a single data bus interface 410 which couples the MCH to the DRAM.

[0078] FIGS. 5A and 5B are block diagrams of a memory module 500 that is couplable to a host system (not shown). The host system may be a server or any other system comprising a memory system controller or an MCH for providing and controlling the read/write access to one or more memory systems, wherein each memory system may include a plurality of memory subsystems, a plurality of memory devices, or at least one memory module. The term

"read/write access" means the ability of the MCH to interface with a memory system or subsystem in order to write data into it or read data from it, depending on the particular requirement at a particular time.

[0079] In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory subsystem which may be integrated with other components of a host system. In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor, and may be referred to as a FDHDIMM, although it is to be understood that in both structure and operation it may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B. Memory module 500 includes two on-module intermediary components: a controller and a data manager. These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal. In the case of a DIMM, these on-module intermediary components are an on-DIMM Controller (CDC) 502 and an on-DIMM data manager (DMgr) 504. While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well. CDC 502 and data manager DMgr 504 are operative to manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510.

[0080] In certain embodiments, CDC 502 controls the read/write access to/from Flash memory 506 from/to DRAM memory 508, and to/from DRAM memory from/to MCH 510. Read/write access between DRAM 508, Flash 506 and MCH 510 may be referred to herein generally as communication, wherein control and address information C/A 560 is sent from MCH 510 to CDC 502, and possible data transfers follow as indicated by Data 550, Data 555, and/or Data 556. In certain embodiments, the CDC 502 performs specific functions for memory address transformation, such as address translation, mapping, or address domain conversion, Flash access control, data error correction, manipulation of data width or data formatting or data modulation between the Flash memory and DRAM, and so on. In certain embodiments, the CDC 502 ensures that memory module 500 provides transparent operation to the MCH in accordance with certain industry standards, such as DDR, DDR2, DDR3, DDR4 protocols. In the arrangement shown in FIGS. 5A and 5B, there is no direct access from the MCH 510 to the Flash 506 memory subsystem. Thus in accordance with certain embodiments, the Flash access speed has minimal impact on the overall FDHDIMM access speed. In the schematic illustration of FIG. 5B and in accordance with one embodiment, the CDC controller 502 receives standard DDR commands from the MCH, interprets, and produces commands and/or control signals to control the operation of the Data manager (DMgr), the Flash memory and the DRAM memory. The DMgr controls the data path routing amongst DRAMs, Flash and MCH, as detailed below. The data path routing control signals are independently operated without any exclusivity.

[0081] An exemplary role of DMgr 504 is described with reference to FIG. 6. In certain embodiments and in response to communication from CDC 502, DMgr 504 provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction. For example, these functions or operations can be performed on-the-fly

(while data is being transferred via the DMgr 504) or performed on buffered or stored data in DRAM or a buffer. In addition, one role of DMgr 504 is to provide interoperability among various memory subsystems or components and/or MCH 510.

[0082] In one embodiment, an exemplary host system operation begins with initialization. The CDC 502 receives a first command from the MCH 510 to initialize FDHDIMM 500 using a certain memory space. The memory space as would be controlled by MCH 510 can be configured or programmed during initialization or after initialization has completed. The MCH 510 can partition or parse the memory space in various ways that are optimized for a particular application that the host system needs to run or execute. In one embodiment, the CDC 502 maps the actual physical Flash 506 and DRAM 508 memory space using the information sent by MCH 510 via the first command. In one embodiment, the CDC 502 maps the memory address space of any one of the Flash 506 and DRAM 508 memory subsystems using memory address space information that is received from the host system, stored in a register within FDHDIMM 500, or stored in a memory location of a non-volatile memory subsystem, for example a portion of Flash 506 or a separate non-volatile memory subsystem. In one embodiment, the memory address space information corresponds to a portion of initialization information of the FDHDIMM 500.

[0083] In one embodiment, MCH 510 may send a command to restore a certain amount of data information from Flash 506 to DRAM 508. The CDC 502 provides control information to DMgr 504 to appropriately copy the necessary information from Flash 506 to the DRAM 508. This operation can provide support for various host system booting operations and/or a special host system power up operation.

[0084] In one embodiment, MCH 510 sends a command which may include various fields comprising control information regarding data transfer size, data format options, and/or startup time. CDC 502 receives and interprets the command and provides control signals to DMgr 504 to control the data traffic between the Flash 506, the DRAM 508, and the MCH 510. For example, DMgr 504 receives the data transfer size, formatting information, direction of data flow (via one or more multiplexers such as 611, 612, 621, 622 as detailed below), and the starting time of the actual data transfer from CDC 502. DMgr 504 may also receive additional control information from the CDC 502 to establish a data flow path and/or to correctly establish the data transfer fabric. In certain embodiments, DMgr 504 also functions as a bi-directional data transfer fabric. For example, DMgr 504 may have more than 2 sets of data ports facing the Flash 506 and the DRAM 508. Multiplexers 611 and 612 provide controllable data paths from any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B) to any one of the MCH 510 and the Flash 506. Similarly multiplexers 621 and 622 provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B). In one embodiment, DRAM 508(1) is a segment of DRAM 508, while in other embodiments, DRAM 508(1) is a separate DRAM memory subsystem. It will be understood that each memory segment can comprise one or more memory circuits, a memory devices, and/or memory integrated circuits. Of course other configurations for DRAM 508 are possible, and other data transfer fabrics using complex data paths and suitable types of multiplexing logic are contemplated.

[0085] In accordance with one embodiment, the two sets of multiplexors 611, 612 and 621, 622 allow independent data transfer to Flash 506 from DRAM-A 508(1) and DRAM-B 508(2). For example, in response to one or more control signals or a command from CDC 502, DMgr

504 can transfer data from DRAM-A 508(1) to MCH 510, via multiplexer 611, at the same time as from DRAM-B 508(2) to the Flash 506, via multiplexer 612; or data is transferred from DRAM-B 508(2) to MCH 510, via multiplexer 611, and simultaneously data is transferred from the Flash 506 to DRAM-A 508(1), via multiplexer 621. Further, in the same way that data can be transferred to or from the DRAM in both device-wide or segment-by-segment fashion, data can be transferred to or from the flash memory in device-wide or segment-by-segment fashion, and the flash memory can be addressed and accessed accordingly.

[0086] In accordance with one embodiment the illustrated arrangement of data transfer fabric of DMgr 504 also allows the CDC 502 to control data transfer from the Flash memory to the MCH by buffering the data from the Flash 506 using a buffer 602, and matching the data rate and/or data format of MCH 510. The buffer 602 is shown in FIG. 6 as a portion of a data format module 604; however, buffer 602 may also be a distributed buffer such that one buffer is used for each one of the set of multiplexer logic elements shown as multiplexers 611, 612, 621, and 622. Various buffer arrangements may be used, such as a programmable size buffer to meet the requirement of a given system design requirement, for example the disparity between read/write access time; or overall system performance, for example latency. In certain embodiments, the buffer 604 may introduce one or more clock cycle delays into a data communication path between MCH 510, DRAM 508, and Flash 506.

[0087] In certain embodiments, data format module 604 contains a data formatting subsystem (not shown) to enable DMgr 504 to format and perform data transfer in accordance with control information received from CDC502. Data buffer 604 of data format module 602, discussed above, also supports a wide data bus 606 coupled to the Flash memory 506 operating

at a first frequency, while receiving data from DRAM 508 using a relatively smaller width data bus 608 operating at a second frequency, the second frequency being larger than the first frequency in certain embodiments. The buffer 602 is designed to match the data flow rate between the DRAM 508 and the Flash 506.

[0088] A register 690 provides the ability to register commands received from MCH 510 via C/A 560 (FIG. 5A). The register 690 may communicate these commands to CDC 502 and/or to the DRAM 508 and/or Flash 506. The register 690 communicates these registered commands to CDC 502 for processing. The register 690 may also include multiple registers (not shown), such that it can provide the ability to register multiple commands, a sequence of commands, or provide a pipeline delay stage for buffering and providing a controlled execution of certain commands received form MCH 510.

[0089] In certain embodiments, the register 690 may register commands from MCH 510 and transmit the registered commands to DRAM 508 and/or Flash 506 memory subsystems. In certain embodiments, the CDC 502 monitors commands received from MCH 510, via control and address bus C/A 560, and provides appropriate control information to DMgr 504, DRAM 508, or Flash 506 to execute these commands and perform data transfer operations between MCH 510 and FDHDIMM 500 via MCH data bus 610.

[0090] FIG. 7 illustrates a functional block diagram of the CDC 502. In certain embodiments, the major functional blocks of the CDC 502 are a DRAM control block DRAMCtrl 702, Flash control block FlashCtrl 704, MCH command interpreter CmdInt 706, DRAM-Flash interface scheduler Scheduler 708, and DMgr control block (DMgrCtrl) 710.

[0091] In accordance with one embodiment, DRAMCtrl 702 generates DRAM commands that are independent from the commands issued by the MCH 510. In accordance with one embodiment, when the MCH 510 initiates a read/write operation from/to the same DRAM 508 that is currently executing a command from the DRAMCtrl 702, then the CDC 502 may choose to instruct DRAMCtrl 702 to abort its operation in order to execute the operation initiated by the MCH. However, the CDC 502 may also pipeline the operation so that it causes DRAMCtrl 702 to either halt or complete its current operation prior to executing that of the MCH. The CDC 502 may also instruct DRAMCtrl 702 to resume its operation once the command from MCH 510 is completed.

[0092] In accordance with one embodiment, the FlashCtrl 704 generates appropriate Flash commands for the proper read/write operations. The CmdInt 706 intercepts commands received from MCH 510 and generates the appropriate control information and control signals and transmit them to the appropriate FDHDIMM functional block. For example, CmdInt 706 issues an interrupt signal to the DRAMCtrl 702 when the MCH issues a command that collides (conflicts) with the currently executing or pending commands that DRAMCtrl 702 has initiated independently from MCH 510, thus subordinating these commands to those from the MCH. The Scheduler 708 schedules the Flash–DRAM interface operation such that there is no resource conflict in the DMgr 504. In accordance with one embodiment, the Scheduler 708 assigns time slots for the DRAMCtrl 702 and FlashCtrl 704 operation based on the current status and the pending command received or to be received from the MCH. The DMgrCtrl 710 generates and sends appropriate control information and control signals for the proper operation and control of the data transfer fabric to enable or disable data paths between Flash 506, DRAM 508, and the MCH 510.

[0093] FIG. 8A is a block diagram showing a Flash-DRAM hybrid DIMM (FDHDIMM) 801. As seen from FIG. 8A, this Flash-DRAM hybrid DIMM requires two separate and independent address buses to separately control the address spaces: one for the Flash memory Flash 803 and the other for the DRAM memory DRAM 805. The MCH 810 treats the DRAM 805 and Flash 803 as separate memory subsystems, for example DRAM and SSD/HD memory subsystems. The memory in each address space is controlled directly by the MCH. However, the on-DIMM data path 807 between Flash 803 and DRAM 805 allows for direct data transfer to occur between the Flash 803 and the DRAM 805 in response to control information from Ctrl 830. In this embodiment, this data transfer mechanism provides direct support for executing commands from the MCH without having the MCH directly controlling the data transfer, and thus improving data transfer performance from Flash 803 to the DRAM 805. However, the MCH needs to manage two address spaces and two different memory protocols simultaneously. Moreover, the MCH needs to map the DRAM memory space into the Flash memory space, and the data interface time suffers due to the difference in the data access time between the Flash memory and the DRAM memory.

[0094] In accordance with one embodiment, a memory space mapping of a Flash-DRAM hybrid DIMM is shown in FIG. 8B. A memory controller of a host system (not shown) controls both of the DRAM 508 address space and the Flash 506 address space using a single unified address space. The CDC 502 receives memory access commands from the MCH and generates control information for appropriate mapping and data transfer between Flash and DRAM memory subsystem to properly carry out the memory access commands. In one embodiment, the memory controller of the host system views the large Flash memory space as a DRAM memory space, and accesses this unified memory space with a standard DDR (double data rate)

protocol used for accessing DRAM. The unified memory space in this case can exhibit overlapping memory address space between the Flash 506 and the DRAM 508. The overlapping memory address space may be used as a temporary storage or buffer for data transfer between the Flash 506 and the DRAM 508. For example, the DRAM memory space may hold a copy of data from the selected Flash memory space such that the MCH can access this data normally via DDR memory access commands. The CDC 502 controls the operation of the Flash 506 and DRAM 508 memory subsystems in response to commands received from a memory controller of a host system.

[0095] In one embodiment, the unified memory space corresponds to a contiguous address space comprising a first portion of the address space of the Flash 506 and a first portion of the address space of the DRAM 508. The first portion of the address space of the Flash 506 can be determined via a first programmable register holding a first value corresponding to the desired Flash memory size to be used. Similarly, the first portion of the address space of the DRAM 508 can be determined via a second programmable register holding a second value corresponding to the desired DRAM memory size to be used. In one embodiment, any one of the first portion of the address space of the Flash 506 and the first portion of the address space of the DRAM 508 is determined via a first value corresponding to a desired performance or memory size, the first value being received by the CDC 502 via a command sent by memory controller of the host system.

[0096] In accordance with one embodiment, a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM is shown in Fig. 9. In certain embodiments, data transfer from the Flash 506 to the DRAM 508 occurs in

accordance with memory access commands which the CDC 502 receives from the memory controller of the host system. In certain embodiments, the CDC 502 controls the data transfer from the DRAM 508 to the Flash 506 so as to avoid conflict with any memory operation that is currently being executed. For example, when all the pages in a particular DRAM memory block are closed. The CDC 502 partitions the DRAM memory space into a number of blocks for the purpose of optimally supporting the desired application. The controller can configure memory space in the memory module based on at least one of one or more commands received from the MCH, instructions received from the MCH, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value. Furthermore, the block size can be configurable by the memory controller of the host system, such that the number pages in a block can be optimized to support a particular application or a task. Furthermore, the block size may be configured on-the-fly, e.g. CDC 502 can receive instruction regarding a desired block size from the memory controller via a memory command, or via a programmable value.

[0097] In certain embodiments, a memory controller can access the memory module using a standard access protocol, such as JEDEC's DDR DRAM, by sending a memory access command to the CDC 502 which in turn determines what type of a data transfer operation it is and the corresponding target address where the data information is stored, e.g. data information is stored in the DRAM 508 or Flash 506 memory subsystems. In response to a read operation, if the CDC 502 determines that data information, e.g. a page (or block), does not reside in the DRAM 508 but resides in Flash 506, then the CDC 502 initiates and controls all necessary data transfer operations from Flash 506 to DRAM 508 and subsequently to the memory controller. In one

embodiment, once the CDC 502 completes the data transfer operation of the requested data information from the Flash 506 to the DRAM 508, the CDC 502 alerts the memory controller to retrieve the data information from the DRAM 508. In on embodiment, the memory controller initiates the copying of data information from Flash 506 to DRAM 508 by writing, into a register in the CDC 502, the target Flash address along with a valid block size. The CDC 502 in turn, executes appropriate operations and generates control information to copy the data information to the DRAM 508. Consequently, the memory controller can access or retrieve the data information using standard memory access commands or protocol.

[0098] An exemplary flow chart is shown in FIG. 9, a starting step or power up 902, is followed by an initialization step 904, the memory controller initiates, at step 906, a data move from the Flash 506 to the DRAM 508 by writing target address and size, to a control register in the CDC 502, which then copies, at 908, data information from the Flash 506 to the DRAM 508 and erases the block in the Flash. Erasing the data information from Flash may be accomplished independently from (or concurrently with) other steps that CDC 502 performs in this flow chart, i.e. other steps can be executed concurrently with the Erase the Flash block step. Once the data information or a block of data information is thus moved to the DRAM 508, the memory controller can operate on this data block using standard memory access protocol or commands at 910. The CDC 502 checks, at 912, if any of the DRAM 508 blocks, or copied blocks, are closed. If the memory controller closed any open blocks in DRAM 508, then the CDC 502 initiate a Flash write to write the closed block from the DRAM 508 to the Flash 506, at 914. In addition, the memory controller, at 916, reopens the closed block that is currently being written into the Flash 506, then the CDC 502 stops the Flash write operation and erases the Flash block which

was being written to, as shown at 918. Otherwise, the CDC 502 continues and completes the writing operation to the Flash at 920.

[0099] The dashed lines in FIG. 9 indicate independent or parallel activities that can be performed by the CDC 502. At any time the CDC 502 receives a DRAM load command from a memory controller which writes a Flash target address and/or block size information into the RC register(s) at 922, as described above, then the CDC 502 executes a load DRAM w/RC step 906 and initiates another branch (or a thread) of activities that includes steps 908 – 922. In one embodiment, the CDC 502 controls the data transfer operations between DRAM 508 and Flash 506 such that the Flash 506 is completely hidden from the memory controller. The CDC 502 monitors all memory access commands sent by the memory controller using standard DRAM protocol and appropriately configures and manipulate both Flash 506 and DRAM 508 memory subsystems to perform the requested memory access operation and thus achieve the desired results. The memory controller does not interface directly with the Flash memory subsystem. Instead, the memory controller interfaces with the CDC 502 and/or DMgr 504 as shown in Fig. 5 and Fig. 6. Moreover, the memory controller may use one or more protocol, such as DDR, DDR2, DDR3, DDR4 protocols or the like.

[00100] In accordance with one embodiment, an example of mapping a DRAM address space to Flash memory address space is shown in FIG. 10. Two sets (1002, 1004) of address bits AD6 to AD17, forming a 24 bit extended memory page address, are allocated for the block address. For example, assuming a Block size of 256K Bytes, then a 24-bit block address space (using the two sets of AD6 to AD17 1002 and 1004) would enable access to 4TB of Flash memory storage space. If a memory module has 1GB of DRAM storage capacity, then it can hold approximately

4K Blocks of data in the DRAM memory, each Block comprise 256 K Bytes of data. The DRAM address space, corresponding to the 4K blocks, can be assigned to different virtual ranks and banks, where the number of virtual ranks and banks is configurable and can be manipulated to meet a specific design or performance needs. For example, if a 1G Bytes memory module is configured to comprise two ranks with eight banks per rank, then each bank would hold two hundred fifty (250) blocks or the equivalent of 62 M Bytes or 62K pages, where each page correspond to a 1K Bytes. Other configurations using different page, block, banks, or ranks numbers may also be used. Furthermore, an exemplary mapping of 24-bit DDR DIMM block address to Flash memory address, using Block addressing as described above, is shown in Fig. 10. The 24-bit can be decomposed into fields, such as a logical unit number LUN address 1060 field, a Block address 1050 field, a Plane address 1040, a Page address 1030, and a group of least significant address bits A_0A_1 1020. The Plane address 1040 is a sub address of the block address, and it may be used to support multiple page IO so as to improve Flash memory subsystem operation. In this example, it is understood that different number of bits may be allocated to each field of the 24-bit

[00101] The CDC 502 manages the block write-back operation by queuing the blocks that are ready to be written back to the Flash memory. As described above, if any page in a queued block for a write operation is reopened, then the CDC 502 will stop the queued block write operation, and remove the block from the queue. Once all the pages in a block are closed, then the CDC 502 restarts the write-back operation and queue the block for a write operation.

[00102] In accordance with one embodiment, an exemplary read operation from Flash 506 to DRAM 508 can be performed in approximately 400μs, while a write operation from DRAM 508

to Flash 506 can be performed in approximately 22ms resulting in a read to write ratio of 55 to 1. Therefore, if the average time a host system's memory controller spends accessing data information in a Block of DRAM is about 22ms (that is the duration that a Block comprises one or more pages that are open), then the block write-back operation from DRAM to Flash would not impact performance and hence the disparity between read and write access may be completely hidden from the memory controller. If the block usage time is 11ms instead of 22ms, then the CDC 502 control the data transfer operation between DRAM 508 and Flash 506 such that there are no more than 9 closed blocks in the queue to be written-back to the Flash memory, hence approximately an average of 100ms can be maintained for a standard DDR DRAM operation. Moreover, the number of closed Blocks in the queue to be written-back to the Flash memory subsystem varies with the average block usage time and the desired performance for a specific host system or for a specific application running using the host system resources.

[00103] Consequently, the maximum number of closed Blocks to be written-back to Flash can be approximated to be

((#of blocks per bank)/(ratio of 'Flash_block_write_time' to 'Flash_read_time'))*(
(Block usage time)/('Flash_block_write_time'))

[00104] In order to maintain less than 100ms time period for queued write-back Blocks, then using a Flash memory subsystem having 22ms write access time per Block would results in a maximum number of four Blocks to be queued for write operation to Flash 506. Therefore, on average approximately 88ms (= 22ms * 4) for blocks means that each bank should not have more than four Blocks that need to be written back to the Flash 506.

[00105] The above equation also indicates that bigger DRAM memory space can support shorter block usage times. For example, 2GB of DRAM memory allows the 8 closed blocks to be written-back to Flash. The table in FIG. 11 provides an estimation of the maximum allowed closed blocks in the queue to be written back to the Flash memory for different DRAM density using various average block use time.

[00106] While embodiments and applications have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts disclosed herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

CLAIMS

What is claimed is:

1. A memory module comprising:

a data manager configured to be coupled to a memory controller of a host system using a data bus, the data manager is operable to communicate data signals with the memory controller of the host system by way of the data bus in accordance with a first protocol;

a first volatile memory subsystem coupled to the data manager using a first data bus, the first volatile memory subsystem is operable to communicate data signals with the data manager by way of the first data bus in accordance with the first protocol;

a second volatile memory subsystem coupled to the data manager using a second data bus, the second volatile memory subsystem is operable to communicate data signals with the data manager by way of the second data bus in accordance with the first protocol;

a non-volatile memory subsystem coupled to the data manager using a third data bus, the non-volatile memory subsystem is operable to communicate data signals with the data manager by way of the third data bus using a second protocol; and

a controller operable to receive one or more commands from the memory controller of the host system in accordance with the first protocol, and in response to the one or more commands received from the memory controller of the host system, the controller generates and transmits one or more control signals to the data manager, wherein, in response to the one or more control signals, the data manager transfers data between the first volatile memory subsystem and the memory controller of the host system1 and transfers data signals from the non-volatile memory subsystem to the second volatile memory subsystem by way of the third data bus and the second data bus.

ABSTRACT

A memory module that is couplable to a memory controller hub (MCH) of a host system includes a non-volatile memory subsystem, a data manager coupled to the non-volatile memory subsystem, a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager, and a controller operable to receive read/write commands from the MCH and to direct transfer of data between any two or more of the MCH, the volatile memory subsystem, and the non-volatile memory subsystem based on the commands.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Information Disclosure Statement

Commissioner:

Listed on accompanying IDS Forms PTO/SB/08a equivalent and PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA),. No statement or fee is required.

Copies of documents **FP1-FP4** are submitted herewith. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of U.S. patents and patent application publications cited as documents **US1-US141** on the attached IDS Forms are submitted.

A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

Document **US139** (9,361,250 B2) is submitted herewith as an English-language counterpart to document **FP2** (CN 102110057 A).

Document **US119** (7,519,754 B2) is submitted herewith as an English-language counterpart to document **FP3** (CN 101017460 A).

Copies of the **NPL1-NPL72** documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. 14/840,865, filed 08-31-2015 (now pending), which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

It is expected that the examiner will review the prosecution and cited art in the parent application no(s). 14/840,865, filed 08-31-215 (now pending); 14/489,269, filed 09-17-2014 (now U.S. Pat. No. 9,158,685); 13/559,476, filed 07-26-2012 (now now U.S. Pat. No. 8,874,831); 12/240,916, filed 09-29-2008 (now now U.S. Pat. No. 8,301,833); and 12/131,873, filed 06-02-2008 (now abandoned) in accordance with MPEP 2001.06(b), and indicate in the next communication

from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending, commonly assigned U.S. Patent Applications as documents **NPL36-NPL43** and **NPL45-NPL56**.

The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

Respectfully submitted,

SHAMI MESSINGER PLLC

Dated: 03-23-2018

/ Khaled Shami /
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
Tel: 202-516-6902

Equivalent of Form PTO/SB/08a (07-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	Filed herewith
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
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				Examiner Name	To be assigned
Sheet	1	of	8	Attorney Docket Number	0016.001000G

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	NPL14	File History for Application No. 12/240,916, filed September 29, 2008, 320 pages.	
	NPL15	File History for Application No. 13/905,048 filed May 29, 2013, 181 pages.	
	NPL16	File History for Provisional Application 60/941,586, filed June 1, 2007, 23 pages.	
	NPL17	File History US Patent No. 8,671,243	
	NPL18	Final Office Action, dated June 15, 2016, issued in U.S. Patent Application No. 14/489,281, 10 pages.	
	NPL19	Horowitz, P. et al., "The Art of Electronics", Cambridge Univesity Press 2nd Ed. 1989, pp. 471, 495-496.	
	NPL20	Innis, J., "MPC8560 PowerQUICC Ill Compact Flash Interface Design", Freescale Semiconductor, Inc., 2004-2006, pp. D 1-23.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	Filed herewith
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	To be assigned
				Examiner Name	To be assigned
Sheet	3	of	8	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL21	Intel 1.8 Volt Intel StrataFlash Wireless Memory (L18).	
	NPL22	International Preliminary Report on Patentabillity in PCT/US12/48750, mailed April 3, 2014, pp.1-8.	
	NPL23	International Search Report and Written Opinion in PCT/US12/48750, dated October 10, 2012 pp.1-10.	
	NPL24	Jacob, B., "Memory Systems Cache, DRAM, Disk", Morgan Kaufman Publishers, Burlington, MA, 2008, Preface and Ch. 7 pp. 315-322.	
	NPL25	Jandhyala, S. et al., "Design-For-Test Analysis of a Buffered SDRAM DIMM", Semiconductor Group, Texas Instruments, Proceedings of International Workshop in Memory Technology, Design and Testing, Singapore, August 13014, 1996, 15 pages.	
	NPL26	JEDEC Standard 21-C, "Configurations for Solid State Memories," pp. 4.5.5-1 to 4.5.5-18.	
	NPL27	JEDEC Standard, "Configurations for Solid State Memories", JEDEC Standard 21-C, Release 9, August 1999, 114 pages.	
	NPL28	JEDEC STANDARD, DDR2 SDRAM Specification, JESD79-2B (Revision of JESD79-2A) January 2005, 113 pages.	
	NPL29	JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79, June 2000, 77 pages.	
	NPL30	JEDEC Standard, Double Data Rate (DDR): SDRAM Specification: JESD79C (Revision JESD79B), March 2003, pp.1-75.	

Examiner Signature		Date Considered	

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Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	Filed herewith
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	To be assigned
				Examiner Name	To be assigned
Sheet	4	of	8	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL31	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification:JESD205, JEDEC SOLID STATE TECH. ASSOC., March 2007, pp. 1-129.	
	NPL32	MetaRAM Develops New Technology That Quadruples Memory Capacity of Servers and Workstations; Reduces Price by Up to 90 Percent", Press Release provided by MetaRAM and published on MarketWired.com, February 25,2008, 3 pages.	
	NPL33	Microsoft Computer Dictionary Fifth Edition, 9 pages.	
	NPL34	Microsoft Windows 2000 Professional Resource Kit, 76 pages.	
	NPL35	Mutnuary, B. et al., "Analysis of Fully Buffered DIMM Interface in High-speed Server Applications", IBM Corp, xSeries eServer Development, 2006 Electronic Components and Technology Conference, pp. 203-208.	
	NPL36	Notice of Allowance in U.S. Application No. 12/240,916, mailed on September 17, 2012.	
	NPL37	Notice of Allowance in U.S. Patent Application No. 13/536,173, mailed July 2, 2013.	
	NPL38	Notice of Allowance in U.S. Patent Application No. 13/559,476, mailed May 6, 2014.	
	NPL39	Notice of Allowance in U.S. Patent Application No. 13/559,476, mailed September 29 ,2014.	
	NPL40	Notice of Allowance in U.S. Patent Application No. 13/905,048, mailed December 19,2013, 8 pages.	

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	Filed herewith
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	To be assigned
				Examiner Name	To be assigned
Sheet	5	of	8	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL41	Notice of Allowance in U.S. Patent Application No. 13/905,053, mailed December 11, 2013.	
	NPL42	Notice of Allowance in U.S. Patent Application No. 14/173,219 dated July 7, 2014.	
	NPL43	Notice of Allowance in U.S. Patent Application No. 14/489,269, mailed October 8, 2015.	
	NPL44	Office Action dated August 19, 2016 of the Chinese Patent Application No. 201280047758.X	
	NPL45	Office Action in U.S. Application No. 13/536,176, mailed on April 15, 2013.	
	NPL46	Office Action in U.S. Patent Application No. 12/240,916, mailed April 3, 2012 pp.1-12.	
	NPL47	Office Action in U.S. Patent Application No. 12/240,916, mailed February 1, 2012 pp 1-14.	
	NPL48	Office Action in U.S. Patent Application No. 12/240,916, mailed July 29, 2011 pp.1-8.	
	NPL49	Office Action in U.S. Patent Application No. 13/536,173, mailed April 15, 2013.	
	NPL50	Office Action in U.S. Patent Application No. 13/625,563, mailed August 5, 2013.	

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Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	Filed herewith
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	To be assigned
				Examiner Name	To be assigned
Sheet	6	of	8	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL51	Office Action in U.S. Patent Application No. 13/625,563, mailed May 9, 2014.	
	NPL52	Office Action in U.S. Patent Application No. 13/905,048, mailed August 1, 2013.	
	NPL53	Office Action in U.S. Patent Application No. 13/905,053, mailed August 1, 2013.	
	NPL54	Office Action in U.S. Patent Application No. 14/173,219, mailed March 13, 2014, pp.1-7.	
	NPL55	Office Action in U.S. Patent Application No. 14/173,242, mailed March 14, 2014, pp.1-7	
	NPL56	Office Action in U.S. Patent Application No. 14/302,292, mailed December 21, 2015.	
	NPL57	Out of Stealth Mode, Start-Up MetaRAM Unveils New Technology That Quadruples DRAM Capacity, Press Release edited by Storage Newsletter on February 28, 2008 at StorageNewsLetter.com, 8 pages.	
	NPL58	PATTERSON et al., "Computer Organization & Design: The Hardware/Software Interface" Morgan Kaufmann Publishers, Inc. (1998).	
	NPL59	Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SanDisk, Corp.), filed June 20, 2014.	
	NPL60	Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed August 22, 2014.	

Examiner Signature		Date Considered	

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Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	Filed herewith
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	To be assigned
				Examiner Name	To be assigned
Sheet	7	of	8	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL61	Petition for Inter Partes Review of U.S. Patent No. 8,301,833, filed September 29, 2008.	
	NPL62	Petition for Inter Partes Review of U.S. Patent No. 8,516,187 (on behalf of SanDisk, Corp.), filed June 19, 2014.	
	NPL63	Petition for Inter Partes Review of U.S. Patent No. 8,516,187 (on behalf of SMART Modular Technologies, Inc.), filed August 22, 2014.	
	NPL64	Petition for Inter Partes Review of U.S. Patent No. 8,671,243, filed May 29, 2013.	
	NPL65	Petition for Inter Partes Review of U.S. Patent No. 8,874,831, filed July 26, 2012.	
	NPL66	Provisional Application No. 60/912,321 filed April 17, 2007	
	NPL67	Provisional Application No. 60/941,586, filed June 1, 2007	
	NPL68	Restriction Requirement in U.S. Patent Application No. 12/240,916, mailed March 31, 2011.	
	NPL69	Smart Storage Systems, Inc's Invalidity Contentions, Case No. 4:13-cv-05889-YGR, dated June 6, 2014.	
	NPL70	Using Two Chip Selects to Enable Quad Rank, an IP.com Prior Art Database Technical Disclosure, IP.com Electronic Publication: December 17, 2005, 2 pages.	

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Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	Filed herewith
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	To be assigned
				Examiner Name	To be assigned
Sheet	8	of	8	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL71	Webster's II New College Dictionary, Houghton Mifflin Company, Boston, MA, 2001, pp. 259, 1115.	
	NPL72	WONG, A. "The BIOS Optimization Guide", Adrian's Rojak Pot, Rev. 6.2, 1998-2001, 67 pages.	

Examiner Signature		Date Considered	

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Electronic Acknowledgement Receipt

EFS ID:	32144416
Application Number:	15934416
International Application Number:	
Confirmation Number:	2728
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Casey Berger
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000G
Receipt Date:	23-MAR-2018
Filing Date:	
Time Stamp:	16:31:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	WebADS.pdf	176716 468c4bc93bd8e8ca9e5962f6af10478aac8230d7	no	9

Warnings:

Information:					
2	Foreign Reference	FP1_WO2013016723A3.pdf	113970 8f5a6f9d06c1e71e458abf89417629f513c34d9c	no	3
Warnings:					
Information:					
3	Foreign Reference	FP2_CN102110057A.pdf	1045016 6e187325df5133a4000435178aecf3290f016456	no	19
Warnings:					
Information:					
4	Foreign Reference	FP3_CN101017460A.pdf	2764170 65df327c7eb63703b861845b759a12248d2af62a	no	44
Warnings:					
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5	Foreign Reference	FP4_EP2737383A2.pdf	15073 7b332408cc0afbc64143c3ac933ed63e667fd00f	no	1
Warnings:					
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6		0016001000G_APP.pdf	2377527 150ecb0ec855a36fad8327c3fe1b310cbec16a2f	yes	75

Multipart Description/PDF files in .zip description

Document Description	Start	End
Power of Attorney	1	1
Oath or Declaration filed	2	6
Assignee showing of ownership per 37 CFR 3.73	7	8
Drawings-only black and white line drawings	9	18
Specification	19	54
Claims	55	55

	Abstract	56	56
	Information Disclosure Statement (IDS) Form (SB08)	57	75

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000G
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hyun		Lee	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Ladera Ranch	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	21 Thalia Street		
Address 2			
City	Ladera Ranch	State/Province	CA
Postal Code	92694	Country i	US

Inventor 2

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Chi-She		Chen	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Walnut	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	944 Crystal Water Lane		
Address 2			
City	Walnut	State/Province	CA
Postal Code	91789	Country i	US

Inventor 3

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey	C.	Solomon	

PTO/AIA/14 (08-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000G
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Irvine	**State/Province**	CA	**Country of Residence** [i]	US

Mailing Address of Inventor:

Address 1	6 Silver Fir		
Address 2			
City	Irvine	**State/Province**	CA
Postal Code	92604	**Country** [i]	US

Inventor 4

Legal Name

Prefix	**Given Name**	**Middle Name**	**Family Name**	**Suffix**
	Scott	H.	Milton	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Irvine	**State/Province**	CA	**Country of Residence** [i]	US

Mailing Address of Inventor:

Address 1	49 Statehouse Place		
Address 2			
City	Irvine	**State/Province**	CA
Postal Code	92602	**Country** [i]	US

Inventor 5

Legal Name

Prefix	**Given Name**	**Middle Name**	**Family Name**	**Suffix**
	Jayesh		Bhakta	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Cerritos	**State/Province**	CA	**Country of Residence** [i]	US

Mailing Address of Inventor:

Address 1	12220 Rose Street		
Address 2			
City	Cerritos	**State/Province**	CA
Postal Code	90703	**Country** [i]	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

PTO/AIA/14 (08-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000G
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ **An Address is being provided for the correspondence Information of this application.**			
Customer Number	151145		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	FLASH-DRAM HYBRID MEMORY MODULE		
Attorney Docket Number	0016.001000G	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	10	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
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Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	151145		

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					
Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					

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Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	14840865	2015-08-31

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14840865	Continuation of	14489269	2014-09-17	9158684	2015-10-13

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14489269	Continuation of	13559476	2012-07-26	8874831	2014-10-28

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13559476	Claims benefit of provisional	61512871	2011-07-28

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13559476	Continuation in part of	12240916	2008-09-29	8301833	2012-10-30

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000G
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12240916	Continuation of	12131873	2008-06-02

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12131873	Claims benefit of provisional	60941586	2007-06-01

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000G
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000G
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information For Applicant:			
Address 1	175 Technology Drive, Suite 150		
Address 2			
City	Irvine	**State/Province**	CA
Country[i]	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000G
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	Netlist, Inc.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	175 Technology Drive, Suite 150		
Address 2			
City	Irvine	**State/Province**	CA
Country i	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000G
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e. g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/ Khaled Shami /			Date (YYYY-MM-DD)	
First Name	Khaled	Last Name	Shami	Registration Number	38745

Additional Signature may be generated within this form by selecting the Add button.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

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WIPO | PCT

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(71) **Applicant** *(for all designated States except US)*: **NETLIST, INC.** [US/US]; 51 Discovery, Suite 150, Irvine, CA 92618 (US).

(72) **Inventors; and**

(75) **Inventors/Applicants** *(for US only)*: **LEE, Hyun** [US/US]; 21 Thalia Street, Ladera Ranch, CA 92694 (US). **CHEN, Chi-She** [—/US]; 944 Crystal Water Lane, Walnut, CA 91789 (US). **SOLOMON, Jeffrey, C.** [US/US]; 6 Silver Fir, Irvine, CA 92604 (US). **MILTON, Scott** [US/US]; 49 Statehouse Place, Irvine, CA 92602 (US). **BHAKTA, Jayesh** [US/US]; 12220 Rose Street, Cerritos, CA 90703 (US).

(74) **Agents**: **SHAMI, Khaled** et al.; P.O. Box 60610, Palo Alto, CA 94306 (US).

(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH,

[Continued on next page]

(54) **Title**: FLASH-DRAM HYBRID MEMORY MODULE

(57) **Abstract**: A memory module that is couplable to a memory controller hub (MCH) of a host system includes a non- volatile memory subsystem, a data manager coupled to the non- volatile memory subsystem, a volatile memory subsystem coupled to the data manager and operable to exchange data with the non- volatile memory subsystem by way of the data manager, and a controller operable to receive read/write commands from the MCH and to direct transfer of data between any two or more of the MCH, the volatile memory subsystem, and the non- volatile memory subsystem based on the commands.

FIG. 5A

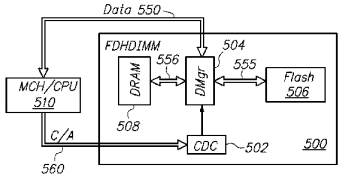
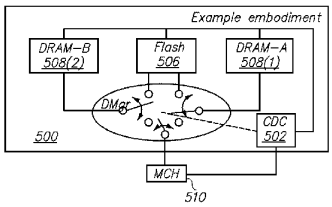


FIG. 5B



WO 2013/016723 A3

GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US12/48750

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 12/00 (2012.01)
USPC - 711/118, 103
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): G06F 12/00, 12/08, 13/16 (2012.01)
USPC: 711/170, 104, 118, 103

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US-G, US-A, EP-A, EP-B, WO, JP-bib, DE-C,B, DE-A, DE-T, DE-U, GB-A, FR-A); DialogPRO; IEEE/IEEEXplore; Google/Google Scholar; IP.com; volatile, non-volatile, memory, controller, manager, performance, frequency, clock, plural, multiple, port, segment, subset

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2008/0104344 A1, (SHIMOZONO, N., et al.), May 1, 2008, figures 19, paragraphs [0017], [0053], [0055], [0057], [0061], [0065], [0067], [0080]	1-6, 9, 11-15, 18-23 ---------- 7, 8, 10, 16, 17, 24
Y	US 2010/0274953 A1, (LEE, T., et al.), October 28, 2010, figures 1, 2, 4B, 10, paragraphs [0005], [0007], [0046], [0053], [0058], [0062], [0065], [0066], [0071], [0080], [0115]	7, 8, 10, 16, 17, 24

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 September 2012 (21.09.2012)	10 OCT 2012
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

(19)中华人民共和国国家知识产权局

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(71)申请人 澜起半导体(上海)有限公司
地址 200233 上海市桂平路680号33幢802室

(72)发明人 山岗 霍华德·杨

(74)专利代理机构 上海翰鸿律师事务所 31246
代理人 李佳铭

(51)Int.Cl.
G06F 12/08(2006.01)

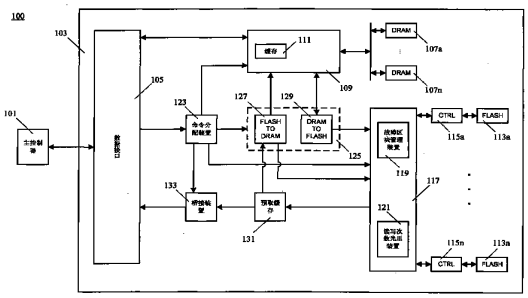
权利要求书 3 页 说明书 9 页 附图 6 页

(54)发明名称

存储器模组及存储器模组内的数据交换方法

(57)摘要

一种存储器模组及存储器模组内的数据交换方法，存储器模组是用于缓存一计算机的CPU和其他装置之间的数据交换。存储器模组包括至少一个易失性存储器装置，至少一个非易失性存储装置，以及数据交换控制装置。数据交换控制装置根据指令控制易失性存储器装置和非易失性存储装置在存储器模组内的数据交换。



CN 102110057 A

1. 一种存储器模组，包括至少一个易失性存储器装置，其特征在于，所述存储器模组还包括：

至少一个非易失性存储装置；以及

数据交换控制装置，根据接收到的指令控制所述易失性存储器装置和所述非易失性存储装置之间在所述存储器模组内的数据交换。

2. 如权利要求 1 所述的存储器模组，其特征在于，当所述数据交换控制装置接收到第一指令时，控制从所述非易失性存储装置读取数据并把这些数据写入所述易失性存储装置。

3. 如权利要求 1 所述的存储器模组，其特征在于，当所述数据交换控制装置接收到第二指令时，控制从所述易失性存储装置读取数据并把这些数据写入所述非易失性存储装置。

4. 如权利要求 1 所述的存储器模组，其特征在于，所述存储器模组用于缓冲计算机的 CPU 与其他装置之间的数据交换。

5. 如权利要求 1 所述的存储器模组，其特征在于，所述易失性存储装置是动态随机存取存储装置。

6. 如权利要求 1 所述的存储器模组，其特征在于，所述非易失性存储装置是闪速存储装置。

7. 如权利要求 1 所述的存储器模组，其特征在于，所述存储器模组还包括一数据接口，所述存储器模组通过该数据接口与外部进行通信，该数据接口是双数据率双面引脚存储器模组数据接口。

8. 如权利要求 1 所述的存储器模组，其特征在于，所述易失性存储器装置和所述非易失性存储装置之间的数据交换不经过控制所述存储器模组的主控制器。

9. 如权利要求 1 所述的存储器模组，其特征在于，它还包括一管理装置，以管理所述非易失性存储装置中的故障区块和管理所述非易失性存储装置各区块的读写次数。

10. 如权利要求 1 所述的存储器模组，其特征在于，它还包括一预取缓存，以缓存从所述非易失性存储装置读出的数据，其中，所述非易失性存储装置平行地连接于所述预取缓存。

11. 如权利要求 1 所述的存储器模组，其特征在于，它还包括命令分配装置，用于判断所述存储器模组接收到的命令，并根据判断结果把接收到的命令分配给所述易失性存储装置或所述非易失性存储装置或所述数据交换控制装置。

12. 如权利要求 12 所述的存储器模组，其特征在于，当所述命令分配装置接收到从所述易失性存储装置读取数据并输出所述存储器模组的命令，或把所述存储器模组接收到的数据写入所述易失性存储装置的命令，命令分配装置把接收到的命令分配给所述易失性存储装置。

13. 如权利要求 12 所述的存储器模组，其特征在于，当所述命令分配装置接收到从所述非易失性存储装置读取数据并输出所述存储器模组的命令，命令分配装置把接收到的命令分配给所述非易失性存储装置。

14. 如权利要求 12 所述的存储器模组，其特征在于，当所述命令分配装置接收到从所述易失性存储装置读取数据并写入所述非易失性存储装置的命令，或从所述非易失性存储

装置读取数据并写入所述易失性存储装置的命令，命令分配装置把接收到的命令分配给所述数据交换控制装置。

15. 如权利要求 1 所述的存储器模组，其特征在于，所述非易失性存储装置的总容量大于所述易失性存储装置的总容量。

16. 如权利要求 1 所述的存储器模组，其特征在于，所述非易失性存储装置和所述易失性存储装置被编址在同一地址空间。

17. 一种计算机存储系统，用于缓存一计算机的处理器和其他装置之间的数据交换，该计算机存储系统包括一个或多个存储器模组以及一个主控制器，该主控制器控制存储器模组与其他装置之间的数据交换，其特征在于，所述存储器模组是如权利要求 1-15 之一所述的存储器模组。

18. 一种存储器模组，用于一计算机，该存储器模组包括至少一个易失性存储装置，其特征在于，该存储器模组还包括至少一个非易失性存储装置，用于存储计算机操作系统，其中，所述易失性存储装置和所述非易失性存储装置之间可在所述存储器模组内进行数据交换。

19. 如权利要求 18 所述的存储器模组，所述易失性存储装置为动态随机存取存储装置，所述非易失性存储装置为闪速存储装置。

20. 一种存储器模组，用于一计算机，该存储器模组包括至少一个易失性存储装置，其特征在于，该存储器模组还包括至少一个非易失性存储装置，当所述计算机从运行状态切换至休眠状态时，在所述存储器模组内，所述易失性存储装置中的相应数据被读取并写入所述非易失性存储装置；当所述计算机从休眠状态切换至运行状态时，在所述存储器模组内，所述非易失性存储装置中的相应数据被读取并写入所述易失性存储装置。

21. 如权利要求 20 所述的存储器模组，所述易失性存储装置为动态随机存取存储装置，所述非易失性存储装置为闪速存储装置。

22. 一种存储器模组内的数据交换方法，该存储器模组用于缓存计算机处理器与其他装置之间的数据交换，该存储器模组包括至少一个易失性存储装置和至少一个非易失性存储装置，该方法包括以下操作：

接收从所述非易失性存储装置读取数据并写入所述易失性存储装置的命令；

从所述非易失性存储装置读取数据；以及

把从所述非易失性存储装置读取的数据写入所述易失性存储装置，其中，从所述非易失性存储装置读取所述数据并写入所述易失性存储装置的操作是在所述存储器模组内进行。

23. 一种存储器模组内的数据交换方法，该存储器模组用于缓存计算机处理器与其他装置之间的数据交换，该存储器模组包括至少一个易失性存储装置和至少一个非易失性存储装置，该方法包括以下操作：

接收从所述易失性存储装置读取数据并写入所述非易失性存储装置的命令；

从所述易失性存储装置读取数据；以及

把从所述易失性存储装置读取的数据写入所述非易失性存储装置，其中，从所述易失性存储装置读取所述数据并写入所述非易失性存储装置的操作是在所述存储器模组内进行。

24. 一种存储器模组，用于缓存计算机处理器与其他装置之间的数据交换，该存储器模组包括至少一个易失性存储装置，其特征在于，该存储器模组还包括至少一个非易失性存储装置，并且该存储器模组被设置成当接收到从所述易失性存储装置读取数据并写入所述非易失性存储装置的命令，从所述易失性存储装置读取数据，并把从所述易失性存储装置读取的数据写入所述非易失性存储装置，其中，从所述易失性存储装置读取所述数据并写入所述非易失性存储装置的操作是在所述存储器模组内进行。

25. 一种存储器模组，用于缓存计算机处理器与其他装置之间的数据交换，该存储器模组包括至少一个易失性存储装置，其特征在于，该存储器模组还包括至少一个非易失性存储装置，并且该存储器模组被设置成当接收到从所述非易失性存储装置读取数据并写入所述易失性存储装置的命令，从所述非易失性存储装置读取数据，并把从所述非易失性存储装置读取的数据写入所述易失性存储装置，其中，从所述非易失性存储装置读取所述数据并写入所述易失性存储装置的操作是在所述存储器模组内进行。

存储器模组及存储器模组内的数据交换方法

【技术领域】

[0001] 本申请的一方面是有关一种存储器模组及存储器模组内的数据交换方法，尤其是有关一种包括易失性存储装置和非易失性存储装置的存储器模组。

【背景技术】

[0002] 存储器大致可分为易失性存储器(volatile memory)和非易失性存储器(non-volatilememory)。易失性存储器包括动态随机存取存储器(DRAM)和静态随机存取存储器(SRAM)等，具有存取速度快的优点，但由于工作时需要持续为其供电否则将导致存储于其内的数据丢失，因而具有较高的功耗。非易失性存储器包括闪速存储器(FLASH memory)，相比易失性存储器具有高集成度的优点，即单位体积存储密度高，并且由于断电不会导致存储于其内的数据丢失而具有较低的功耗。非易失性存储器的存取速度低于易失性存储器，高于机械式硬盘。

[0003] 目前，被用于计算机存储系统的主要是易失性存储器，如DRAM。而非易失性存储器，如FLASH，则越来越多地被用于通过I/O接口存取的外部存储设备，比如固态硬盘(solid statedisk)或U盘等。

【发明内容】

[0004] 一方面，在计算机系统中通过I/O接口与存储系统进行数据交换一般需要经过多次数据格式转换，比如外部设备的数据格式与I/O接口的数据格式之间的转换，以及I/O接口的数据格式与存储系统的数据格式之间的转换等，因此，外部设备与存储系统之间的数据交换过程比较复杂并且会消耗较大的系统资源。

[0005] 另一方面，存储系统是由系统中各设备所共享，一个外部设备，如固态硬盘，若要与存储系统进行数据交换就需要跟其他设备进行竞争。而连接于I/O接口的外部设备的优先级一般较低，在竞争中处于劣势，这样将使外部设备中的一些重要数据无法及时送至存储系统而降低了整个系统的效率。

[0006] 又一方面，通过I/O接口与存储系统进行数据交换需要由中央处理器(CPU)进行调度，而这又进一步的消耗了CPU的资源。

[0007] 又一方面，通过I/O接口与存储系统进行数据交换需要由主控制器参与，这会消耗主控制器的资源。

[0008] 又一方面，当计算机处于休眠状态时，存储系统中仍存储着大量数据，为保持这些数据不丢失，系统必须为存储系统一直供电，而这将进一步增加系统的功耗；若将这些数据在计算机休眠时存储于连接于I/O接口的硬盘的话，由于I/O接口与存储系统之间的数据交换速度较慢，将导致恢复系统的时间较长。

[0009] 发明人意识到由于I/O接口传输速率的瓶颈以及I/O接口与存储系统之间的数据交换的复杂机制，非易失性存储器，如FLASH，远高于传统机械式硬盘存取速度的优势并未得到充分利用。

[0010] 本申请的一方面提供了一种存储器模组(memory module),该存储器模组包括至少一个易失性存储装置、至少一个非易失性存储装置以及数据交换控制装置。该数据交换控制装置根据接收到的指令控制易失性存储器装置和非易失性存储装置在该存储器模组内的数据交换。

[0011] 在一些实施例中,当数据交换控制装置接收到第一指令时,控制从非易失性存储装置读取数据并把这些数据写入易失性存储装置;当数据交换控制装置接收到第二指令时,控制从易失性存储装置读取数据并把这些数据写入非易失性存储装置。

[0012] 在一些实施例中,存储器模组用于缓存一计算机处理器,如 CPU,和其他装置,如通过 I/O 接口连接于该计算机的装置,之间的数据交换。

[0013] 在一些实施例中,存储器模组是由一主控制器控制,主控制器与处理器和存储器模组直接连接。

[0014] 在一些实施例中,存储器模组的易失性存储装置用于存储计算机处理器正在使用的数据。

[0015] 易失性存储器包括但不限于动态随机存取存储装置 (DRAM)、静态随机存取存储装置 (SRAM) 等。非易失性存储器包括但不限于闪速存储装置 (FLASH)、铁电随机存取存储装置 (FRAM)、相变随机存取存储装置 (PCRAM) 等。

[0016] 在一些实施例中,存储器模组是安装在一块印刷电路板上的至少一个存储装置的总成。

[0017] 在一些实施例中,计算机可以包括一个以上处理器。

[0018] 该存储器模组包括一个数据接口,该存储器模组通过该数据接口与其他装置进行数据交换。在一些实施例中,该数据接口为双数据率 (DDR,double data rate) 接口;在又一实施例中,该存储器模组数据接口为 RAMBUS 存储器模组接口。

[0019] 在一些实施例中,易失性存储装置和非易失性存储装置之间的数据交换可以是单向的,如自非易失性存储装置至易失性存储装置,或自易失性存储装置至非易失性存储装置。在又一实施例中,易失性存储装置和非易失性存储装置之间的数据交换可以是双向的。其中,易失性存储装置和非易失性存储装置之间的数据交换不经过控制各存储器模组和其他装置之间数据交换的主控制器。

[0020] 在一些实施例中,存储器模组对应每一非易失性存储装置设有非易失性存储装置控制器,以控制对应的非易失性存储装置。

[0021] 在一些实施例中,存储器模组还包括易失性存储装置控制器,以控制易失性存储装置。

[0022] 在一些实施例中,存储器模组还包括故障区块管理装置,以管理非易失性存储装置中的故障区块。

[0023] 在一些实施例中,存储器模组还包括读写次数管理装置,以使非易失性存储装置中各区块的读写次数尽量平均,从而提高非易失性存储装置的使用寿命。

[0024] 在一些实施例中,存储器模组还包括一个预取缓存,以缓存由非易失性存储装置读出的数据。在一些实施例中,复数个非易失性存储装置并行地连接于预取缓存,以提高数据读取速度。

[0025] 在一些实施例中,存储器模组还包括一个命令分配装置。命令分配装置把从存储

器模组外部接收到的命令分配给对应的装置。在一些实施例中，当命令分配装置接收到向易失性存储装置写入从存储器模组外部接收到的数据的命令时，把接收到的写命令分配给易失性存储装置控制器。当命令分配装置接收到由易失性存储器读出数据至其他设备时，把接收到的读命令分配给易失性存储装置控制器。当命令分配装置接收到从非易失性存储装置读取数据至数据接口的命令时，命令分配装置把接收到的命令分配给非易失性存储装置。当命令分配装置接收到从易失性存储装置读取数据并写入非易失性存储装置的命令时，把接收到的命令分配给数据交换控制装置。接着，数据交换控制装置产生一个读命令至易失性存储装置，产生一个写命令至非易失性存储装置。当命令分配装置接收到从非易失性存储装置读取数据并写入易失性存储装置的命令时，把接收到的命令分配给数据交换控制装置。接着，数据交换控制装置产生一个读命令至非易失性存储装置，产生一个写命令至易失性存储装置。

[0026] 本申请的又一方面提供了一种计算机存储系统，用于缓存一计算机内的 CPU 和其他装置之间的数据交换。该存储系统包括一个或多个存储器模组以及一个主控制器。该主控制器控制存储器模组与其他装置之间的数据交换。该存储器模组包括至少一个易失性存储器装置、至少一个非易失性存储装置以及数据交换控制装置。该数据交换控制装置根据接到的指令控制该至少一个易失性存储器装置和该至少一个非易失性存储装置在该存储器模组内的数据交换。存储器模组内易失性存储器装置和非易失性存储装置之间的数据交换不经过主控制器。

[0027] 在一些实施例中，主控制器可以是一个独立的装置，也可以是集成在计算机处理器中。

[0028] 本申请的又一方面提供了一种存储器模组，用于缓存计算机处理器与其他装置之间的数据交换。该存储器模组包括至少一个易失性存储器装置、至少一个非易失性存储装置以及数据交换控制装置。该数据交换控制装置根据接到的指令控制该至少一个易失性存储器装置和该至少一个非易失性存储装置在该存储器模组内的数据交换。

[0029] 本申请的又一方面提供了一种存储器模组，用于计算机系统，该存储器模组包括至少一个易失性存储装置和至少一个非易失性存储装置。其中，非易失性存储装置可用于当计算机系统处于关机或休眠状态时存储计算机程序，易失性存储装置可用于运行这些计算机程序。

[0030] 本申请的又一方面提供了一种存储器模组，用于计算机系统，该存储器模组包括至少一个易失性存储装置和至少一个非易失性存储装置。其中，非易失性存储装置可用于当计算机系统从运行状态切换休眠状态时，存储至少部分易失性存储装置中的数据。

[0031] 在一些实施例中，存储器模组是双面引脚存储器模组 (dual-in-line memory module)。

[0032] 在一些实施例中，存储器模组为双数据率双面引脚存储器模组。

[0033] 在一些实施例中，非易失性存储装置的总容量大于等于易失性存储装置的总容量。

[0034] 本申请的又一方面提供了一种存储器模组内的数据读写方法，该存储器模组包括至少一个易失性存储装置和至少一个非易失性存储装置，该方法包括以下操作：接收来自主控制器的把非易失性存储装置中的数据读出并写入易失性存储装置的指令；自非易失性

存储装置读出这些数据；以及把这些数据写入易失性存储装置。

[0035] 在一些实施例中，这些数据在从非易失性存储装置中读出到写入易失性存储装置的过程不经过主控制器。在又一实施例中，这些数据在从非易失性存储装置中读出到写入易失性存储装置的过程在存储器模组内进行。在又一实施例中，这些数据在从非易失性存储装置中读出到写入易失性存储装置的过程不经过存储器模组对外的接口。

[0036] 在一些实施例中，存储器模组还包括缓存，方法还包括以下操作：把自非易失性存储装置读出这些数据存储在缓存中；以及把缓存中的这些数据写入易失性存储装置。

[0037] 本申请的又一方面提供了一种存储器模组内的数据读写方法，该存储器模组包括至少一个易失性存储装置和至少一个非易失性存储装置，该方法包括以下操作：接收来自主控制器的把易失性存储装置中的数据读出并写入非易失性存储装置的指令；自易失性存储装置读出这些数据；以及把这些数据写入非易失性存储装置。其中，这些数据在从易失性存储装置中读出到写入非易失性存储装置的过程中不经过主控制器。

[0038] 在一些实施例中，存储器模组还包括缓存，方法还包括以下操作：把自易失性存储装置读出这些数据存储在缓存中；以及把缓存中的这些数据写入非易失性存储装置。

[0039] 在一些实施例中，这些数据在从易失性存储装置中读出到写入非易失性存储装置的过程不经过主控制器。在又一实施例中，这些数据在从易失性存储装置中读出到写入非易失性存储装置的过程在存储器模组内进行。在又一实施例中，这些数据在从易失性存储装置中读出到写入非易失性存储装置的过程不经过存储器模组对外的接口。

[0040] 本申请的又一方面提供了一种存储器模组，用于一计算机，该存储器模组包括至少一个易失性存储装置，该存储器模组还包括至少一个非易失性存储装置，用于存储计算机操作系统，其中，易失性存储装置和非易失性存储装置可在存储器模组内进行数据交换。

[0041] 本申请的又一方面提供了一种存储器模组，用于一计算机，该存储器模组包括至少一个易失性存储装置，该存储器模组还包括至少一个非易失性存储装置，当计算机从运行状态切换至休眠状态时，在存储器模组内，易失性存储装置中的相应数据被读取并写入非易失性存储装置；当计算机从休眠状态切换至运行状态时，在存储器模组内，非易失性存储装置中的相应数据被读取并写入易失性存储装置。

[0042] 本申请的又一方面提供了一种存储器模组内的数据交换方法，该存储器模组用于缓存计算机的 CPU 与其他装置之间的数据交换，该存储器模组包括至少一个易失性存储装置和至少一个非易失性存储装置，该方法包括以下操作：接收从非易失性存储装置读取数据并写入所述易失性存储装置的命令；从非易失性存储装置读取数据；以及把从非易失性存储装置读取的数据写入易失性存储装置，其中，从非易失性存储装置读取数据并写入易失性存储装置的操作是在存储器模组内进行。

[0043] 本申请的又一方面提供了一种存储器模组内的数据交换方法，该存储器模组用于缓存计算机的 CPU 与其他装置之间的数据交换，该存储器模组包括至少一个易失性存储装置和至少一个非易失性存储装置，该方法包括以下操作：接收从易失性存储装置读取数据并写入非易失性存储装置的命令；从易失性存储装置读取数据；以及把从易失性存储装置读取的数据写入非易失性存储装置，其中，从易失性存储装置读取数据并写入非易失性存储装置的操作是在存储器模组内进行。

[0044] 本申请的又一方面提供了一种存储器模组，用于缓存计算机处理器与其他装置之

间的数据交换。该存储器模组包括至少一个易失性存储装置和至少一个非易失性存储装置。该存储器模组被设置成当接收到从易失性存储装置读取数据并写入非易失性存储装置的命令，从易失性存储装置读取数据，并把从易失性存储装置读取的数据写入非易失性存储装置，其中，从易失性存储装置读取数据并写入非易失性存储装置的操作是在存储器模组内进行。

[0045] 本申请的又一方面提供了一种存储器模组，用于缓存计算机处理器与其他装置之间的数据交换，该存储器模组包括至少一个易失性存储装置和至少一个非易失性存储装置。该存储器模组被设置成当接收到从非易失性存储装置读取数据并写入易失性存储装置的命令，从非易失性存储装置读取数据，并把从非易失性存储装置读取的数据写入易失性存储装置，其中，从非易失性存储装置读取数据并写入易失性存储装置的操作是在存储器模组内进行。

[0046] 本申请的设计可以在一定程度上减轻计算机系统中 CPU 和主控制器的负担，提高计算机系统开关机速度以及在运行状态和休眠状态之间的切换的速度，以及降低存储系统的功耗。

【附图说明】

[0047] 以下附图为本申请的一部分，结合以下附图可以更好地理解本申请。以下附图展示了本申请的一些实施例，以帮助技术人员更好地理解本申请的原理。在参考以下具体实施方式后，业界一般技术人员在本申请的启示下可以本申请的范围内得到更多其它实施例，并且理解本申请的其他优势。

[0048] 图 1 展示了本申请一个实施例中存储系统的功能模块图。

[0049] 图 2 展示了本申请一个实施例中把从主控制器接收到的数据写入易失性存储装置的方法的流程图。

[0050] 图 3 展示了本申请一个实施例中从易失性存储装置读取数据至主控制器的方法的流程图。

[0051] 图 4 展示了本申请一个实施例中从非易失性存储装置读取数据并写入易失性存储装置的方法的流程图。

[0052] 图 5 展示了本申请一个实施例中从易失性存储装置读取数据并写入非易失性存储装置的方法的流程图。

[0053] 图 6 展示了本申请一实施例中从非易失性存储装置读取数据至主控制器的方法的流程图。

【具体实施方式】

[0054] 以下将对本申请的具体实施例进行详细描述，并且这些描述将详细到使业界一般技术人员能够理解本申请。可以理解，除了本申请描述的具体实施例外，还可以在本申请的精神下和范围内通过改变结构、逻辑以及电路以获得其他实施方案，这些实施方案依然在本申请的保护范围之内。在描述以下具体实施例的过程中，为了对这些具体实施例进行清楚的描述，将采用一些特定的术语，然而采这些术语的本意并非限制本申请的保护范围，这些术语的范围应该扩展至任何以大致相同的手段达到大致相同的目的的等效物。比如“连

接”一词，不仅包括直接连接，还包括通过其他电路连接。

[0055] 图 1 展示了本申请一个实施例中存储系统 100 的功能模块图。存储系统 100 可用于缓存 CPU（图中未示）与其他装置之间的数据交换。存储系统 100 包括主控制器 101 和存储器模组 103。为便于说明，图 1 所示的实施例中只展示了一个存储器模组，但可以理解的是，一个存储系统中可以包括任意个存储器模组，比如 2 个、3 个、4 个、6 个等。

[0056] 主控制器 101 控制对存储器模组 103 的读写操作。

[0057] 存储器模组 103 包括数据接口 105，存储器模组 103 通过数据接口 105 与外部进行数据交换。在一些实施例中，数据接口 105 符合 DDR DIMM（双数据率双列直插存储器模组）的数据接口标准，比如 DDR-1、DDR-2 或 DDR-3 等。在一些实施例中，数据接口 105 符合 RAMBUS 存储器模组的数据接口标准。

[0058] 存储器模组 103 包括多个动态随机存取存储装置 107a-107n 和动态随机存取存储装置控制器 109。动态随机存取存储装置控制器 109 控制对动态随机存取存储装置 107a-107n 的读写操作。在一些实施例中，动态随机存取存储装置控制器 109 包括缓存 111，用以缓存写入动态随机存取存储装置 107a-107n 的数据和 / 或从动态随机存取存储装置 107a-107n 读出的数据。

[0059] 存储器模组 103 还包括多个闪速存储装置 113a-113n，并且对应每一闪速存储装置 113a-113n 设有闪速存储装置控制器 115a-115n，用以控制对对应的闪速存储装置的读写操作。

[0060] 存储器模组 103 还包括管理装置 117，以优化对闪速存储装置 113a-113n 的使用。管理装置 117 包括故障区块管理装置 119 和读写次数管理装置 121。故障区块管理装置 119 检测闪速存储装置 113a-113n 中的故障区块，并防止系统再次使用这些故障区块。读写次数管理装置 121 均化对各闪速存储装置各区块的读写次数，防止系统对某些区块进行读写的次数远高于其他区块而使这些区块过早损坏。

[0061] 存储器模组 103 还包括一个命令分配装置 123，通过数据接口 105 接收主控制器 101 发出的指令，并把相应的指令发送至存储器模组 103 内对应的装置。

[0062] 存储器模组 103 还包括一个内部数据交换控制装置 125，以控制闪速存储装置 113a-113n 与动态随机存取存储装置 107a-107n 之间的数据交换。内部数据交换控制装置 125 可以包括第一数据交换控制装置 127，以控制自闪速存储装置 113a-113n 读取数据并写入动态随机存取存储装置 107a-107n 的操作。内部数据交换控制装置 125 可以包括第二数据交换控制装置 129，以控制从动态随机存取存储装置 107a-107n 读取数据并写入闪速存储装置 113a-113n 的操作。在一些实施例中，内部数据交换控制装置 125 可以采用状态机实现。

[0063] 存储器模组 103 还包括预取缓存 131 和桥接装置 133。预取缓存 131 用于缓存从闪速存储装置 113a-113n 读出的数据。在一些实施例中，预取缓存 131 的位宽比单个闪速存储装置的位宽大。把多个闪速存储装置并行地连接至预取缓存 131，从这些闪速存储装置读出的数据可以并行地写入预取缓存 131，可以在一定程度上弥补闪速存储装置较慢的读取速度，以提高存储器模组 103 的整体效率。预取缓存 131 通过桥接装置 133 与数据接口 105 连接，把从闪速存储装置 113a-113n 读出的数据输出存储器模组 103。桥接装置 105 把从预取缓存 131 接收到的数据转换成符合数据接口 105 标准的数据，并通过数据接口 105

把这些数据发送给对应的装置。在一些实施例中，预取缓存 131 与桥接装置 105 可以整合为一个装置。

[0064] 在一些实施例中，动态随机存取存储装置 107a-107n 和闪速存储装置 113a-113n 在同一地址空间被编址，或使用一统一的编址空间。

[0065] 以下结合图 1 和图 2-7 说明本申请一个实施例中的存储器模组 103 的操作。

[0066] 图 2 展示了本申请一个实施例中数据由主控制器 101 写入动态随机存取存储装置 107a-107n 的方法 200 的流程图。方法 200 包括以下操作：数据接口 105 接收由主控制器 101 发出的对动态随机存取存储装置 107a-107n 之一或多个进行写操作的命令以及需要写入的数据 (201)；数据接口 105 把接收到的命令发送给命令分配装置 123(203)；数据接口 105 把接收到的数据发送至缓存 111(205)；命令分配装置 123 对接收到的命令进行判断 (207)；命令分配装置 123 发送写命令给动态随机存取存储装置控制器 109(209)；动态随机存取存储装置控制器 109 根据从命令分配装置 123 接收到的命令把缓存 111 中的数据写入对应的动态随机存取存储装置 (211)。

[0067] 在一些实施例中，命令可以包括需要写入这些数据的动态随机存取存储装置的地址。

[0068] 在一些实施例中，命令分配装置 123 可以根据接收到的命令发出新的命令。在一些实施例中，命令分配装置 123 也可以判断接收到的命令，再根据判断的结果直接把接收到的命令发送至相应的装置。

[0069] 图 3 展示了本申请一个实施例中主控制器 101 从动态随机存取存储装置 107a-107n 读取数据的方法 300 的流程图。方法 300 包括以下操作：数据接口 105 接收由主控制器 101 发出的从动态随机存取存储装置 107a-107n 之一或多个读取数据的命令 (301)；数据接口 105 把接收到的命令发送给命令分配装置 123(303)；命令分配装置 123 对接收到的命令进行判断 (305)；命令分配装置 123 把命令发送给动态随机存取存储装置控制器 109(307)；动态随机存取存储装置控制器 109 根据接收到的命令控制动态随机存取存储装置 107a-107n 读出数据并把这些数据发送给数据接口 105(309)；数据接口 105 把这些数据发送给主控制器 101(311)。

[0070] 图 4 展示了本申请一个实施例中从闪速存储装置 113a-113n 读取数据并写入动态随机存取存储装置 107a-107n 的方法 400 的流程图。方法 400 包括以下操作：数据接口 105 接收由主控制器 101 发出的从闪速存储装置 113a-113n 读取数据并写入动态随机存取存储装置 107a-107n 的命令 (401)；数据接口 105 把接收到的命令发送给命令分配装置 123(403)；命令分配装置 123 对接收到的命令进行判断 (405)；命令分配装置 123 把接收到的命令发送给第一数据交换控制装置 127(407)；第一数据交换控制装置 127 根据接收到的命令，产生从闪速存储装置 113a-113n 读取数据的命令并将该命令发送至管理装置 117，产生把这些数据写入动态随机存取存储装置 107a-107n 的命令并把该命令发送至动态随机存取存储装置控制器 109(409)；管理装置 117 根据接收到的命令从闪速存储装置 113a-113n 读取数据至预取缓存 131(411)；缓存 111 通过第一数据交换控制装置 127 从预取缓存 131 接收这些数据 (413)；动态随机存取存储装置控制器 109 根据接收到的命令把缓存 111 中的数据写入动态随机存取存储装置 107a-107n(415)。

[0071] 图 5 展示了本申请一个实施例中从动态随机存取存储装置 107a-107n 读取数据

并写入闪速存储装置 113a-113n 的方法 500 的流程图。方法 500 包括以下操作：数据接口 105 接收由主控制器 101 发出的从动态随机存取存储装置 107a-107n 读取数据并写入闪速存储装置 113a-113n 的命令 (501)；数据接口 105 把接收到的命令发送给命令分配装置 123(503)；命令分配装置 123 对接收到的命令进行判断 (505)；命令分配装置 123 把接收到的命令发送给第二数据交换控制装置 129(507)；第二数据交换控制装置 129 根据接收到的命令，产生从动态随机存取存储装置 107a-107n 读取数据的命令并将该命令发送至动态随机存取存储装置控制器 109，产生把这些数据写入闪速存储装置 113a-113n 的命令并把该命令发送至管理装置 117(509)；动态随机存取存储装置控制器根据 109 接收到的命令控制动态随机存取存储装置 107a-107n 读出数据经过第二数据交换控制装置 129 至管理装置 117(511)；管理装置 117 根据接收到的命令把接收到的数据写入闪速存储装置 113a-113n(513)。

[0072] 图 6 展示了本申请一个实施例中主控制器 101 从闪速存储装置 113a-113n 读取数据的方法 600 的流程图。方法 600 包括以下操作：数据接口 105 从主控制器 101 接收从闪速存储装置 113a-113n 之一或多个读取数据的命令 (601)；数据接口 105 把接收到的命令发送给命令分配装置 123(603)；命令分配装置 123 对接收到的命令进行判断 (605)；命令分配装置 123 根据判断结果把接收到的命令发送给管理装置 117(607)；管理装置 117 根据接收到的命令从闪速存储装置 113a-113n 中读取数据至预取缓存 131(609)；桥接装置 133 从预取缓存 131 接收数据 (611)；桥接装置 133 把接收到的数据转换成主控制器 101 所要求的格式 (613)；桥接装置 133 通过数据接口 105 把这些数据发送给主控制器 101(615)。

[0073] 对以上的方法的描述只是示例性的，以上每一方法的各操作可以不严格按照上述的顺序进行。一些操作可以合并为一个，而一些操作可以被分割成多个。

[0074] 在一些实施例中，闪速存储装置 113a-113n 和动态随机存取存储装置 107a-107n 之间的数据交换可以不经过数据交换控制装置 125。

[0075] 以上所述的装置可以是电路装置，也可以是电路装置与计算机程序的结合，还可以是计算机程序所实现的功能。比如，命令分配装置 123、桥接装置 133、数据交换控制装置 125 和管理装置 117 等。

[0076] 在一些实施例中，存储器模组 103 可以包括一个内建检测装置 (MBIST)(图中未示)。因为内建检测装置具有读写存储器模组 103 上各存储装置的功能，数据交换控制装置 125 可以借用内建检测装置的部分电路或功能，以降低成本。

[0077] 在一些实施例中，管理装置 117 可以在抽象层中 (abstraction layer)。

[0078] 在一些实施例中，闪速存储装置 113a-113n 可用于存储计算机操作系统、用户配置数据以及一些其他计算机程序，比如启动计算机时被自动运行的计算机程序，这些计算机程序包括但不限于杀毒软件、电子词典、各种驱动程序等。

[0079] 在一些实施例中，一个存储系统中的各存储器模组可同时进行模组内的数据交换，比如从非易失性存储装置读取数据并写入易失性存储装置，或从易失性存储装置读取数据并写入非易失性存储装置。如果把计算机操作系统和其他相关的计算机程序存储在非易失性存储装置中，当需要把这些计算机程序载入非易失性存储装置时，各存储器模组只需要从主控制器接收一个命令即可，数据的交换在存储器模组内部完成。而现有的存储系统中，开机前，所有计算机程序和数据都是存储在硬盘或其它装置内，需要载入这些数据至

易失性存储装置时，所有的数据都要经过同一主控制器载入各存储器模组，其效率显然较低。本申请的存储系统可以提高计算机开关机以及休眠和从休眠中恢复的速度。

[0080] 在一些实施例中，可以在动态随机存取存储装置 107a-107n 中开辟一个区块作为缓存，把系统需要写入闪速存储装置 113a-113n 的数据先存储在这个缓存中。

[0081] 由于本申请的存储器模组内易失性存储装置和非易失性存储装置之间的数据交换过程不需要主控制器和 CPU 参与，一方面可节约计算机系统的资源，另一方面还可提高系统效率。

[0082] 在一些实施例中，在计算机开机时，用户可选择从硬盘或存储器模组载入操作系统和其他计算机程序。

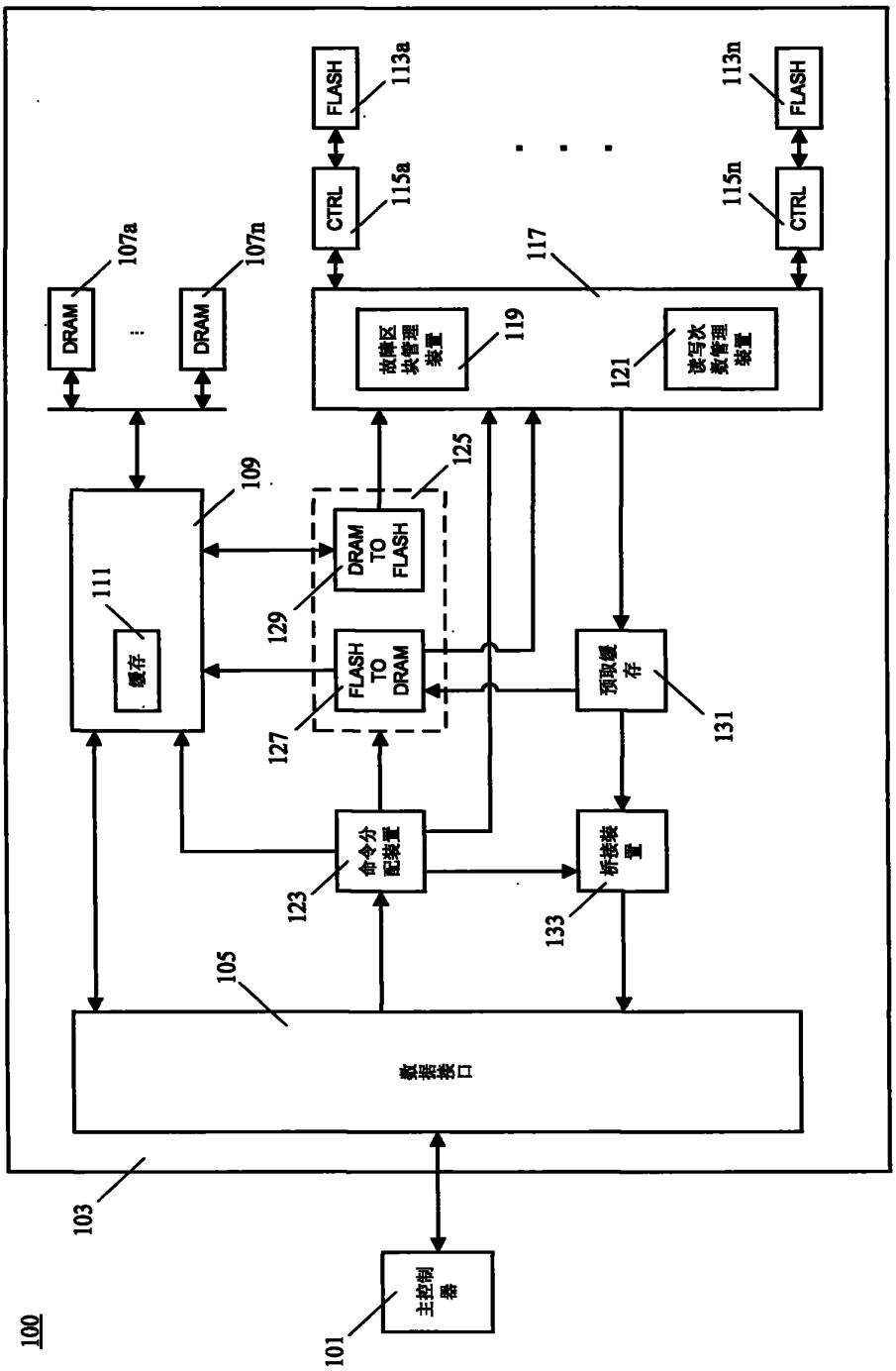


图 1

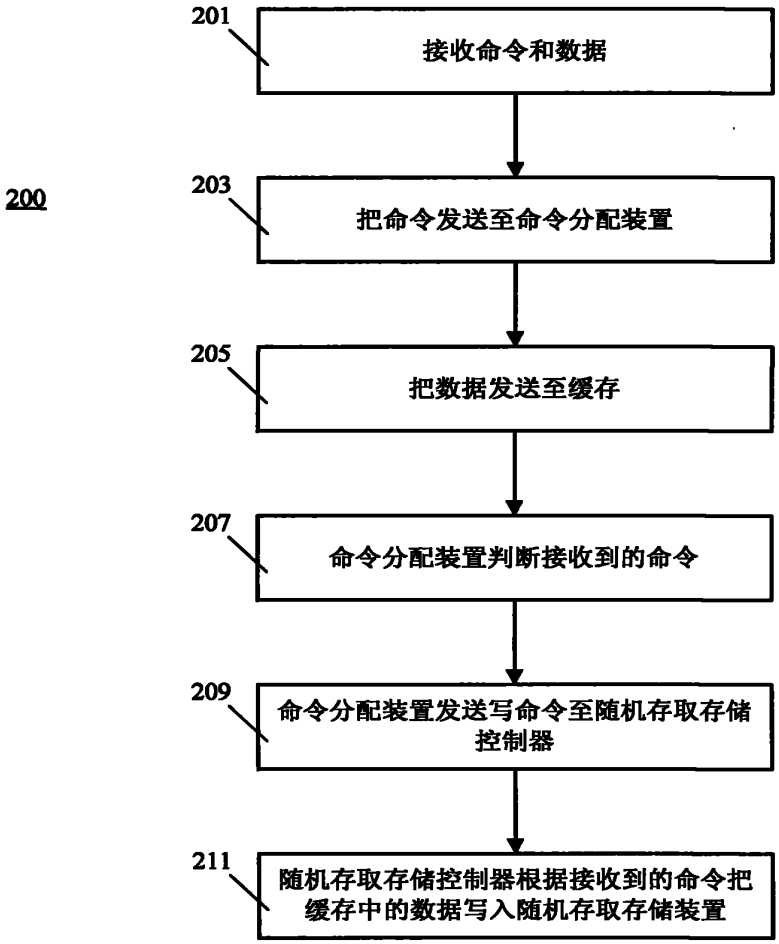


图 2

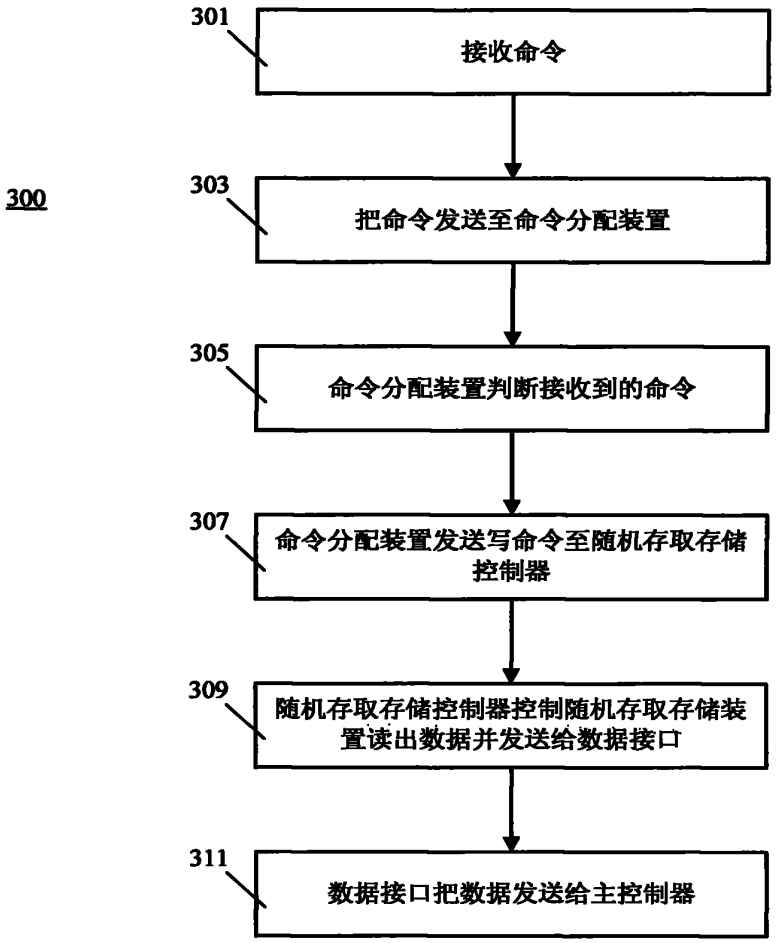


图 3

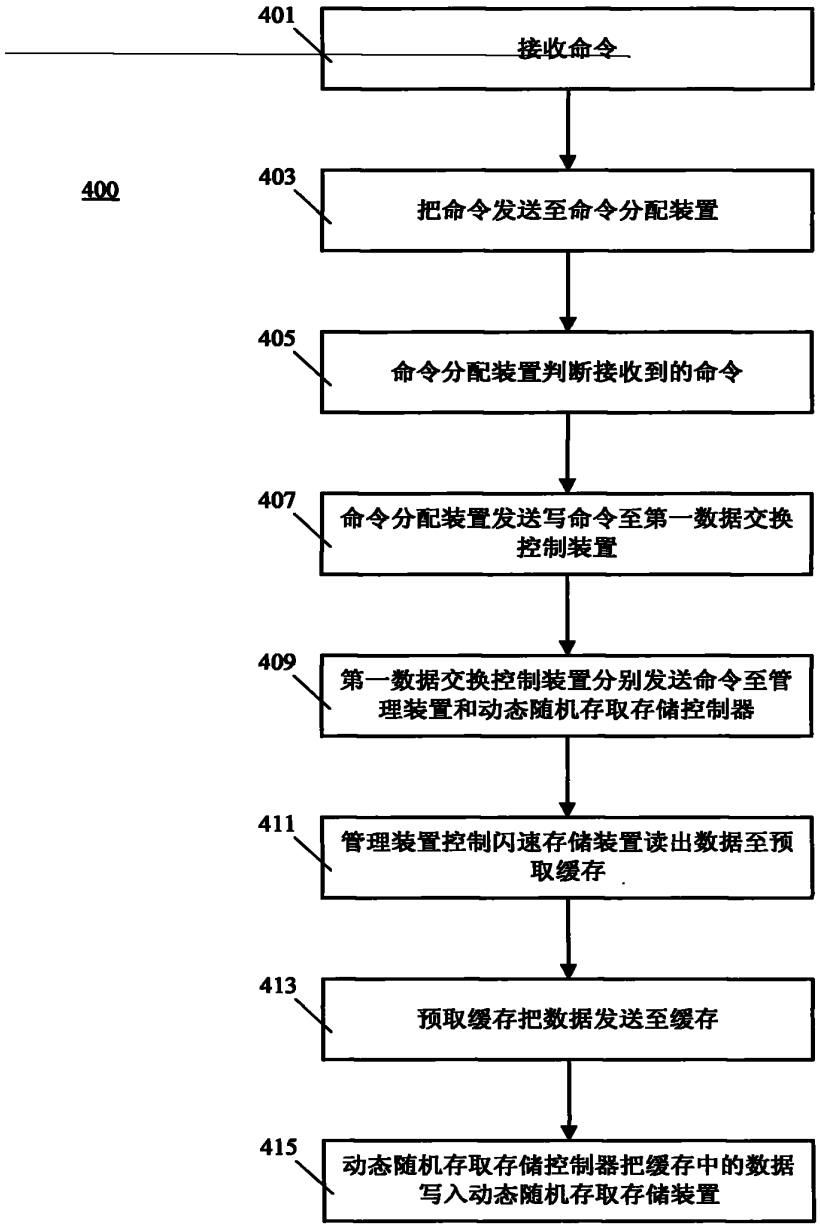


图 4

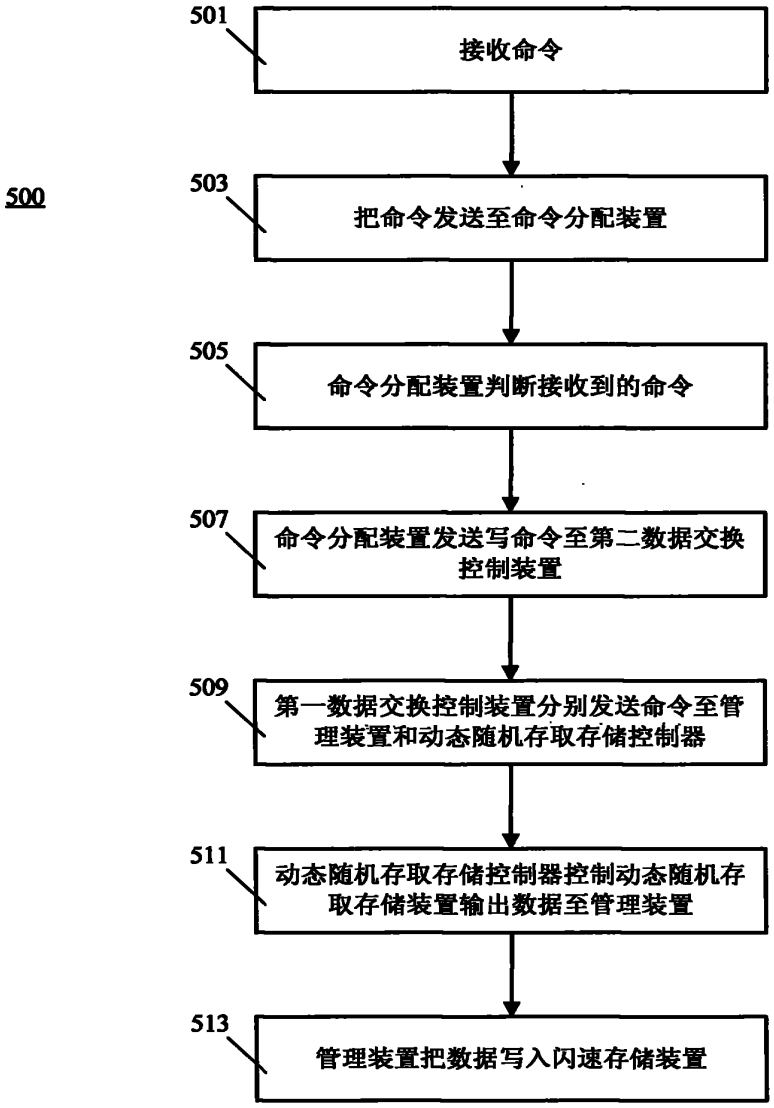


图 5

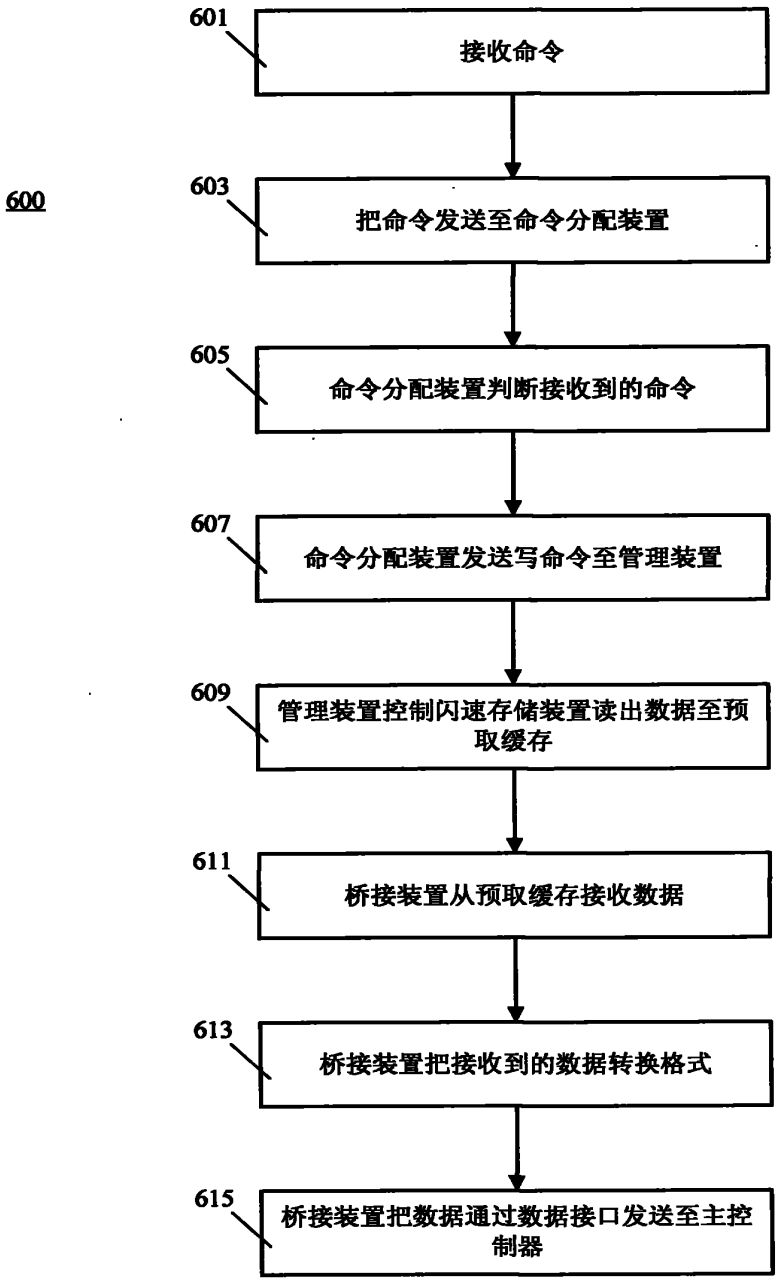


图 6

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[71] 申请人 硅存储技术公司
地址 美国加利福尼亚州
[72] 发明人 F·L·林 B·叶

[74] 专利代理机构 中国专利代理(香港)有限公司
代理人 张雪梅 刘 杰

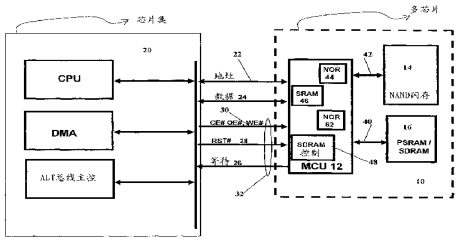
权利要求书 7 页 说明书 27 页 附图 9 页

[54] 发明名称

统一的存储器和控制器

[57] 摘要

具有控制器的存储器装置。该控制器具有用于接收 RAM 地址信号的第一地址总线，用于接收 RAM 数据信号的第一数据总线，用于接收 RAM 控制信号的第一控制总线。该控制器还具有与易失性 RAM 存储器接口连接的第二地址总线、第二数据总线、和第二控制总线。该控制器还具有与非易失性 NAND 存储器接口连接的第三地址/数据总线，和与非易失性 NAND 存储器接口连接的第三控制总线。该控制器还具有非易失性可引导存储器，用于在第一地址总线上接收第一地址并将第一地址映射到非易失性 NAND 存储器中的第二地址的装置，以及用于保持存储在作为高速缓存的易失性 RAM 存储器中的数据与在非易失性 NAND 存储器中的第二地址处的数据之间的数据一致性的装置。



1．一种存储器控制器，包括：

第一总线，用于从主机装置接收地址信号和数据信号；

第二总线，用于与易失性 RAM 存储器装置接口连接；

第三总线，用于与 NAND 存储器装置接口连接；

非易失性存储器，用于存储用于所述存储器控制器的可引导代码，所述可引导代码用于启动所述控制器的操作；

用于从第一总线接收第一地址并用于将所述第一地址映射到所述 NAND 存储器装置的第二地址，以及用于操作作为用于至或来自所述 NAND 存储器装置中的第二地址的数据的高速缓存的所述易失性 RAM 存储器装置的装置；以及

用于保持存储在所述 NAND 存储器装置中的所述第二地址处的数据与存储在用作高速缓存的所述易失性 RAM 存储器中的数据之间的数据一致性的装置。

2．如权利要求 1 所述的存储器控制器，进一步包括连接到所述第二总线的 RAM。

3．如权利要求 1 所述的存储器控制器，进一步包括：

用于从所述第一总线接收 NOR 协议命令，并用于对所述 NAND 存储器装置操作所述 NOR 命令的装置。

4．一种存储器控制器，包括：

第一总线，用于从主机装置接收地址信号和数据信号；

第二总线，用于与易失性 RAM 存储器装置接口连接；

第三总线，用于与 NAND 存储器装置接口连接；

NOR 存储器，用于存储用于所述存储器控制器的可引导代码，所述可引导代码用于启动所述控制器的操作；

用于从所述第一总线接收 NOR 协议命令，并用于操作所述 NOR 存储器，以及用于操作所述易失性 RAM 存储器装置以模拟 NOR 存储器的操作的装置；以及

用于操作作为 ATA 存储装置的 NAND 存储器装置的装置。

5．如权利要求 4 所述的存储器控制器，进一步包括：

寄存器，用于存储来自主机装置的结构参数，所述结构参数用于将来自第一总线的地址分成 NOR 操作、RAM 操作和 NAND 操作。

6．如权利要求 4 所述的存储器控制器，进一步包括连接到所述第二总线的易失性 RAM 存储器装置。

7．如权利要求 4 所述的存储器控制器，其中用于操作所述易失性 RAM 存储器装置以模拟 NOR 存储器的操作的所述装置进一步包括：

用于从第一总线接收第一地址并且用于将所述第一地址映射到所述 NAND 存储器装置的第二地址，以及用于操作作为用于至或来自所述 NAND 存储器装置中的第二地址的数据的高速缓存的所述易失性 RAM 存储器装置的装置；以及

用于保持存储在所述 NAND 存储器装置中的所述第二地址处的数据与存储在用作高速缓存的所述易失性 RAM 存储器中的数据之间的数据一致性的装置。

8．一种存储器控制器，包括：

第一总线，用于从主机装置接收地址信号和数据信号；

第二总线，用于与易失性 RAM 存储器装置接口连接；

第三总线，用于与 NAND 存储器装置接口连接；

寄存器，用于存储来自主机装置的结构参数，所述结构参数用于将来自第一总线的地址分成由所述 RAM 存储器装置进行的操作和由所述 NAND 存储器装置进行的操作。

9．一种存储器控制器，包括：

第一总线，用于从主机装置接收地址信号和数据信号；

第二总线，用于与易失性 RAM 存储器装置接口连接；

NOR 非易失性存储器装置，其中所述 NOR 非易失性存储器装置存储被配置用于操作控制器的程序代码，由此被所述控制器接收的所述第一总线上的第一地址用于响应于 NOR 协议命令操作该 NOR 存储器，被所述控制器接收的所述第一总线上的第二地址用于响应于 RAM 存储器协议操作该 RAM 存储器，以及被所述控制器接收的所述第一总线上的第三地址用于模拟 NOR 协议命令来操作该 RAM 存储器。

10．一种存储器控制器，包括：

第一总线，用于从主机装置接收地址信号和数据信号；

第二总线，用于与易失性 RAM 存储器装置接口连接；

NOR 非易失性存储器装置；以及

寄存器，用于存储来自主机装置的结构参数，所述结构参数用于将来自第一

总线的地址分成由作为 NOR 存储器装置的所述 NOR 存储器装置、作为 RAM 存储器装置的所述 RAM 存储器装置、和模拟 NOR 存储器装置的操作的所述 RAM 存储器装置进行的操作。

11．一种 NOR 存储器，包括：

存储器控制器的第一集成电路管芯，其具有用于接收 NOR 协议命令信号的第一总线；

所述存储器控制器进一步具有用于采用 NAND 存储器协议与 NAND 存储器装置进行通信的第二总线；

所述存储器控制器进一步具有 NOR 存储器，其用于存储用于启动所述存储器控制器的操作的程序代码，并用于从所述第一总线接收 NOR 协议命令并响应于其在所述第二总线上发出 NAND 协议命令，以模拟 NOR 存储器装置的操作；

NAND 存储器装置的第二集成电路管芯，其被连接到所述第一集成电路装置的所述第二总线；

其中所述第一和第二集成电路装置被一起封装在同一封装中。

12．如权利要求 11 所述的 NOR 存储器，进一步包括：

所述第一集成电路管芯进一步具有第三总线，其用于采用 RAM 存储器协议与 RAM 存储器装置进行通信。

13．如权利要求 12 所述的 NOR 存储器，进一步包括：

连接到所述第三总线的 RAM 存储器。

14．如权利要求 13 所述的 NOR 存储器，其中所述 RAM 存储器是独立的集成电路管芯，并被封装在与所述第一和第二集成电路管芯相同的封装中。

15．如权利要求 13 所述的 NOR 存储器，其中所述 RAM 存储器与具有所述存储器控制器的所述第一集成电路管芯集成在一起。

16．如权利要求 13 所述的 NOR 存储器，其中所述 RAM 存储器用作操作用于模拟所述 NOR 协议命令的所述 NAND 存储器装置的高速缓存。

17．如权利要求 13 所述的 NOR 存储器，进一步包括：

存储器控制器的所述第一集成电路管芯进一步具有寄存器，其用于存储用于将来自第一总线的地址分成 NOR 操作和使用所述 NAND 存储器的 NOR 模拟操作的参数。

18．如权利要求 17 所述的 NOR 存储器：

其中所述寄存器用于存储用于将来自第一总线的地址分成 NOR 操作、使用所述 NAND 存储器的 NOR 模拟操作、RAM 操作和 NAND 操作的参数；并且

其中用于分开来自第一总线的地址的所述参数是来自主机装置的结构参数。

19．一种通用存储器，包括：

存储器控制器，其具有用于从主机装置接收地址信号和数据信号的第一总线、用于与 NAND 存储器接口连接的第二总线；和用于与 RAM 存储器接口连接的第三总线；以及用于与 NOR 存储器接口连接的第四总线；

连接到所述第二总线的 NAND 存储器；

连接到所述第三总线的 RAM 存储器；

连接到所述第四总线的 NOR 存储器；并且

其中所述存储器控制器响应于在所述第一总线上提供的 NOR 协议命令、RAM 协议命令和 ATA NAND 协议命令。

20．如权利要求 19 所述的通用存储器，其中所述通用存储器是单片集成电路管芯。

21．如权利要求 19 所述的通用存储器，其中所述存储器控制器是第一集成电路管芯，所述 NAND 存储器是第二集成电路管芯，所述 RAM 存储器是第三集成电路管芯，以及所述 NOR 存储器被集成在所述存储器控制器中。

22．如权利要求 21 所述的通用存储器，其中所述第一、第二和第三集成电路管芯被封装在一起。

23．如权利要求 19 所述的通用存储器，其中所述存储器控制器是第一集成电路管芯，所述 NAND 存储器是第二集成电路管芯，所述 RAM 存储器和所述 NOR 存储器被集成在所述存储器控制器中。

24．如权利要求 23 所述的通用存储器，其中所述第一和第二集成电路管芯被封装在一起。

25．如权利要求 19 所述的通用存储器，其中所述 NOR 存储器用于存储程序代码，其被配置用以响应于作为 NOR 地址的所述第一总线上的第一地址；作为 RAM 地址的所述第一总线上的第二地址；以及作为 ATA NAND 地址的所述第一总线上的第三地址。

26．如权利要求 25 所述的通用存储器，其中所述 NOR 存储器用于进一步存

储被配置用于启动所述存储器控制器的操作的程序代码。

27．如权利要求26所述的通用存储器，其中所述存储器控制器进一步包括：

寄存器，用于存储来自主机装置的结构参数，所述结构参数将来自第一总线的地址分成NOR操作、使用所述NAND存储器的NOR模拟操作、RAM操作和ATA NAND操作。

28．如权利要求27所述的通用存储器，其中所述NOR存储器用于进一步存储被配置用于使所述RAM存储器用作用于使用所述NAND存储器的NOR模拟操作的高速缓存的程序代码。

29．一种主机可确定的存储器，包括：

存储器控制器，其具有用于连接到主机装置并用于接收地址信号和数据信号的第一总线；用于连接到NOR存储器的第二总线；用于连接到RAM存储器的第三总线；用于连接到NAND存储器的第四总线；

连接到所述第二总线的NOR存储器；

连接到所述第三总线的RAM存储器；

连接到所述第四总线的NAND存储器；以及

寄存器，用于存储来自主机装置的结构参数，所述结构参数用于将来自第一总线的第一地址分成NOR操作，将来自第一总线的第二地址分成使用所述NAND存储器的NOR模拟操作，将来自第一总线的第三地址分成RAM操作，以及将来自第一总线的第四地址分成ATA NAND操作。

30．如权利要求29所述的主机可确定的存储器，其中所述NOR存储器与所述存储器控制器集成到同一集成电路管芯中。

31．如权利要求30所述的主机可确定的存储器，其中所述RAM存储器与所述存储器控制器集成到同一集成电路管芯中。

32．如权利要求30所述的主机可确定的存储器，其中所述RAM存储器是第一集成电路管芯，以及所述存储器控制器是第二集成电路管芯，并且其中所述第一集成电路管芯与所述第二集成电路管芯封装在一起。

33．如权利要求29所述的主机可确定的存储器，其中所述NOR存储器用于存储被配置用于启动所述存储器控制器的操作的程序代码。

34．一种NOR模拟存储器，包括：

存储器控制器，其具有用于存储用于启动存储器控制器的操作的程序代码的

非易失性存储器，并具有用于从主机装置接收地址和数据信号的第一总线；用于与 RAM 存储器接口连接的第二总线；以及用于与 NAND 存储器接口连接的第三总线；

连接到所述第二总线的易失性 RAM 存储器；

连接到所述第三总线的 NAND 存储器；

用于从所述第一总线接收 NOR 协议命令和第一地址，并用于将所述第一地址映射到所述 NAND 存储器中的第二地址，以及用于响应其来操作所述 NAND 存储器的装置，并且所述 RAM 存储器用作用于至或来自该 NAND 存储器中的第二地址的数据的高速缓存；以及

用于保持作为高速缓存的RAM中所存储的数据与在NAND存储器中的第二地址处的数据之间的数据一致性的装置。

35．如权利要求 34 所述的 NOR 模拟存储器，其中所述用于接收的装置和所述用于保持的装置包括存储在所述非易失性存储器中的程序代码。

36．如权利要求 34 所述的 NOR 模拟存储器，其中所述易失性 RAM 被嵌入到所述存储器控制器中，并且其中所述存储器控制器是第一集成电路管芯，以及其中所述 NAND 存储器是第二集成电路管芯，并且其中所述第一和第二管芯封装在一起。

37．一种存储器装置，包括：

存储器控制器，其具有用于与多个主机装置接口连接的多个第一总线，且每个第一总线与每个主机装置连接；并具有多个第二总线；

连接到该多个第二总线并具有输出总线的仲裁电路；

连接到仲裁电路的输出总线的 NAND 存储器；并且

其中所述主机装置的每一个具有通过所述仲裁电路对所述 NAND 存储器的存取。

38．如权利要求 37 所述的存储器装置，进一步包括：

所述存储器控制器具有多个第三总线；

连接到该多个第三总线并具有输出总线的第二仲裁电路；

连接到第二仲裁电路的输出总线的易失性 RAM 存储器；并且

其中所述主机装置的每一个具有通过所述第二仲裁电路对所述易失性 RAM 存储器的存取。

39．一种存储器装置，包括：

存储器控制器，其具有用于与多个主机装置接口连接的第一总线，且每个主机装置被提供有来自所述存储器控制器的用于许可对所述第一总线的存取的单独的控制信号；该存储器控制器还具有多个第二总线和多个第三总线；

连接到该多个第二总线并具有第一输出总线的第一仲裁电路；

连接到第一仲裁电路的第一输出总线的NAND存储器；

其中所述主机装置的每一个具有通过所述第一仲裁电路对所述NAND存储器的存取；

连接到该多个第三总线并具有第二输出总线的第二仲裁电路；

连接到第二仲裁电路的第二输出总线的易失性RAM存储器；并且

其中所述主机装置的每一个具有通过所述第二仲裁电路对所述易失性RAM存储器的存取。

40．一种存储器装置，包括：

存储器控制器，其具有用于与多个主机装置接口连接的多个第一总线，且每个第一总线用于从不同的主机装置接收地址信号和数据信号，用于与NAND存储器接口连接的第二总线；和用于与RAM存储器接口连接的第三总线；以及用于与NOR存储器接口连接的第四总线；

连接到所述第二总线的NAND存储器；

连接到所述第三总线的RAM存储器；

连接到所述第四总线的NOR存储器；并且

其中所述存储器控制器响应于在所述不同的第一总线的每一个上提供的NOR协议命令、RAM协议命令和ATA NAND协议命令。

统一的存储器和控制器

本申请要求于2005年12月28日提交的临时申请60/754,937的优先权，在此并入其公开的全部内容。

技术领域

本发明涉及一种存储器装置，更具体地说，涉及一种这样的存储器装置，该存储器装置具有接收常规随机地址格式的地址和数据的能力，并将该数据/地址映射到NOR存储器、RAM存储器、用作用于NAND存储器的高速缓存由此模拟伪NOR（PNOR）操作的RAM存储器、以及ATA格式的非易失性NAND存储器。所述地址和数据通过单个总线或多个总线从一个或多个处理器接收。本发明还涉及一种用在这种存储器装置中的具有嵌入式可引导NOR存储器的存储器控制器。

背景技术

易失性随机存取存储器，诸如SRAM或DRAM（或者SDRAM）或者PSRAM（下文统称为RAM），是本领域中公知的。典型地，这些类型的易失性存储器在地址总线上接收地址信号，在数据总线接上收数据信号，并且在控制总线上接收控制信号。

并行NOR型非易失性存储器也是本领域公知的。典型地，它们在与提供给RAM的相同类型的地址总线上接收地址信号，在与提供给RAM的相同类型的数据总线上接收数据信号，并且在与提供给RAM的相同类型的控制总线上接收控制信号。与RAM类似，NOR存储器是随机存取存储器装置。然而，由于NOR存储器需要某些操作，而RAM不需要，诸如扇区擦除或者块擦除，因此这些具有命令的性质的操作以特定数据模式的序列被提供给NOR装置。这称为NOR协议命令。在现有技术中，存在两种类型的NOR协议命令：1)与最初由Intel发布的协议命令集兼容的那些协议命令；2)与最初由AMD发布的协议命令集兼容的那些协议命令。在任一种情况下，NOR存储器都电接口连接至与RAM所接口连接的相同的地址、数据和控制总线。而且，常规的NOR存储器装置也可以以公知的常规格式，如SPI、LPC或固件集线器，串行地提供数据、地址和控制信号。

NAND 型非易失性存储器也是本领域公知的。然而，与并行的 NOR 装置不同，NAND 存储器将数据存储在可随机存取的块中，其中块内的单元被以顺序的格式存储。而且，地址和数据信号被提供在相同的总线上，但采用的是多路复用的方式。NAND 存储器具有的优点是，它们比 NOR 装置更致密，从而降低了每比特数据的存储成本。

由于 NAND 装置的每比特数据的较低的成本，已经尝试使用 NAND 装置来模拟 NOR 装置的操作。被称为 OneNAND（三星公司的商标）的一种这样的装置使用 RAM 存储器来临时缓冲数据到 NAND 存储器和从 NAND 存储器临时缓冲数据，由此模拟 NOR 存储器的操作。然而，OneNAND 装置被认为受到两个缺点的影响。第一，与 OneNAND 界面连接的用户或主机装置被认为必须留意数据一致性。在数据一致性中，由于用户或主机向 RAM 写入，因此 RAM 中的数据可能新于（并且从此不同于）在 NAND 中最初读取 RAM 中的数据的位置中的数据。因而，在 OneNAND 装置中用户或主机必须进行这样的动作，即将来自 RAM 的数据写回 NAND 中的最终位置以便存储该数据，或记住 RAM 中的数据是更新的数据。被认为是 OneNAND 装置的缺点的第二个问题是它不能提供自动地址映射。在 OneNAND 装置中，一旦数据被写入该 OneNAND 装置的 RAM 部分中，主机或用户必须发出命令或命令序列以向该 OneNAND 装置的 NAND 部分中的最终位置写入该 RAM 部分中的数据。类似地，对于读操作，主机或用户必须从 OneNAND 的 NAND 部分中的特定区域发出读命令，以将该数据载入 RAM 部分中，然后从该 RAM 部分读出数据。

被认为具有类似缺陷的另一现有技术装置是来自 M Systems 的 DiskOnChip 装置。在 DiskOnChip 装置中，具有有限量的 RAM 的控制器控制 NAND 存储器的操作。然而，DiskOnChip 装置的控制器部分被认为不具备任何板上非易失性可引导存储器，如 NOR 存储器。

于 2006 年 3 月 9 日公布的美国专利申请 2006/0053246 中示出了表明模拟 NOR 存储器操作的具有控制器的 NAND 存储器的使用的现有技术公开物。尽管该公开物示出了具有连接到多个处理器的控制器的 NAND 存储器的使用，但是看起来该 NAND 存储器不能通过 ATA 格式操作直接存取。因而，在没有与外部直接存取的情况下，对该 NAND 存储器的所有存取必须借助控制器来完成。

因而，需要一种没有这些缺点并具有提供现有技术中没有发现的另外的存储

器存取特性的能力的存储器装置。

发明内容

在本发明中，通用的存储器装置具有控制器。该控制器具有用于从主机装置接收地址信号和数据信号的第一总线、用于与 NAND 存储器接口连接的第二总线；和用于与 RAM 存储器接口连接的第三总线；以及用于与 NOR 存储器接口连接的第四总线。NAND 存储器连接到第二总线。RAM 存储器连接到第三总线。NOR 存储器连接到第四总线。该存储器控制器响应于 NOR 协议命令、RAM 协议命令和 ATA NAND 协议命令。

本发明还涉及一种用在这种存储器装置中的存储器控制器。

最后本发明还涉及存储器控制器与不同类型的存储器 NOR、RAM 和 NAND 的多种组合，以便作为 NOR 存储器、RAM 存储器、NOR 模拟存储器和 ATA NAND 存储器工作。

附图说明

图 1 是包括存储器控制器、连接到单个主机系统或用户的存储器装置的第一实施例的方框图。

图 2 是示出在存储器装置外部由主机或用户所见的地址空间与图 1 中所示的存储器装置的第一实施例中的 NOR 存储器、RAM 存储器和 NAND 存储器的映射的存储器映射图。

图 3 是用于该存储器装置中的控制器的详细方框电路图。

图 4 是包含存储器控制器、与单个主机系统或用户相连接的存储器装置的第二实施例的方框图。

图 5 是示出在存储器装置外部由主机或用户所见的地址空间与图 4 中所示的存储器装置的第二实施例中的 NOR 存储器、RAM 存储器和 NAND 存储器的映射的存储器映射图。

图 6 是包含本发明的存储器控制器、通过单个总线与多个主机系统或用户以及多个请求总线相连接的本发明的存储器装置的第三实施例的方框图。

图 7 是包含本发明的存储器控制器、通过多个总线与多个主机系统或用户相连接的本发明的存储器装置的第四实施例的方框图。

图 8 是包含本发明的存储器控制器、通过多个总线与多个主机系统或用户相连接的本发明的存储器装置的第五实施例的方框图。

图9是包含本发明的存储器控制器、通过多个总线与多个主机系统或用户相连接的本发明的存储器装置的第六实施例的方框图。

具体实施方式

参考图1，示出了存储器装置10的第一实施例。存储器装置10包括存储器控制器12，NAND存储器14，以及RAM存储器16。存储器装置10与主机装置20通过第一RAM地址总线22，第一RAM数据总线24，以及多个控制信号例如等待26，RST#28，以及CE#，OE#，和WE#30接口连接，其全部是用于RAM总线的控制信号的领域中的技术人员所熟知的。以下除非另有规定，等待26，RST#28以及CE#，OE#，和WE#30上的所有控制信号被称为第一RAM控制总线32。第一RAM地址总线22，第一RAM数据总线24和第一RAM控制总线32从主机装置20连接到存储器装置10的存储器控制器12。进一步地，如之前所讨论的，存储器装置10和主机装置20之间的接口连接可以通过串行总线，其中数据、地址和控制总线串行地连接在主机装置20和存储器装置10之间。这种存储器装置10也在本发明的范围内。

存储器控制器12具有第二RAM地址总线(与第一RAM地址总线22类似)，第二RAM数据总线（与第一RAM数据总线24类似），以及第二控制总线（与第一RAM控制总线32类似），其全部被共同地简单示为连接到RAM存储器16的第二RAM总线40。存储器控制器12还具有连接到NAND存储器14的NAND地址/数据总线和NAND控制总线（其全部被共同地示为NAND总线42）。RAM存储器16可以集成或嵌入在存储器控制器12中，作为单芯片集成电路。可替换地，RAM存储器16可以是与存储器控制器12分开的集成电路。可替换地，部分RAM存储器16可以与存储器控制器12集成以及部分RAM存储器16可以与存储器控制器12分开。RAM存储器16作为单独管芯（die）的优点将在下文中讨论。然而，RAM存储器16与存储器控制器12集成的优点是在操作中RAM存储器16可以更快速。

在一个实施例中，存储器控制器12为单个集成电路管芯。该控制器还具有嵌入在该存储器控制器集成电路管芯内的第一NOR存储器44，第二NOR存储器62，SRAM存储器46，以及SDRAM控制器48（用于控制RAM16的操作，如果RAM16为SDRAM类型的RAM存储器，并且在存储器控制器12之外）。当然，第一NOR存储器44和第二NOR存储器62可以是相同的物理NOR存储器

的一部分。在图3中示出了存储器控制器12的实施例的详细的方框图。正如在此所使用的，“NOR存储器”意指任何类型的随机存取非易失性存储器。该NOR存储器包括但不限于浮栅型存储器，ROM，或使用俘获材料的单元等。进一步如在此所使用的，“NAND存储器”意指任何类型的串行存取非易失性存储器，其可以包括有缺陷的单元。

在一个实施例中，存储器控制器12，RAM存储器16和NAND存储器14中的每一个由单个集成电路管芯制成并且采用MCP（多芯片封装）方式被封装在一起。这种配置的优点是，对于要求大（或小）容量的存储器的用户或主机20而言，存储器的容量可以通过简单地改变容易可用的NAND存储器14的管芯或者如果速度是一个因素则改变容易可用的RAM存储器16来改变。因此，在单独的管芯中具有存储器控制器12，RAM存储器16和NAND存储器14意味着能够容易地制造存储器装置10的不同尺寸和速度或性能。

当然，也能将存储器控制器12，RAM存储器16和NAND存储器14制成单一的集成电路管芯。如果存储器控制器12，RAM存储器16和NAND存储器14由单一的集成电路管芯制成，则还可以进行供应以提供外部NAND总线42以便另外从外部提供的NAND存储器能够附着到存储器装置10以扩展存储器装置10的存储器容量。

参考图2，示出了说明如主机装置20所见的并且映射到图1所示的存储器装置10的第一实施例中的地址映射的存储器映射。如主机装置20所见的存储器映射具有两个一般部分：随机存取和大容量存储存取。随机存取部分占用较低的存储器地址位置（尽管那不是必要条件）。在随机存取部分内，最低的存储器地址用于NOR存储器存取部分50，之后是伪NOR（PNOR）存储器存取部分52，之后是RAM存取部分54，之后是结构存取部分56。每个部分将进行如下说明。

如主机装置20所见的NOR存储器存取部分50在于，当主机20在该部分50中进行操作时，结果是对物理NOR存储器44的操作。因此，存储器部分50与物理NOR存储器44的映射为一对一的。换句话说，分配给NOR部分50的存储器空间的量依赖于在存储器装置10中可用的NOR存储器44的量。在一个实施例中，嵌入在存储器控制器12中的NOR存储器44的量为4兆位，且具有2K字扇区大小和32K字块大小。进一步地，当主机装置20认为其正对NOR部分50进行操作时（如在发布读取/写入/擦除等的命令中），作为结果而发生的操作是直接

对 NOR 存储器 44 进行。该 NOR 部分 50 可以由正在设法存储要求无等待时间的随机存取的性能关键代码/数据的主机装置 20 来使用。进一步地，如果程序存储在 NOR 存储器 44 中，则其能够在 NOR 存储器 44 内被原位执行。因此 NOR 存储器 44 能够存储“引导”主机装置 20 的程序或代码。

如主机装置 20 所见的 PNOR 部分 52 在于，当主机 20 在该部分 52 中进行操作时，主机 20 认为其正对非易失性的 RAM 存储器 16 进行操作。因此，对于主机装置 20，其能够类似对任何其它 RAM 存储器 16 那样对 PNOR 部分 52 进行操作，除了存储在 PNOR 部分 52 中的数据是非易失性的以外，全部都不用发布 NOR 协议命令。在一个实施例中，PNOR 部分 52 恰似 NAND 存储器那样被分成页，且每页为 8K 字节，2K 字节或 512 字节。在操作过程中，当主机装置 20 与存储器装置 10 接口连接时，其与 RAM 存储器 16 接口连接，且存储器控制器 12 将数据备份到 NAND 存储器 14 以及从 NAND 存储器 14 备份数据，并且保持在 RAM 存储器 16 和 NAND 存储器 14 之间的数据一致性，并且存储器控制器 12 将由主机装置 20 提供的地址映射到 NAND 存储器 14 中的实际数据的地址。由于可用的 NAND 存储器 14 的量大于实际的 RAM 存储器 16，因此 PNOR 部分 52 可以是比 RAM 存储器 16 中可用的实际存储器的量大得多的存储器空间。

进一步地，PNOR 部分 52 能够分为四（4）个区域，每一个映射到区（zone）：RAM 存储器 16 中的区 0，区 1，区 2 以及区 3。每个区能具有不同程度的映射。在从 PNOR 部分 52 中的区域到 RAM 存储器 16 中的区的映射是一对一的情况下，于是这被称为“静态分页模式”。在从 PNOR 部分 52 中的区域到 RAM 存储器 16 中的区的映射是多对一的情况下，于是这被称为“动态分页模式”。静态分页模式映射将导致最小的等待时间，因为 PNOR 部分 52 中的存储器空间的量，例如 256 页（或在 2K 字节页的情况下为 512K 字节），总是映射到 RAM 16 中的相同量的存储器空间，例如 256 页（或 512K 字节），其又映射到 NAND 存储器 14 中的 256 页（或 512K 字节）中。在那种情况下，尽管由于 RAM 存储器 16 也是随机存取所以在操作过程中存取时没有等待时间，但是在最初从 NAND 存储器 14 到 RAM 存储器 16 和从 RAM 存储器 16 到 NAND 存储器 14 的加载和存储时存在等待时间。在动态分页模式映射中，例如映射映射到 RAM 存储器 16 的 512 页的 PNOR 部分 52 中的存储器空间的 40,000 页，其又映射到 NAND 存储器 14 的 40,000 页，将出现更大量的等待时间。该等待时间将出现在最初的数据/程序从 NAND 存储

器 14 到 RAM 16 中的加载中，以及在从 PNOR 部分 52 重新获得数据/程序的操作过程中，如果存在高速缓存缺失，则其可能要求数据/程序首先从 NAND 存储器 14 加载到 RAM 16 中。因此，对于 PNOR 部分 52 的等待时间将根据所配置的区的大小而不同。RAM 存储器 16 的每个区的边界，并且因此，多少存储器空间从 PNOR 部分 52 的每个区域被映射到 RAM 存储器 16 中，可以由主机装置 20 或用户来设置。结果，主机装置 20 能够配置四个区在静态分页模式下操作以存储/重新获得程序或时间临界（time critical）数据，或在动态分页模式下操作以存储/重新获得程序或非时间关键的数据，结果是如果存在高速缓存缺失则存在等待时间。

在为静态分页模式配置区的情况下，数据读取一致性不是问题，因为 PNOR 部分 52 中的相同量的存储器空间总是映射到 RAM 存储器 16 中的相同量的空间中。然而，数据写入一致性仍然必须执行。但是，在为动态分页模式配置区的情况下，必须提供数据一致性。主机装置 20 能够配置该区以两个高速缓存一致性模式的一个进行操作。在第一模式中，主机装置 20 启动高速缓存一致性模式。在该模式中，主机装置 20 刷新（flush）RAM 存储器 16 中的高速缓存操作，如且当主机装置 20 需要时。在第二模式中，存储器控制器 12 通过刷新 RAM 存储器 16 中的高速缓存操作，如且当主机装置 20 需要时，来启动高速缓存一致性模式，以保持 RAM 存储器 16 中的高速缓存和 NAND 存储器 14 之间的数据的一致性。

一旦由用户设置了 PNOR 部分 52 的存储器空间的量和其到 RAM 存储器 16 的映射，RAM 存储器 16 中的可用存储器空间的剩余部分就可用于 RAM 存储器存取部分。如主机装置 20 所见的 RAM 存储器存取部分 54 在于，当主机 20 在该部分 54 中进行操作时，结果是对物理 RAM 存储器 16 进行的操作。因此，存储器部分 54 与物理 RAM 存储器 16 的映射是一对一的。进一步地，分配给 RAM 部分 54 的存储器空间的量依赖于在存储器装置 10 中可用的 RAM 存储器 16 的总量，以及 PONR 存储器 52 的存储器空间部分到 RAM 存储器 16 的映射程度。当主机认为其对 RAM 部分 54 进行操作时（如在发布读取/写入等的命令中），作为结果而发生的操作是直接对 RAM 存储器 16 进行的。该 RAM 部分 54 可以由正设法使用存储器空间作为缓冲区的主机装置 20 来使用。由于在每个区中的 PNOR 部分 52 的存储器空间到 RAM 存储器 16 的映射可以由用户来设置，并且 RAM 存储器 16 的总量是已知的，因此 PNOR 部分 52 和 RAM 部分 54 之间的边界间接地

由用户来设置。因此，如果需要具有大量的缓冲器，则可以通过在一个或多个区中减少PNOR部分52和RAM存储器16之间的映射来分配更大量的RAM部分54。此外，通过复位存储器控制器12，并在每个区中重建PNOR部分52的存储器空间和RAM存储器16之间的映射，PNOR部分52和RAM部分54之间的边界在存储器装置10的操作过程中可以改变。

对于RAM存储器16的每个区的存储器映射的边界和PNOR部分52的存储器空间的大小可以预先分配并存储到存储器控制器12中的非易失性结构寄存器60中。对于结构寄存器60的存取通过结构存取部分56来进行。非易失性的结构寄存器60可以是嵌入式NOR存储器62的一部分。可替换地，对于RAM存储器16的每个区的存储器映射的边界和PNOR部分52的存储器空间的大小可以由用户通过一个或多个芯片选择引脚来选择。在那种情况下，当存储器控制器12被加电时，不同存储器的边界能够重新设置。NOR存储器62还能够存储用于在启动期间通过存储器控制器12的执行以及用于存储器控制器12和MCU 64的操作的固件代码61。

最后，在大容量存储存取部分58中，当主机装置20存取存储器空间的该部分时，主机装置20认为其正在存取ATA盘驱动器。存储器控制器12使用公知的闪存文件系统（FFS）协议将逻辑ATA盘驱动器空间地址转变为NAND存储器14物理空间地址。在一个实施例中，对于读取操作，大容量存储存取部分58的开始部分包括加载到ATA任务文件寄存器79中的16字节逻辑地址。存储器控制器12解码该16字节的任务命令和逻辑地址并将其转变为用于存取NAND存储器14内的特定“页”的物理地址。读取来自NAND存储器14中的页的512字节的该页，然后将其加载到数据寄存器81中，在此由主机装置20顺序地或者随机地存取它们。对于写入操作，发生了反转。将要存储512字节的数据处的逻辑地址首先加载到任务文件寄存器79中。将写入命令写入到任务文件寄存器79中。存储器控制器12解码任务文件寄存器中的作为写入命令的命令并将其转变为物理地址以存取NAND存储器14中的该特定页，并在该位置将该512字节存储到数据寄存器81中。在另一个实施例中，可以存在采用所谓的乒乓（ping-pong）式结构的两个数据寄存器81（a和b）（未示出）。在那种情况下，数据寄存器中的一个81a被用于向主机装置20提供512字节的数据以及之前从NAND存储器14的一页加载的数据，而另一个数据寄存器81b用于将数据从NAND存储器14的另一页加

载到数据寄存器81b中，以在来自数据寄存器81a的数据被完全读出后将数据提供给主机装置20。以这种方式，能够发生跨越来自NAND存储器14的数据的多页的连续读取操作。数据寄存器81（a和b）也能够以乒乓方式用于写入操作，因此数据的多个连续页可以写入到NAND存储器14中并且具有很少的或没有等待设立时间。

如之前所讨论的，存储器装置10和主机装置20之间的接口连接可以通过串行总线进行。特别地，这样的串行总线可以连接存储器装置10的NOR或PNOR区域与主机装置20，且常规并行总线连接存储器装置10的RAM部分与主机装置20。

参考图3示出了与RAM存储器16和NAND存储器14接口连接的存储器控制器12的详细方框图。存储器控制器12具有微控制器64。微控制器64完成或执行FFS的所有簿记功能。此外，其完成或执行缺陷管理（DM）和高速缓存数据一致性算法，以及高速缓存刷新替换算法。最后，微控制器64完成或执行高速缓存分页方案算法。所有这些操作都是借助存储在NOR存储器62中的固件或程序代码61来实现的，包括存储器控制器12的启动操作或初始化。

微控制器64连接到第二NOR存储器62，其如之前所讨论的也存储用于通过微控制器64来执行的固件61。除了存储非易失性结构寄存器60之外，NOR存储器62还存储用于FFS和DM的操作的固件。

微控制器64还通过MUX 74与SRAM存储器46接口连接。SRAM存储器64用作微控制器64的局部高速缓冲器以存储运行时间数据。此外，SRAM存储器46能够存储缺陷映射高速缓存，和FFS数据结构。

尽管，相对于硬件部件对存储器控制器12进行了详细描述，但是下文中所描述的所有功能也可以采用用于通过微控制器64执行的软件来实现。

存储器控制器12包括当前高速缓存页地址寄存器66，其可以被实施为具有内容可寻址存储器66的性质。CAM 66的功能是当在对PNOR部分52的读取或写入操作期间存在存取失败时保持当前PNOR高速缓存页地址并更新CAM 66。CAM 66内的每个入口具有三个部分：页地址部分66a，索引地址部分66b，以及状态部分66c。随后关于存储器控制器和CAM存储器66的操作的讨论是关于下述实例的，然而应当理解本发明并不限于下述实例。假设来自主机装置20的地址为32比特，其包含21个最高有效位（位11—31）以及11个最低有效位（位0—

10)。该21个最高有效位包括页地址，而该11个最低有效位包含偏移地址。CAM存储器66中的每一个入口还包含包括21比特的页地址部分66a，包括9比特的索引地址部分66b，以及包括12比特的状态部分，其由下述构成：1比特的有效（或无效）；1比特的污损（dirty）（或干净（clean））；1比特的静态（或动态）；1比特的主机启动的高速缓存一致性（或控制器启动的）；以及8比特的最后存取时间标记。在32比特来自主机装置20的情况下，该主机装置能够寻址2^{32}字节或1GB量的存储器空间。如下文中将要讨论的，存储器控制器12使用来自CAM存储器66的9比特的索引地址部分与来自主机装置20的偏移地址的11比特来形成20比特地址，从而能够寻址1MB的RAM 16。当然，这些数字仅是作为实例的并且没有限制本发明。

存储器控制器12还包括命中/失败比较逻辑68。该命中/失败比较逻辑68从地址总线22接收地址信号，以及从控制总线32接收控制信号。然后该命中/失败比较逻辑68将来自主机装置20的32比特的地址的21比特的页地址发送到CAM存储器66。CAM存储器66将那些21比特的页地址与存储在CAM存储器66的每个入口中的页地址66a进行比较。如果命中，即来自主机装置20的该21比特的页地址与CAM存储器66中的入口之一相匹配，则CAM存储器66输出相关联的9比特的索引地址66b到MUX 70。如果失败，则该命中/失败比较逻辑68产生读取失败信号或写入失败信号。将该读取失败信号和写入失败信号提供给微代码控制器（MCC）/错误码校正（ECC）单元72作为用于MCC/ECC单元72执行数据一致性的信号。提供给MCC/ECC单元72的该信号是命中信号：其表明存储在RAM存储器16中的当前页地址中的一个是如在地址总线22上所提供的来自主机装置20的地址，或者是失败信号：其表明存储在RAM存储器16中的当前页地址中没有一个是如在地址总线22上所提供的来自主机装置20的地址。最后，该命中/失败比较逻辑68还连接到等待状态信号26。当存储器控制器12希望通知主机装置20存储器控制器12希望保持总线循环操作时产生等待状态信号26。等待状态信号26被取消声明（de-asserted）以释放总线22/24/32来允许主机装置20重新开始操作。被存储器控制器12声明（assert）的等待状态信号26的一个实例是在存在读取/写入失败并且存储器控制器12需要从NAND存储器14中的地址重新获得数据并将其加载到RAM存储器16中时。在从NAND存储器14重新获得数据并将其加载到RAM存储器16中的时间期间，由存储器控制器12

来声明等待状态信号 26。

存储器控制器 12 还包括在微控制器 64 的控制下进行操作的 MCC/ECC 单元 72。MCC/ECC 单元 72 监视读取失败/写入失败信号用于高速缓存数据一致性、刷新替换和分页操作。此外，在微控制器 64 的控制下，其操作 NAND 存储器 14 并且提供 NAND 存储器 14 的缺陷管理操作。进一步地，在微控制器 64 的控制下，MCC/ECC 单元 72 提供 DMA 功能以在 NAND 存储器 14、RAM 存储器 16 和 SRAM 存储器 46 之间移动数据。最后，MCC/ECC 单元 72 对存储在 NAND 存储器 14 中的数据执行错误检测和校正。

存储器控制器 12 还包括提供安全和数字版权管理的密码引擎 90。此外，存储器控制器 12 可以具有嵌入其中即形成在同一集成电路管芯上的附加 RAM 存储器 92，以用于增加 RAM 存储器 16 的量。如之前所表明的，RAM 存储器 16 可以是独立的集成电路管芯，在这种情况下，嵌入到存储器控制器 12 中的 RAM 存储器 92 扩充了 RAM 存储器 16。然而，如果 RAM 存储器 16 和存储器控制器 12 集成到相同管芯中，则 RAM 存储器 16 和 RAM 存储器 92 都可以是同一个存储器阵列的一部分。

现在将相对于所述多种操作模式来描述存储器装置 10。在加电期间，命中/失败比较逻辑 68 产生等待信号并声明该等待状态信号 26。存储器控制器 12 从非易失性寄存器 60 读取结构参数并将它们加载到非易失性寄存器 46（其可以是 SRAM 46 的一部分）。静态页，即静态地映射到 PNOR 部分 52 的来自 NAND 存储器 14 的数据也从 NAND 存储器 14 中读出并存储到 RAM 存储器 16 中。这由微控制器 64 通过 MCC/ECC 72 执行 FFS 协议以将来自 NAND 存储器 14 的页地址进行转变并产生物理地址和控制信号给 NAND 存储器 14 以从其重新获得数据并将它们存储到 RAM 存储器 16 中来完成。在加电期间，MCU 64 和 MCC/ECC 72 还扫描 NAND 存储器 14 以发现主索引表。读取主索引表并将其存储到本地 SRAM 存储器 46 中。MCU 64 将核对主索引表的数据结构完整性。MCU 64 和 MCC/ECC 72 也扫描 NAND 存储器 14 以确定是否需要重建主索引表。MCU 64 和 MCC/ECC 72 还将来自 NAND 存储器 14 的两页数据送入本地 SRAM 存储器 64 中。被称为 V 页的来自 NAND 存储器 14 的首先两页数据包含用于将主机装置 20 的逻辑地址映射到 NAND 存储器 14 的物理地址的数据并且具有跳过 NAND 存储器 14 中的有缺陷的扇区的能力。然后 FFS 准备好接受映射转变请求。然后命中/失败比较逻

辑 68 取消声明等待状态信号 26，即释放等待状态信号 26。

应当注意的是在加电期间，当存储器控制器 12 正从 NAND 存储器 14 重新获得静态页并将其存储到 RAM 存储器 16 中，以及执行其它辅助操作（overhead）功能，例如更新 NAND 存储器 14 的主索引表时，存储器装置 10 仍然可被主机装置 20 使用。特别地，由于等待状态信号 26 的声明只影响指向对存储器空间的 PNOR 部分 52 的寻址请求的那些操作，所以即使在加电期间 NOR 存储器 44 也可以被主机装置 20 存取。

NOR 存储器操作

在 NOR 存储器 44 读取操作中，主机装置 20 将在存储器空间的 NOR 存储器存取部分 50 内的地址总线 22 上的地址信号发送到存储器装置 10。此外，由主机装置 20 将在控制总线 32 上的适当的控制信号发送到存储器装置 10。由于地址信号处于除了在 PNOR 存储器存取部分 52 中以外的空间中，因此命中/失败比较逻辑 68 未被激活，并且等待状态信号 26 未被声明。将地址信号和控制信号提供给 NOR 存储器 44，在此读取来自于所提供的地址的数据。然后将该数据沿数据总线提供到 MUX 84 并且沿数据总线 24 向外提供到主机装置 20，从而完成读取循环。

在 NOR 存储器 44 写入或者编程操作中，主机装置 20 将在存储器空间的 NOR 存储器存取部分 50 内的地址总线 22 上的地址信号发送到存储器装置 10。此外，由主机装置 20 将在控制总线 32 上的适当的控制信号发送到存储器装置 10。由于地址信号处于除了在 PNOR 存储器存取部分 52 中以外的空间中，因此命中/失败比较逻辑 68 未被激活，并且等待状态信号 26 未被声明。将地址信号和控制信号提供给 NOR 存储器 44。将要被写入或编程的数据和程序命令沿数据总线 24 从主机装置 20 发送到存储器控制器 12 和 MUX 84 中。然后将数据从 MUX 84 发送到 NOR 存储器 44，在这里在地址总线 22 上所提供的地址处数据被编程到 NOR 存储器 44 中。主机装置 20 能够执行字节程序操作，允许将 NOR 存储器 44 以一个字节接一个字节为基础进行编程。当数据被写入到 NOR 存储器 44 中时，完成写入或编程循环。

在 NOR 存储器 44 擦除操作中，例如扇区擦除，或块擦除，主机装置 20 将在存储器空间的 NOR 存储器存取部分 50 内的地址总线 22 上的地址信号发送到存储器装置 10。此外，由主机装置 20 将在控制总线 32 上的适当的控制信号发送到存储器装置 10。由于地址信号处于除了在 PNOR 存储器存取部分 52 中以外的空

间中，因此命中/失败比较逻辑 68 未被激活，并且等待状态信号 26 未被声明。将地址信号和控制信号提供给 NOR 存储器 44。沿数据总线 24 将表示擦除命令协议的数据信号从主机装置 20 发送到存储器控制器 12 和 MUX 84 中。然后从 MUX 84 将数据发送到 NOR 存储器 44，在这里由 NOR 存储器 44 对数据进行解码然后执行擦除操作。当 NOR 存储器 44 完成擦除循环时，完成了擦除循环。

PNOR 存储器操作—读取

在 PNOR 存储器读取操作中，主机装置 20 将在存储器空间的 PNOR 存储器存取部分 52 内的地址总线 22 上的地址信号发送到存储器装置 10。存在两种可能性：读取命中和读取失败。

在读取命中的情况下，在地址总线 22 上提供的地址信号的页地址部分由命中/失败比较逻辑 68 接收，并与当前在 RAM 存储器 16 中的，如被存储在 CAM 66 中的地址进行比较。如果在地址总线 22 上提供的页地址在存储在 CAM 66 中的页地址之内，则命中。命中/失败逻辑 68 激活 MUX 70，以便然后将地址和控制信号引导到 RAM 存储器 16，并且将来自 CAM 存储器 66 的相关联的索引地址 66b 与来自主机装置 20 的偏移地址串接以寻址 RAM 存储器 16。然后将从 RAM 存储器 16 的较低地址读出的数据发送到 MUX 80，在这里然后将它们提供给 MUX 84（MUX 80 的默认状态），其已经被命中/失败比较逻辑 68 指示（未示出）允许将数据沿数据总线 24 发送到主机装置 20，从而完成读取循环。

在读取失败的情况下，存在多种可能性。首先是被称为无高速缓存刷新的读取失败的可能性。在来自地址总线 22 的地址信号的页地址部分与来自 CAM 66 的页地址寄存器 66a 的比较导致失败的情况下，即地址总线 22 上的页地址不在存储于 RAM 存储器 16 中的页地址之内，那么命中/失败比较逻辑 68 发送读取失败信号到 MCC/ECC 单元 72 以便 MCC/ECC 单元 72 启动读取一致性循环。此外，命中/失败比较逻辑 68 声明在等待状态信号 26 上的信号。在 MCU 64 的控制下，MCC/ECC 单元 72 执行 FFS 操作以将由主机装置 20 提供的地址转变为 NAND 存储器 14 中的物理地址。然后 MCC/ECC 单元 72 产生适当的地址和控制信号给 NAND 存储器 14，和适当的地址和控制信号给 RAM 存储器 16。

从 NAND 存储器 14 读取包含来自地址总线 22 上所指定的地址的数据的整页数据，并将其经过 MUX 80 传送到 RAM 存储器 16，在此其被写入到由 MCC/ECC 单元 72 所指定的 RAM 存储器 16 中的整页位置中，并且由 MCC/ECC

单元 72 在其上进行操作以通过错误校正检查等来确保数据的完整性。然后更新当前的页地址寄存器 CAM 66 以在当前读取失败地址内添加该地址页的地址。命中/失败比较逻辑 68 取消声明在等待状态信号 26 上的信号。此外，MCU 64 切换 MUX 80 到默认位置。命中/失败比较逻辑 68 发送索引地址 66b 到 MUX 70，在这里其与来自地址总线 22 的偏移地址部分相结合，以寻址 RAM 存储器 16。然后来自对 RAM 存储器 16 的该读取操作的数据通过 MUX 80 以及通过 MUX 84 被提供到至主机装置 20 的数据总线 24，从而完成该循环。由于从 NAND 存储器 14 读出的数据的量是以页为基础的，因此整页的数据必须被存储到 RAM 存储器 16 中。这种没有高速缓存刷新的读取失败的情况假设 RAM 存储器 16 的整页可用于存储来自 NAND 存储器 14 的数据，或者将存储整页数据的 RAM 存储器 16 中的位置包含一致的数据（和 NAND 存储器 14 中的数据相同），然后从 NAND 存储器 14 读出的整页的数据能够被存储到 RAM 存储器 16 中的位置中。高速缓存刷新意味着从 RAM 存储器 16 到 NAND 存储器 14 的数据写入，由此刷新数据一致性问题的高速缓存（RAM 存储器 16）。

读取失败的另一个可能的情况被称为具有高速缓存刷新的读取失败。在该情况下，在不重写 RAM 存储器 16 中某些比 NAND 存储器 14 中的数据更新的数据的情况下，来自 NAND 存储器 14 的整页数据不能被存储在 RAM 存储器 16 中。这产生了数据一致性问题。因此，在来自 NAND 存储器 14 的处于不同位置的数据可以被读取到 RAM 存储器 16 中之前，RAM 存储器 16 中的数据页必须首先写入到 NAND 存储器 14 中。操作顺序如下。来自主机装置 20 的地址总线 22 的地址信号的页地址部分与来自 CAM 66 的页地址信号 66a 进行比较以确定是否来自地址总线 22 的地址信号在当前页地址的任何一个之内。该比较导致失败，使得命中/失败比较逻辑 68 发送读取失败信号到 MCC/ECC 单元 72 以便 MCC/ECC 单元 72 启动读取一致性循环。此外，命中/失败比较逻辑 68 声明在等待状态信号 26 上的信号。MCC/ECC 单元 72 在 MCU 64 的控制下确定 RAM 存储器 16 中的数据页必须首先写入到 NAND 存储器 16 中，因为存在数据一致性问题来自 NAND 存储器 14 的数据应当被读取到 RAM 存储器 16 中。MCU 64 执行 FFS 操作以将来自 RAM 存储器 16 的地址转变为 NAND 存储器 14 中的地址。

从 RAM 存储器 16 读取整页的数据，该整页的数据经过 MUX 80 并提供到 NAND 存储器 14，在此将它们存储到 NAND 存储器 14 中。其后，由 MCU 64 通

过 FFS 操作将来自主机装置 20 的地址变换为物理 NAND 地址。然后在 MCU 64 的指示下 MCC/ECC 单元 72 产生适当的地址和控制信号给 NAND 存储器 14 并且使用来自 CAM 存储器 66 的索引地址 66b、控制信号和来自 MCC/ECC 72 的偏移地址部分来寻址 RAM 存储器 16。从 NAND 存储器 14 读出的整页的数据之后被通过 MUX 80 从 NAND 存储器 14 传送到 RAM 存储器 16，在此其被写入到由 MCC/ECC 单元 72 和索引地址 66b 所指定的 RAM 存储器 16 中的位置页中，并且通过 MCC/ECC 单元 72 在其上被操作以通过错误校正检查等确保数据的完整性。CAM 66 的当前页地址寄存器 66a 之后被更新以添加包含当前读取失败地址的页地址，以及与其相关联的索引地址 66b。命中/失败比较逻辑 68 取消声明在等待状态信号 26 上的信号。此外，MCU 64 将 MUX 80 切换到默认位置。命中/失败比较逻辑 68 发送索引地址 66a 到 MUX 70，在此它们和来自地址总线 22 的偏移地址结合以启动 RAM 存储器 16 中的读取操作。然后将该数据从 RAM 存储器 16 中读出，并且通过 MUX 80 以及通过 MUX 84 将该数据提供到至主机装置 20 的数据总线 24，从而完成读取循环。

在读取命中、没有高速缓存刷新的读取失败、以及具有高速缓存刷新的读取失败的每种情况下，从主机装置 20 的角度来观察，该操作与对 RAM 装置的读取没有任何的不同，且在读取失败的情况下存在等待时间。主机装置 20 不必处理地址转变和/或数据一致性。

PNOR 存储器操作—写入

在 PNOR 存储器写入操作中，主机装置 20 将在存储器空间的 PNOR 存储器存取部分 52 内的地址总线 22 上的地址信号连同将被写入到 RAM 存储器 16 中的数据一起发送到存储器装置 10。存在两种可能性：写入命中和写入失败。

在写入命中的情况下，在地址总线 22 上提供的地址信号的页地址部分由命中/失败比较逻辑 68 来接收，并与 CAM 66 中的页地址 66a 进行比较，其反映当前存储在 RAM 存储器 16 中的数据。在地址总线 22 上提供的页地址在 CAM 66 中所存储的页地址之内。命中/失败逻辑 68 激活 MUX 70 以便然后将地址和控制信号引导到 RAM 存储器 16。来自 CAM 66 的索引地址 66b 和来自地址总线 22 的地址信号的偏移地址部分相结合以产生用于通过 MUX 70 存取 RAM 存储器 16 的地址信号。通过 MUX 84 提供来自数据总线 24 的数据并通过 MUX 80 将该数据提供给 RAM 存储器 16，在此其然后被写入到 RAM 存储器 16 中，从而完成写

入命中循环。

应当注意的是在写入命中操作之后，RAM 存储器 16 中的数据将与来自 NAND 存储器 14 中的同样位置的数据不一致。实际上，RAM 存储器 16 中的数据将是最当前的数据。为了解决数据一致性的问题，存在两种解决方案。

第一，在按照需要的基础上，存储器装置 10 能够自动解决数据一致性的问题。如之前所讨论的，例如，在具有高速缓存刷新操作的读取失败的情况下，如果 RAM 存储器 16 中的数据页需要被替换以存储新要求的来自 NAND 存储器 14 的数据页，则 RAM 存储器 16 中的更为当前的数据将被写回到 NAND 存储器 14 中。如下文将要讨论的，MCU 64 还将通过在具有高速缓存刷新操作的写入失败中将数据写回到 NAND 存储器 14 中来对 RAM 存储器 16 中的数据执行高速缓存刷新。

对于数据一致性问题的替换解决方案是在主机装置 20 的控制下执行数据一致性。因此，主机装置 20 可以发布高速缓存刷新命令使得存储器控制器 12 将来自 RAM 存储器 16 的不一致的数据写回到 NAND 存储器 14 中。该操作的优点是其能够由主机装置 20 在任何时间执行，包含但是不限于关键事件，例如改变应用，关闭，或接收到的低功率中断。然而，由于存储器控制器 12 还能够自动执行数据一致性，在主机装置 20 的用户未能执行数据一致性操作的情况下，这样的操作还将根据需要由存储器控制器 12 来执行。

在写入失败的情况下，存在多种可能性。首先是被称为没有高速缓存刷新的写入失败的可能性。在来自地址总线 22 的地址信号的页地址部分与来自 CAM 66 的页地址信号 66a 的比较导致失败的情况下，即地址总线 22 上的地址不在存储于 RAM 存储器 16 中的页地址之内，那么命中/失败比较逻辑 68 发送写入失败信号到 MCC/ECC 单元 72。此外，命中/失败比较逻辑 68 声明在等待状态信号 26 上的信号。MCC/ECC 单元 72 确定是否来自 NAND 存储器 14 的新数据页，包含来自主机装置 20 的在地址总线 22 上所指定的地址处的数据，将存储在旧的一致数据或 RAM 存储器 16 的空白区域之上。在那种情况下，在将数据从 NAND 存储器 14 传送到 RAM 存储器 16 中的位置之前，不需要存储器控制器 12 执行写入一致性循环。MCC/ECC 单元 72 在 MCU 64 的控制下执行 FFS 操作来将由主机装置 20 提供的地址转变成 NAND 存储器 14 中的物理地址。然后 MCC/ECC 单元 72 产生适当的地址和控制信号给 NAND 存储器 14，以及适当的地址和控制信号给 RAM

存储器 16。

包含来自在地址总线 22 上所指定的地址的数据的整页的数据，被从 NAND 存储器 14 中读出并经过 MUX 80 传送到 RAM 存储器 16，在此其被写入到由 MCC/ECC 单元 72 和索引地址 66b 所指定的 RAM 存储器 16 中的整页位置中，并且通过 MCC/ECC 单元 72 在其上被操作以通过错误校正检查等确保数据的完整性。然后更新 CAM 66 的当前页地址寄存器 66a 以在当前的写入失败地址和相关联的索引地址 66b（索引地址 66b 是 RAM 存储器 16 中的较高的 9 比特地址，在此存储数据页）内添加该地址页的地址。命中/失败比较逻辑 68 取消声明在等待状态信号 26 上的信号。此外，MCU 将 MUX 80 切换到默认位置。命中/失败比较逻辑 68 发送索引地址 66b 到 MUX 70，在此它们与来自地址 22 的偏移地址相结合，以启动 RAM 存储器 16 中的写入操作。然后从主机装置 20 经过 MUX 84 以及经过 MUX 80 将数据写入到 RAM 存储器 16 中，从而完成该循环。现在在 RAM 存储器 16 中的数据不再与在 NAND 存储器 14 中的相同地址处的数据相一致。该一致性问题由存储器控制器 12 自动地根据需要启动写入高速缓存刷新来解决，或由主机装置 20 在任何时间启动写入高速缓存刷新来解决，全部都如之前所讨论的。

另一个写入失败的可能的情况被称为具有高速缓存刷新的写入失败。在该情况下，在不重写 RAM 存储器 16 中某些比 NAND 存储器 14 中的数据更新的数据的情况下，来自 NAND 存储器 14 的整页的数据不能被存储到 RAM 存储器 16 中。这产生数据一致性问题。因此，在来自 NAND 存储器 14 的处于不同位置的数据能够被读取到 RAM 存储器 16 中之前，RAM 存储器 16 中的数据页必须首先被写入到 NAND 存储器 14 中。操作的顺序如下。来自主机装置 20 的地址总线 22 的信号的页地址部分与来自 CAM 66 的页地址信号 66a 进行比较以确定是否来自地址总线 22 的地址信号在当前页地址的任何一个之内。该比较导致失败，使命中/失败比较逻辑 68 发送写入失败信号到 MCC/ECC 单元 72 以便 MCC/ECC 单元 72 启动写入一致性循环。此外，命中/失败比较逻辑 68 声明在等待状态信号 26 上的信号。因为存在数据一致性问题来自 NAND 存储器 14 的数据应当被读取到 RAM 存储器 16 中，所以 MCC/ECC 单元 72 在 MCU 64 的控制下确定 RAM 存储器 16 中的数据页必须首先写入到 NAND 存储器 16 中。MCU 单元 64 执行 FFS 操作以将来自 RAM 存储器 16 的地址转变为 NAND 存储器 14 中的地址。

从RAM存储器16读取整页数据，并且该整页数据经过MUX 80并提供到NAND存储器14，在此它们被存储到NAND存储器14中。其后，通过FFS操作将来自主机装置20的地址变换为物理NAND地址。然后MCC/ECC单元72使用来自FFS的物理NAND地址产生适当的地址和控制信号给NAND存储器14，以及索引地址和控制信号给RAM存储器16。然后将自NAND存储器14读取的整页的数据从NAND存储器14经过MUX 80传送到RAM存储器16，在此其被写入到借助来自MCC/ECC单元72的偏移地址和来自索引地址寄存器66b的索引地址所指定的RAM存储器16中的位置页中，并且通过MCC/ECC单元72在其上被操作以通过错误校正检查等确保数据的完整性。然后将CAM 66的当前页地址寄存器进行更新以添加包含当前读取失败地址的页地址66a和相关联的索引地址66b。命中/失败比较逻辑68取消声明在等待状态信号26上的信号。此外，MCU将MUX 80切换到默认位置。命中/失败比较逻辑68发送索引地址66b到MUX 70，在此它们与来自地址总线22的偏移地址相结合以形成写入到RAM存储器16中的地址。然后从主机装置20到数据总线24经过MUX 84并且经过MUX 80将数据写入到RAM存储器16中。与前面关于没有高速缓存刷新的写入失败的讨论相类似，现在RAM存储器16中的数据是更为当前的并且产生了数据一致性问题，该问题能够通过主机装置20启动高速缓存刷新，或通过存储器控制器12启动高速缓存刷新操作来解决。

在写入命中，没有高速缓存刷新的写入失败、和具有高速缓存刷新的写入失败的每一种情况下，从主机装置20的角度来观察，该操作与对RAM装置的写入没有任何的不同，且在写入失败的情况下具有等待时间。主机装置20不必处理地址转变和/或数据一致性。

为了进一步减小在具有高速缓存刷新的读取失败或具有高速缓存刷新的写入失败的情况下由首先执行从RAM存储器16到NAND存储器14的写入操作以解决数据一致性问题的需要所引起的等待时间，可以执行如下操作。将被写入到NAND存储器14中的数据页首先从RAM存储器16写入到本地SRAM 46中。这是比直接写入到NAND存储器14中快得多的操作。其后，具有高速缓存刷新的读取失败或写入失败高速缓存刷新操作继续进行，似乎其是没有高速缓存刷新的读取失败或没有高速缓存刷新操作的写入失败。在读取失败或写入失败操作完成后，当存储器装置10空闲或存取局限于在NOR存储器存取部分50或RAM存

储器存取部分 54 或结构寄存器存取部分 56 中的操作时，存储在本地 SRAM 46 中的数据能够在后台操作中被写入到 NAND 存储器 14 中。

应当注意，在 PNOR 操作中，从主机装置 20 的角度来观察，该操作与对 RAM 存储器所执行的没有任何的不同，且数据是非易失性的，但是主机装置 20 不发布 NOR 协议命令，例如扇区或块擦除。然而，在本发明内存储器装置 10 还能够使用 RAM 存储器 16 和 NAND 存储器 14 模拟 NOR 操作。在那样的情况下，对于 NOR 存储器存取部分 50 进行映射的存储器空间将延伸以超过仅对 NOR 存储器 44 的映射。NOR 存储器存取部分 50 能够被映射到 RAM 存储器 16 的一部分，且 RAM 存储器 16 被静态地映射到 NAND 存储器 14，从而在存取的过程中不出现等待问题。来自 NAND 存储器 14 的数据在加电时将被加载到 RAM 16 中，并且对 NOR 存储器存取部分 50 的读取/写入将从 RAM 存储器 16 读取或写入到 RAM 存储器 16。仅其它的变化将用于存储器控制器 12 响应于 NOR 协议命令。如之前所讨论的，当由主机装置 20 发布这样的 NOR 协议命令时，它们被提供作为唯一的数据模式的序列。在数据总线 24 上提供的数据将经过 MUX 84 并且经过 MUX 80。由于在地址总线上提供的地址表明操作将在由 RAM 存储器 16 所模拟的 NOR 存储器存取部分 50 中进行，因此切换 MUX 74 以允许 MCU 64 接收该数据模式。一旦该数据模式被解码为 NOR 命令，则 MCU 利用那些 NOR 命令操作 NAND 存储器 14，如果例如该命令为擦除。当然，作为易失性存储器的 RAM 存储器 16 不必被“擦除”。因此，借助模拟 NOR 存储器 44 的 RAM 存储器 16，NOR 协议命令的执行将导致比执行 NOR 协议命令的真实 NOR 存储器 44 更快的操作。进一步地，该模拟操作不需要模拟全部 NOR 协议命令集。代替地，控制器 12 能够模拟部分 NOR 协议命令集。因此，如这里所使用的，术语“NOR 协议命令”表示来自由例如英特尔公司或 AMD 公司所发布的全部 NOR 协议命令集的一个或多个命令。

RAM 存储器操作

在 RAM 存储器 16 读取操作中，主机装置 20 将在存储器空间的 RAM 存储器存取部分 54 内的地址总线 22 上的地址信号发送到存储器装置 10。此外，由主机装置 20 将在控制总线 32 上的适当的控制信号发送到存储器装置 10。由于地址信号在 RAM 存储器存取部分 54 中，因此命中/失败比较逻辑 68 激活 MUX 70 以允许来自地址总线 22 和控制总线 32 的地址/控制信号被提供给 RAM 存储器 16。

然而，等待状态信号 26 没有被声明。此外，来自主机装置 20 的地址被解码并且连同来自控制总线 32 的控制信号一起形成提供给 RAM 存储器 16 的地址信号，在此读取来自所提供的地址的数据。然后将该数据沿数据总线提供到 MUX 80 和 MUX 84 并且沿数据总线 24 向外提供到主机装置 20，从而完成读取循环。

在 RAM 存储器 16 写入操作中，主机装置 20 将在存储器空间的 RAM 存储器存取部分 54 内的地址总线 22 上的地址信号发送到存储器装置 10。此外，由主机装置 20 将在控制总线 32 上的适当的控制信号发送到存储器装置 10。由于地址信号在 RAM 存储器存取部分 54 中，因此命中/失败比较逻辑 68 激活 MUX 70 以允许来自地址总线 22 和控制总线 32 的地址/控制信号被提供给 RAM 存储器 16。然而，等待状态信号 26 没有被声明。此外，来自主机装置 20 的地址被解码并且连同来自控制总线 32 的控制信号一起形成提供给 RAM 存储器 16 的地址信号，在此将来自数据总线 24 的数据在所提供的地址处写入到 RAM 存储器 16 中。

由主机装置 20 的观察，RAM 存储器存取部分中的读取或写入操作与存取 RAM 装置没有任何的不同且没有等待。

结构寄存器操作

在结构寄存器操作中，主机装置 20 将在存储器空间的结构寄存器存取部分 56 内的地址总线 22 上的地址信号发送到存储器装置 10。此外，由主机装置 20 将在控制总线 32 上的适当的控制信号发送到存储器装置 10。然后将数据写入到非易失性寄存器 60 中。

NAND 存储器操作

在 NAND 存储器 14 读取操作中，主机装置 20 将在存储器空间的大容量存储存取部分 58 或 ATA 存储器存取部分 58 内的地址总线 22 上的地址信号发送到存储器装置 10。此外，由主机装置 20 将在控制总线 32 上的适当的控制信号发送到存储器装置 10。由于地址信号处于除了在 PNOR 存储器存取部分 52 中以外的空间中，因此命中/失败比较逻辑 68 未被激活，并且等待状态信号 26 未被声明。主机装置 20 遵从 ATA 协议以对于 ATA 读取/写入命令来读取/写入任务文件寄存器 79。任务文件寄存器 79 包括用于存储：命令、状态、柱面（cylinder）、磁头（head）、扇区等的寄存器。MCC/ECC 单元 72 在 MCU 64 的控制下操作将主逻辑地址转变为 NAND 物理地址的闪存文件系统，且具有避免使用有缺陷的 NAND 扇区的能力。参考美国专利 6,427,186；6,405,323；6,141,251 和 5,982,665，其公开的全部内

容被并入作为参考。每个来自主机装置20的逻辑地址在被称为V页的表中具有入口。该入口的内容指向存储逻辑地址数据的物理地址。

为了从NAND存储器14读取数据页，将地址信号和控制信号提供给NAND存储器14。主机装置20遵从ATA协议，并且任务文件寄存器79存储命令和逻辑地址。每个扇区大小为512字节。主机装置20通过读取存储器空间的任务文件寄存器存取部分58中的状态寄存器79来检验存储器10是否准备就绪。主机装置20将“读取”命令写入到存储器空间58内的命令寄存器79中。MCU 64执行逻辑地址到物理地址的FFS转变并且MCC/ECC单元72在MCU 64的控制下从NAND存储器14读取数据，并将数据页传送到缓冲器81中。在整页数据被存储到数据寄存器81中，并且通过MCC/ECC单元72在其上被操作以通过错误校正检查等确保数据的完整性之后，沿数据总线24将数据从存储器控制器12中读出。

写入NAND存储器14的操作与从NAND存储器14读取的操作相类似。主机装置20通过读取任务存储器空间58部分中的状态寄存器79来检查存储器10是否准备就绪。主机装置20将一页数据写入到数据寄存器81中，然后将“写入”命令和逻辑地址一起写入到命令寄存器79中。其后，使用FFS的MCU 64将逻辑地址转变为物理地址并且MCC/ECC单元72在MCU 64的控制下将来自ATA缓冲器81的该一页数据写入到NAND存储器14中。

FFS通过定位将要被更新的页的物理地址来更新数据页。FFS发现已擦除的扇区作为“缓冲器扇区”或者如果没有已擦除的扇区，则其首先对扇区执行擦除操作。然后FFS读取旧的还没有被修改并且编程到缓冲器扇区的数据。然后FFS将更新的页数据进行编程。然后其等待下一请求。如果下一页在同一个擦除扇区上，则FFS继续更新操作。如果下一页在正传送的擦除扇区之外，则未修改数据的其余部分将被复制到缓冲器扇区。映射表入口被改变为缓冲器扇区物理地址。然后开始新的页更新操作。

参考图4示出了存储器装置10的第二实施例。存储器装置110与图1所示的存储器装置10相类似。因此，类似的数字代表类似的部分。存储器装置110和存储器装置10之间唯一的不同点为在存储器装置100中，第二RAM总线40直接将RAM存储器100连接到主机装置20，而不是连接到存储器控制器12。因此，在存储器装置110中，主机装置具有对RAM存储器100的直接存取和控制。

存储器装置10的实施例和存储器装置110的实施例之间的该不同点反映在

图5所示的存储器映射中。与存储器装置10类似，对存储器装置10的存储器映射包括映射到NOR存储器44的NOR存储器存取部分50、映射到存储器装置110中的RAM存储器16的PNOR存储器存取部分52，其然后被映射到NAND存储器14、以及映射到RAM存储器16的RAM存储器存取部分54。然而，在RAM存储器100可直接被主机装置20通过第二RAM总线40存取的情况下，对存储器装置110的存储器映射还包含另一个RAM存储器存取部分55，其直接映射到RAM存储器100。然后存储器装置110进一步包括结构寄存器存取部分56，以及最后包括ATA存储器存取部分58，其与关于存储器装置10所描述的类似。

在存储器控制器12与主机装置20和NAND存储器14接口连接的情况下，存储器装置10比现有技术中的存储器装置提供更多的保护。特别地，存储器控制器12能够限制对存储在NAND存储器14中的特定数据的存取，如在涉及数字版权管理的关注中。进一步地，存储器控制器12能够加密存储于NAND存储器14中的数据来保护敏感的数据。最后，存储器控制器12能够提供保护以避免NAND存储器14的一个或多个特定部分中的意外数据擦除。最后利用存储在NOR存储器62中的程序，存储器控制器12成为自启动装置，因为它不需要来自主机装置20的初始命令。

参考图6，示出了本发明的存储器装置210的方框图。该存储器装置210类似于存储器装置10。它包括类似于存储器控制器12、连接到NAND存储器14和RAM存储器16的存储器控制器112。该控制器112被连接到单个总线23，其是图1中所示的第一RAM地址总线22、第一RAM数据总线24、和第一RAM控制总线32的集合。然而，不同于图1所示的实施例，该单个总线23被连接到多个处理器120（a-c）。该多个处理器120（a-c）中的每一个可以对总线23进行存取，从而对存储器装置210存取。因此，该单个总线23被所有处理器120（a-c）共享。

为了由处理器120（a-c）中的每一个存取存储器装置210，每个处理器120具有向控制器112发送信号请求允许存取总线23的相关联的总线请求信号线122、以及来自存储器装置210的控制器112的许可该请求的总线许可信号线124。因而，当由控制器112对处理器120之一许可允许时，至其他处理器120的总线许可线124将处于禁止模式。每个处理器120可以存取如图2所示的存储器装置210中的所有存储器空间，或者存储器装置210中的存储器空间可以被划分使得

仅特定地址空间可用于特定处理器 120。存储器装置 210 的实施例的缺点在于所有处理器 120 必须共享同一总线 23。因此可能存在性能损失（performance hit）。

参考图 7，示出了本发明的存储器装置 310 的另一个实施例的方框图。存储器装置 310 类似于存储器装置 210。它包括连接到 NAND 存储器 14 和 RAM 存储器 16 的存储器控制器 212。存储器控制器 212 被连接到三个总线 23（a-c），其每一个是图 1 中所示的第一 RAM 地址总线 22、第一 RAM 数据总线 24 和第一 RAM 控制总线 32 的集合。总线 23（a-c）的每一个连接到单个处理器 120（a-c）。该多个处理器 120（a-c）中的每一个可以存取它的总线 23，由此对存储器装置 310 进行存取。

进一步地，存储器控制器 212 包括多个控制器 12（a-c），且每个控制器 12 具有专用的相关联的 NOR 存储器 44 和 SRAM 存储器 46。因此，每个处理器 120 具有相关联的专用总线 23 和相关联的专用控制器 12。因而，与图 6 所示的存储器装置 210 的实施例不同，每个处理器 120 无需请求（和等待）总线许可。此外，由于每个控制器 12 具有专用的 NOR 存储器 44，因此图 2 所示的地址空间中的 NOR 存储器存取部分 50 可被每个处理器 120 单独寻址。此外，每个处理器 120 专用的每个控制器 12 中的 SRAM 46 用作专用于为该处理器 120 服务的一级高速缓存。存储器装置 310 具有 NAND 存储器 14 和 SDRAM 存储器 16，其通常被所有处理器 120 共享。因而，对 NAND 存储器 14 或者 SDRAM 存储器 16 的存取的请求必须提供给仲裁电路 250。结果，控制器 12 请求对 SDRAM 存储器 16 进行存取，它在至仲裁电路 250 的总线请求线上请求，并且仲裁电路 250 通过发送总线许可信号给进行请求的控制器 12 来进行响应。然后仲裁电路 250 禁止其它控制器 12 对该总线的存取。这类似于前面关于图 6 所示的对总线 23 的存取所述的方案。类似于图 1 所示和所描述的实施例，从存储器控制器 212，单个总线 40 连接到 SDRAM 16，并且单个总线 42 连接到 NAND 存储器 14。

在操作中，当存在命中时在处理器 120 的一侧不存在性能退化。当每个处理器请求对 NOR 存储器地址空间 50 存取时，也不存在性能退化。如果每个处理器 120 请求在 PNOR 空间 52 或 RAM 地址空间 54 中的地址并且存在一级高速缓存失败，即在相关联的 SRAM 46 中未发现数据，那么每个控制器 12 访问仲裁电路 250，寻求对至 SDRAM 16 的总线的控制。如果二级高速缓存也失败，则控制器 12 将寻求对至 NAND 存储器 14 的总线的控制。当从 NAND 存储器 14 中重新获

得数据以填充二级高速缓存存储器 SDRAM 16 时，相同的数据也可以写入到进行请求的控制器 12 的一级高速缓存 SRAM 存储器 46 中（取决于 SDRAM 存储器 46 的大小）。如果所有处理器 120（a-c）使用单独的地址范围，则将保持单个高速缓存。如果所有处理器 120（a-c）共享相同的地址范围，则将使用修改、独占、共享、无效（MESI）高速缓存协议。具有单个高密度存储器 SDRAM 存储器 16 或 NAND 存储器 14 比多个低密度存储器更节省成本。

参考图 8，示出了本发明的存储器装置 410 的另一实施例的方框图。存储器装置 410 类似于存储器装置 310。它包括类似于存储器控制器 212 的存储器控制器 312，其通过单个总线 42 连接到 NAND 存储器 14，并通过多个总线 40（a-c）连接到多个 RAM 存储器 16。存储器控制器 312 连接到三个总线 23（a-c），其每一个是图 1 中所示的第一 RAM 地址总线 22、第一 RAM 数据总线 24 和第一 RAM 控制总线 32 的集合。总线 23（a-c）中的每一个连接到相关联的处理器 120（a-c）。该多个处理器 120（a-c）中的每一个可以存取其总线 23，从而对存储器装置 410 进行存取。

此外，存储器控制器 312 包括多个控制器 12（a-c）且每个控制器 12 具有专用的相关联的 NOR 存储器 44 和 SRAM 存储器 46，以及具有相关联的专用 SDRAM 存储器 16。因此，每个处理器 120 具有相关联的专用总线 23、相关联的专用控制器 12、和相关联的 SDRAM 存储器 16。因而，与图 7 所示的存储器装置 310 的实施例不同，如果期望对存储在 SDRAN 存储器 16 中的二级高速缓存进行存取，则每个处理器 120 无需请求（和等待）总线许可。此外，由于每个控制器 12 具有专用的 NOR 存储器 44，因此 NOR 存储器存取部分 50 可被每个处理器 120 单独寻址。此外，每个控制器 12 中的 SRAM 46 和每个处理器 120 专用的 SDRAM 16 用作专用于为该处理器 120 服务的一级和二级高速缓存。存储器装置 410 具有 NAND 存储器 14，其通常被所有处理器 120 共享。因而，对 NAND 存储器 14 的存取的请求必须提供给仲裁电路 250。

在操作中，当存在命中时在处理器 120 的一侧不存在性能退化。当每个处理器请求对 NOR 存储器地址空间 50 存取时，也不存在性能退化。如果每个处理器 120 请求在 PNOR 空间 52 或 RAM 地址空间 54 中的地址并且存在一级高速缓存失败，即在相关联的 SRAM 46 中未发现数据，那么每个控制器 12 访问相关联的 SDRAM 存储器 16。如果二级高速缓存也失败，则控制器 12 将寻求对至 NAND

存储器 14 的总线的控制。当从 NAND 存储器 14 中重新获得数据时，它填充二级高速缓存存储器 SDRAM 16。如果所有处理器 120（a-c）使用单独的地址范围，则将保持单个高速缓存。如果所有处理器 120（a-c）共享相同的地址范围，则将使用修改、独占、共享、无效（MESI）高速缓存协议。具有单个高密度 NAND 存储器 14 比多个低密度存储器更节省成本。

参考图 9，示出了本发明的存储器装置 510 的另一实施例的方框图。存储器装置 510 类似于存储器装置 410。它包括类似于存储器控制器 312 的存储器控制器 412，其通过单个总线 42 连接到 NAND 存储器 14。存储器控制器 312 连接到三个总线 23（a-c），其每一个是图 1 中所示的第一 RAM 地址总线 22、第一 RAM 数据总线 24 和第一 RAM 控制总线 32 的集合。总线 23（a-c）的每一个连接到相关联的处理器 120（a-c）。该多个处理器 120（a-c）中的每一个可以存取其总线 23，从而对存储器装置 410 进行存取。

此外，存储器控制器 312 还包括多个控制器 12（a-c）且每个控制器 12 具有集成在其中的专用的相关联的 NOR 存储器 44 和 SRAM 存储器 46 以及 SDRAM 16。因而，与图 8 所示的存储器装置 410 的实施例不同，存储器装置 510 不具有在存储器控制器 412 外部将存储器控制器 412 连接到 SDRAM 16 的任何总线 40。在所有其他方面中，存储器装置 510 与存储器装置 410 类似。

本发明存在多个方面。首先，存储器装置 10、110、210、310、410 或 510 为通用的存储器装置。该存储器装置具有存储器控制器，该存储器控制器具有用于接收 RAM 地址信号的第一地址总线，用于接收 RAM 数据信号的第一数据总线，以及用于接收 RAM 控制信号的第一控制总线。存储器控制器具有嵌入在其中的 NOR 存储器并且进一步具有用于接口连接易失性的 RAM 存储器的第二地址总线，用于接口连接易失性的 RAM 存储器的第二数据总线，以及用于接口连接易失性的 RAM 存储器的第二控制总线。该控制器进一步具有用于接口连接非易失性 NAND 存储器的第三地址/数据总线，和用于接口连接非易失性 NAND 存储器的第三控制总线。该存储器装置进一步具有连接到所述第二地址总线，所述第二数据总线和所述第二控制总线的 RAM 存储器。该存储器装置进一步具有连接到第三地址/数据总线和第三控制总线的非易失性 NAND 存储器。该控制器响应于在第一地址总线上提供的地址信号，由此 NOR 存储器响应于在第一地址总线上提供的第一地址范围，由此 RAM 存储器响应于在第一地址总线上提供的第二地

址范围，以及由此NAND存储器响应于在第一地址总线上提供的第三地址范围。

在本发明的另一方面中，该存储器装置是通用的存储器装置，其中用户能够限定存储器空间分配。该存储器装置具有存储器控制器，该存储器控制器具有用于接收RAM地址信号的第一地址总线，用于接收RAM数据信号的第一数据总线，和用于接收RAM控制信号的第一控制总线。该存储器控制器具有嵌入在其中的NOR存储器并且进一步具有用于接口连接易失性RAM存储器的第二地址总线，用于接口连接易失性RAM存储器的第二数据总线，以及用于接口连接易失性RAM存储器的第二控制总线。该控制器进一步具有用于接口连接非易失性NAND存储器的第三地址/数据总线，和用于接口连接非易失性NAND存储器的第三控制总线。该存储器装置进一步具有与所述第二地址总线，所述第二数据总线，以及所述第二控制总线相连接的RAM存储器。该存储器装置进一步具有与第三地址/数据总线和第三控制总线相连接的非易失性NAND存储器。该存储器装置响应于限定存储器空间分配的用户，其中在第一地址总线上提供的第一地址范围内，该存储器装置响应于NOR存储器操作，包含响应于NOR协议命令，以及在第一地址总线上提供的第二地址范围内，该存储器装置响应于RAM操作，以及在地址总线上提供的第三地址范围内，该存储器装置响应于用作ATA盘驱动装置的NAND存储器，其中第一，第二和第三地址范围都可以由用户限定。

在本发明的另一方面中，该存储器装置具有存储器控制器，该存储器控制器具有用于接收RAM地址信号的第一地址总线，用于接收RAM数据信号的第一数据总线，和用于接收RAM控制信号的第一控制总线。该存储器控制器进一步具有用于接口连接易失性RAM存储器的第二地址总线，用于接口连接易失性RAM存储器的第二数据总线，以及用于接口连接易失性RAM存储器的第二控制总线。该控制器进一步具有用于接口连接非易失性NAND存储器的第三地址/数据总线，和用于接口连接非易失性NAND存储器的第三控制总线。该存储器装置进一步具有与所述第二地址总线，所述第二数据总线，以及所述第二控制总线相连接的RAM存储器。该存储器装置进一步具有与第三地址/数据总线和第三控制总线相连接的非易失性NAND存储器。该控制器进一步具有用于接收第一地址总线上的第一地址并将第一地址映射到非易失性NAND存储器中的第二地址的装置，且易失性RAM存储器对于到或来自非易失性NAND存储器中的第二地址的数据用作高速缓存，以及用于保持存储于作为高速缓存的易失性RAM存储器中

的数据和在非易失性 NAND 存储器中的第二地址处的数据之间的数据一致性的装置。另外，用于保持存储于易失性 RAM 存储器中的数据和存储于非易失性 NAND 存储器中的数据之间的数据一致性的装置可以基于硬件或者基于软件。最后，用于在非易失性 NAND 存储器中将第一地址总线上的地址映射到第二地址上的地址的装置也可以基于硬件或者基于软件。

在本发明的另一方面中，该存储器装置具有存储器控制器，该存储器控制器用于接收 NOR 地址信号的第一地址总线，用于接收 NOR 数据信号和数据协议命令的第一数据总线，和用于接收 NOR 控制信号的第一控制总线。该存储器控制器进一步具有用于接口连接易失性 RAM 存储器的第二地址总线，用于接口连接易失性 RAM 存储器的第二数据总线，以及用于接口连接易失性 RAM 存储器的第二控制总线。该控制器进一步具有用于接口连接非易失性 NAND 存储器的第三地址/数据总线，和用于接口连接非易失性 NAND 存储器的第三控制总线。该存储器装置进一步具有与所述第二地址总线，所述第二数据总线，以及所述第二控制总线相连接的 RAM 存储器。该存储器装置进一步具有与第三地址/数据总线和第三控制总线相连接的非易失性 NAND 存储器。该控制器进一步操作 RAM 存储器以模拟包含 NOR 协议命令的 NOR 存储器装置的操作。

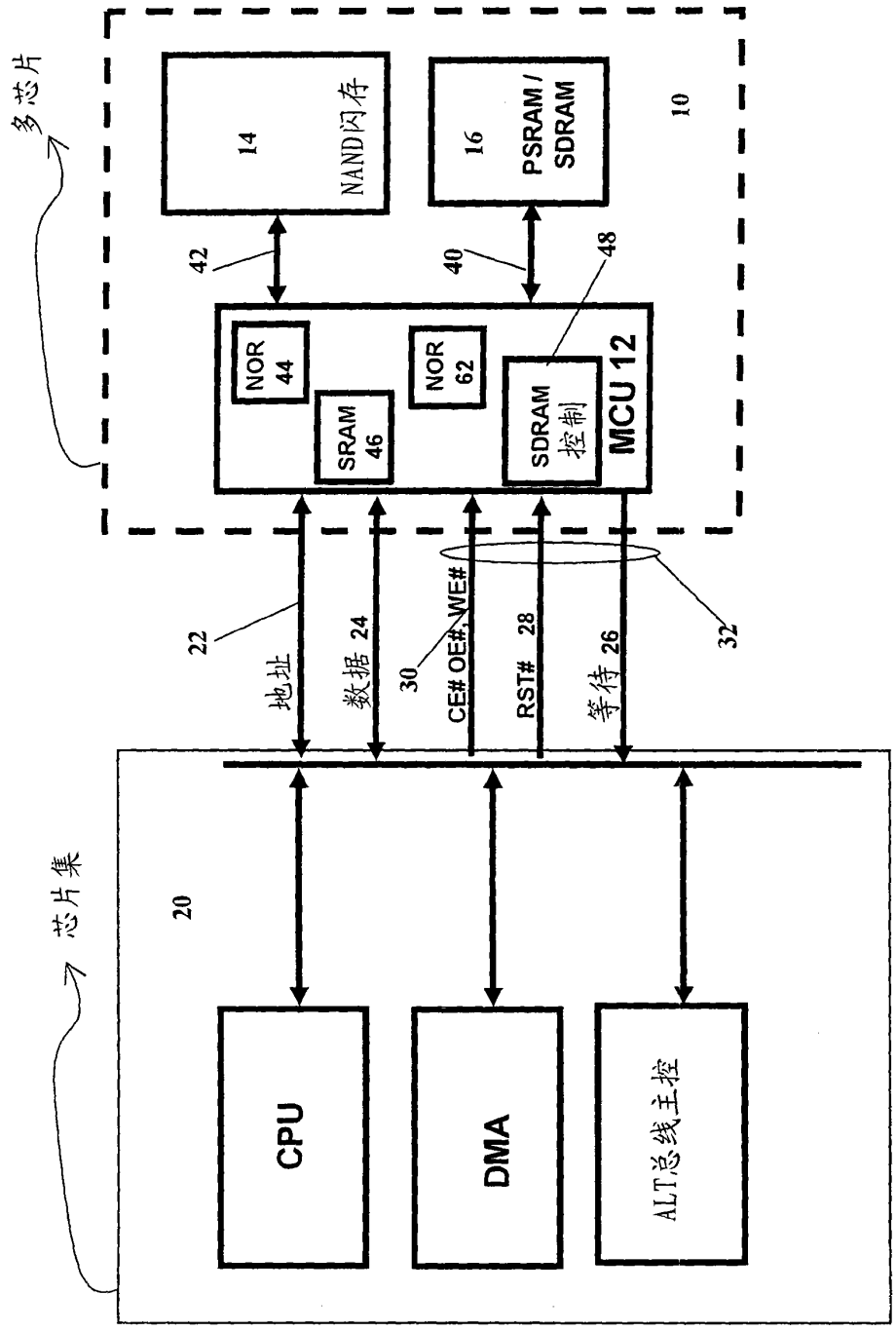


图 1

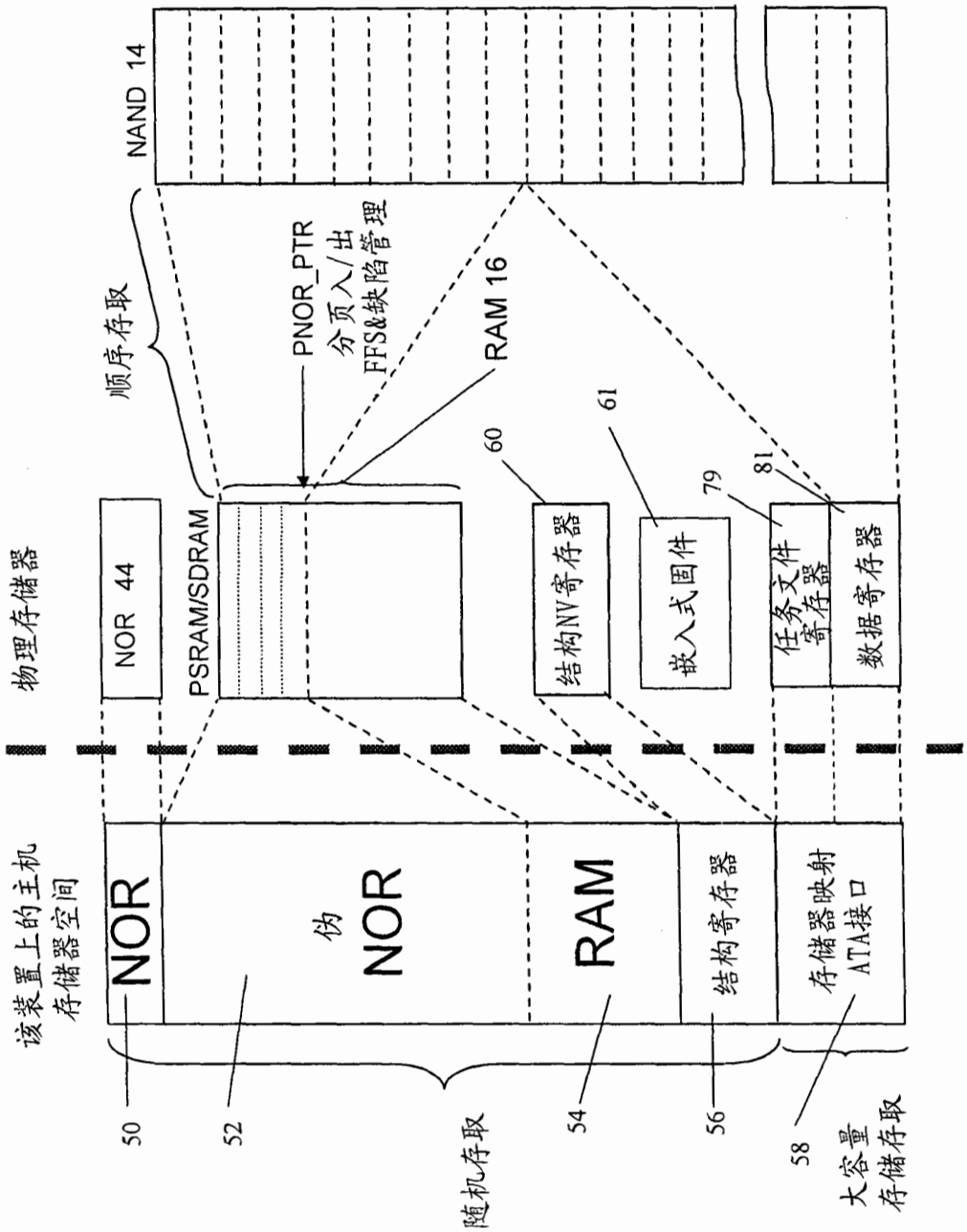


图 2

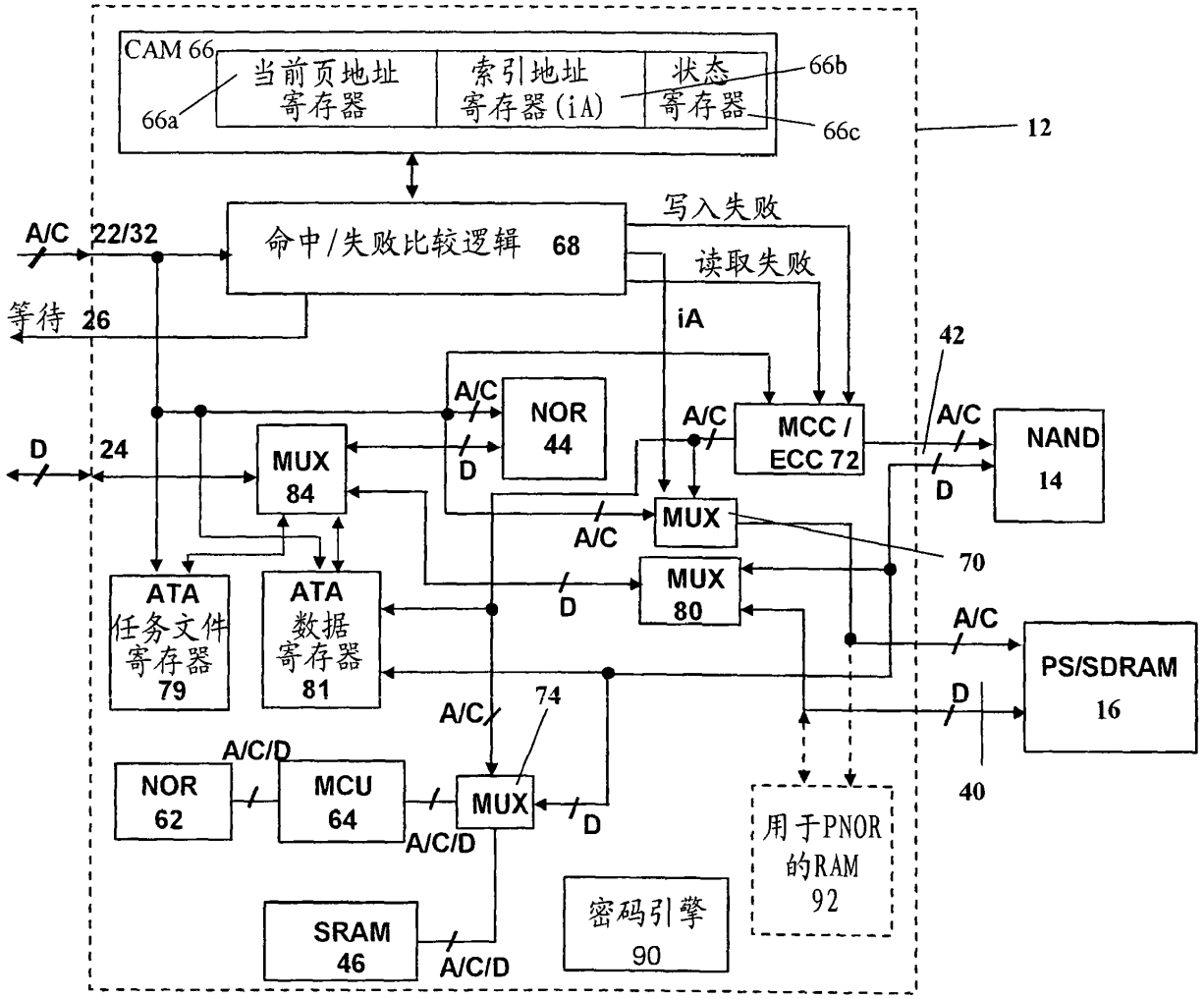


图 3

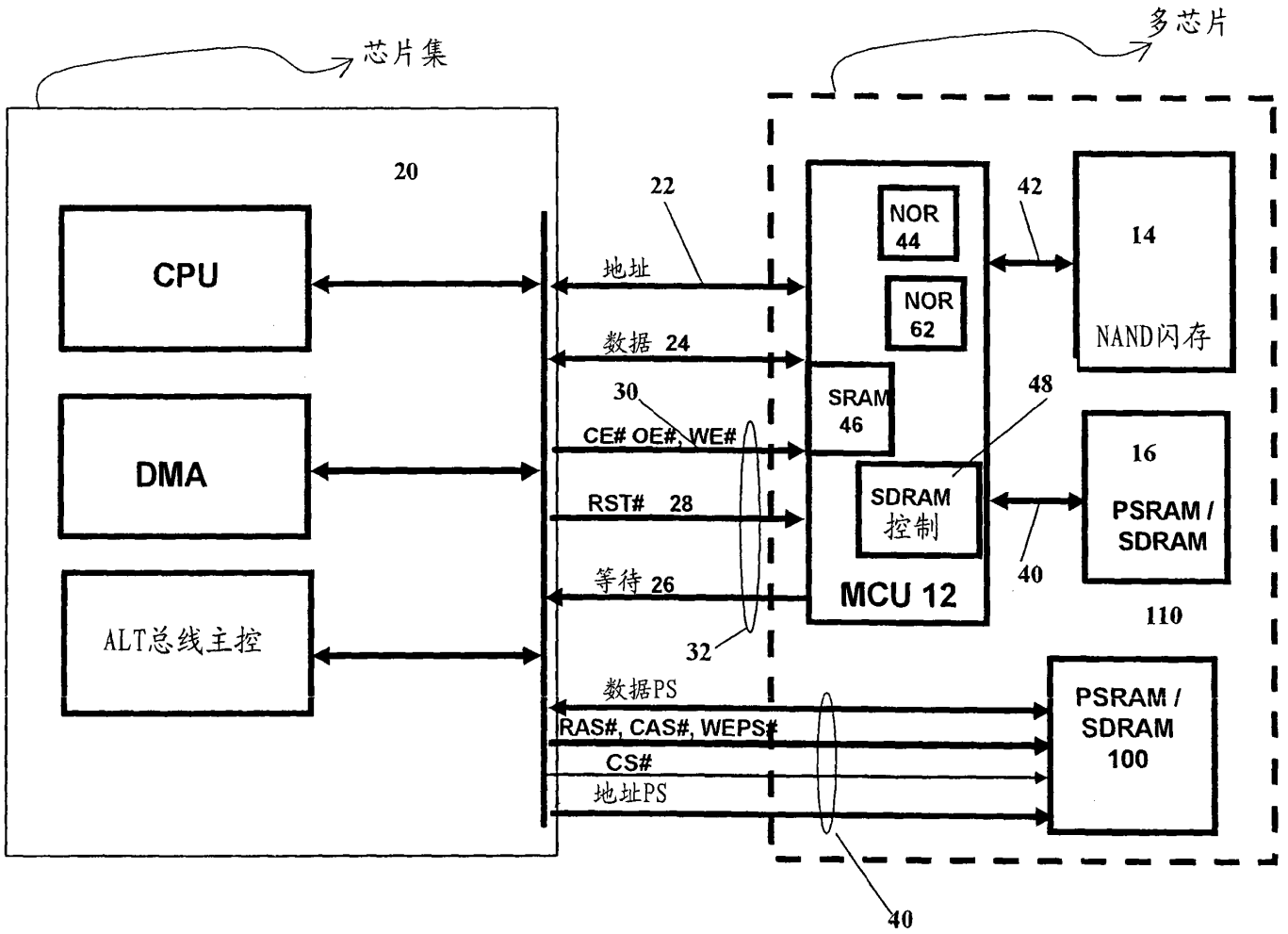


图 4

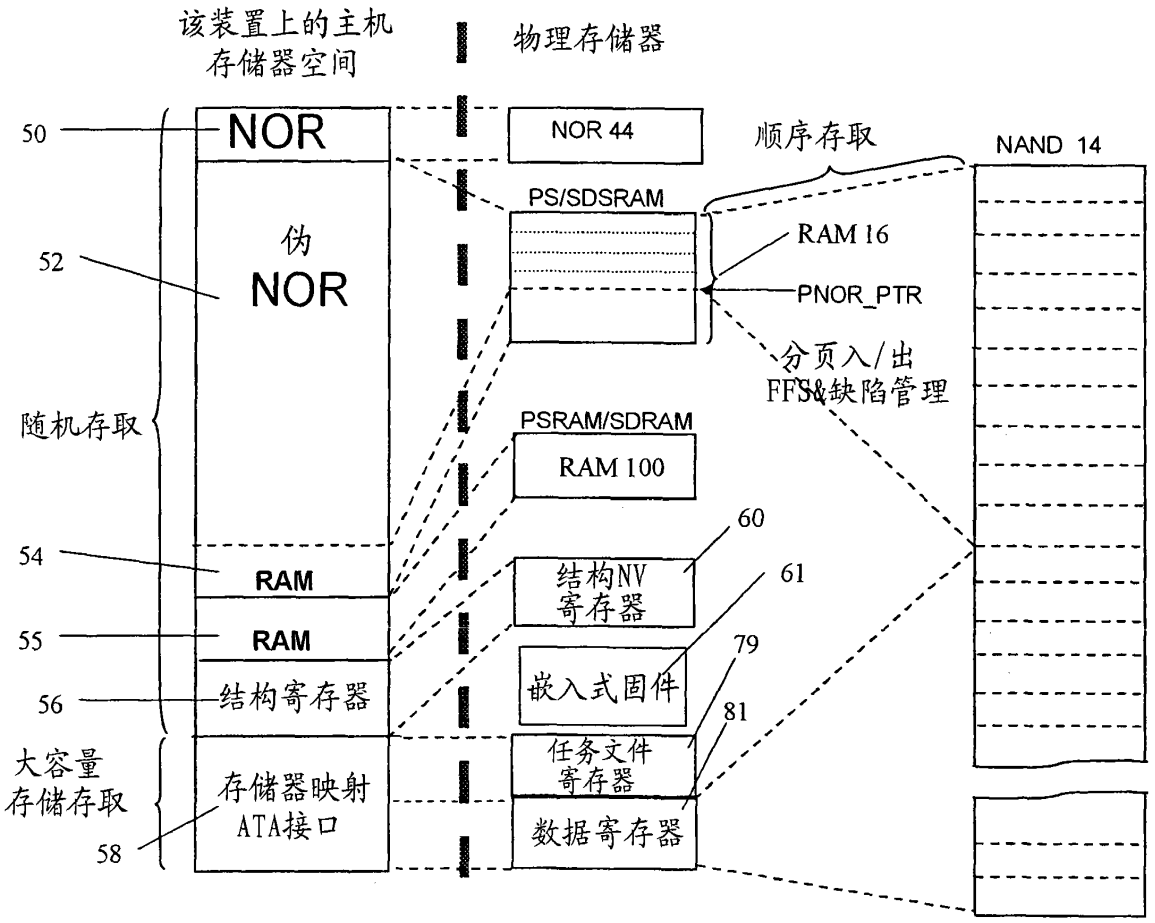


图 5

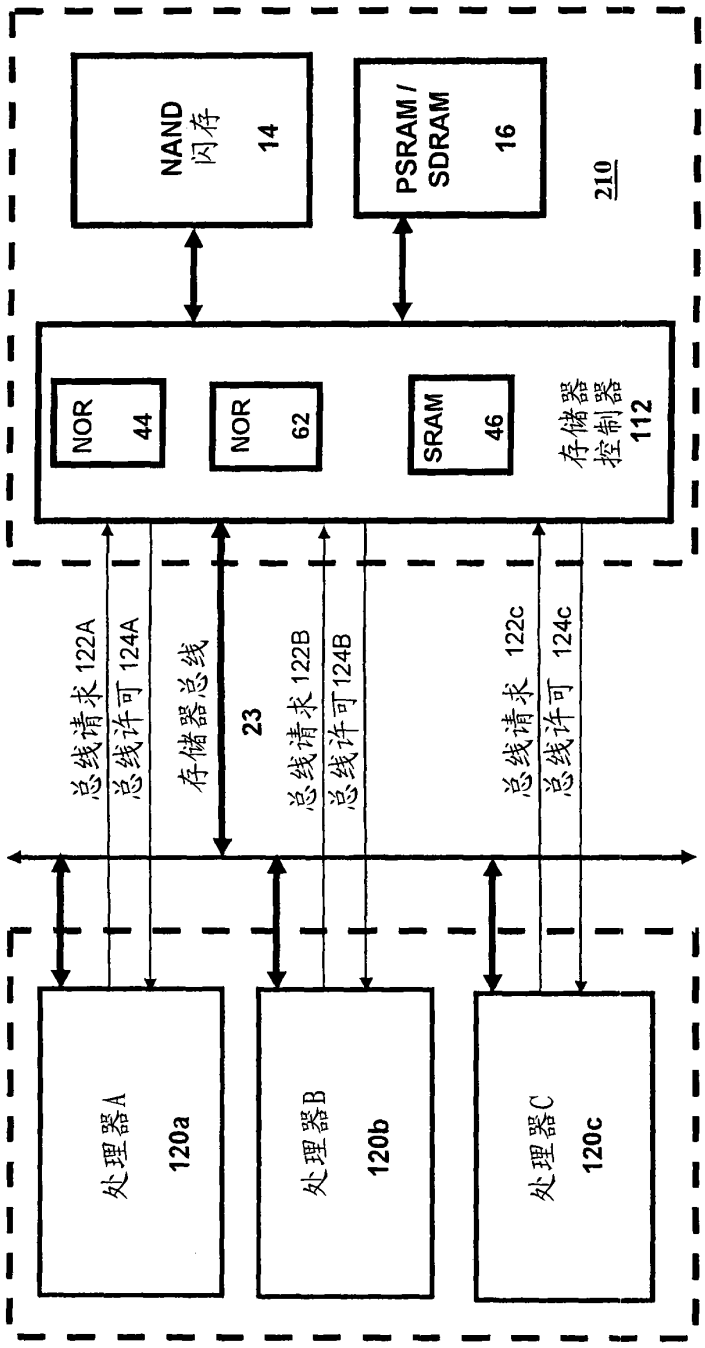


图 6

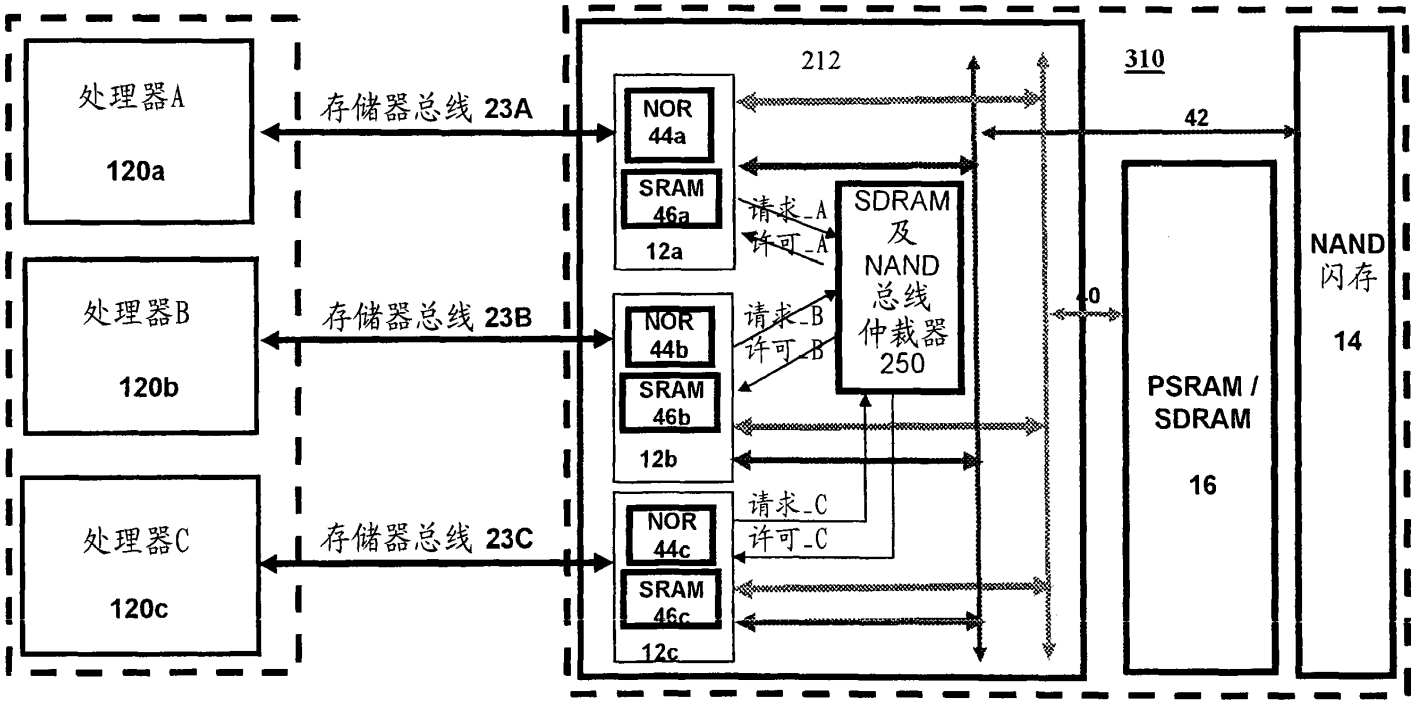


图 7

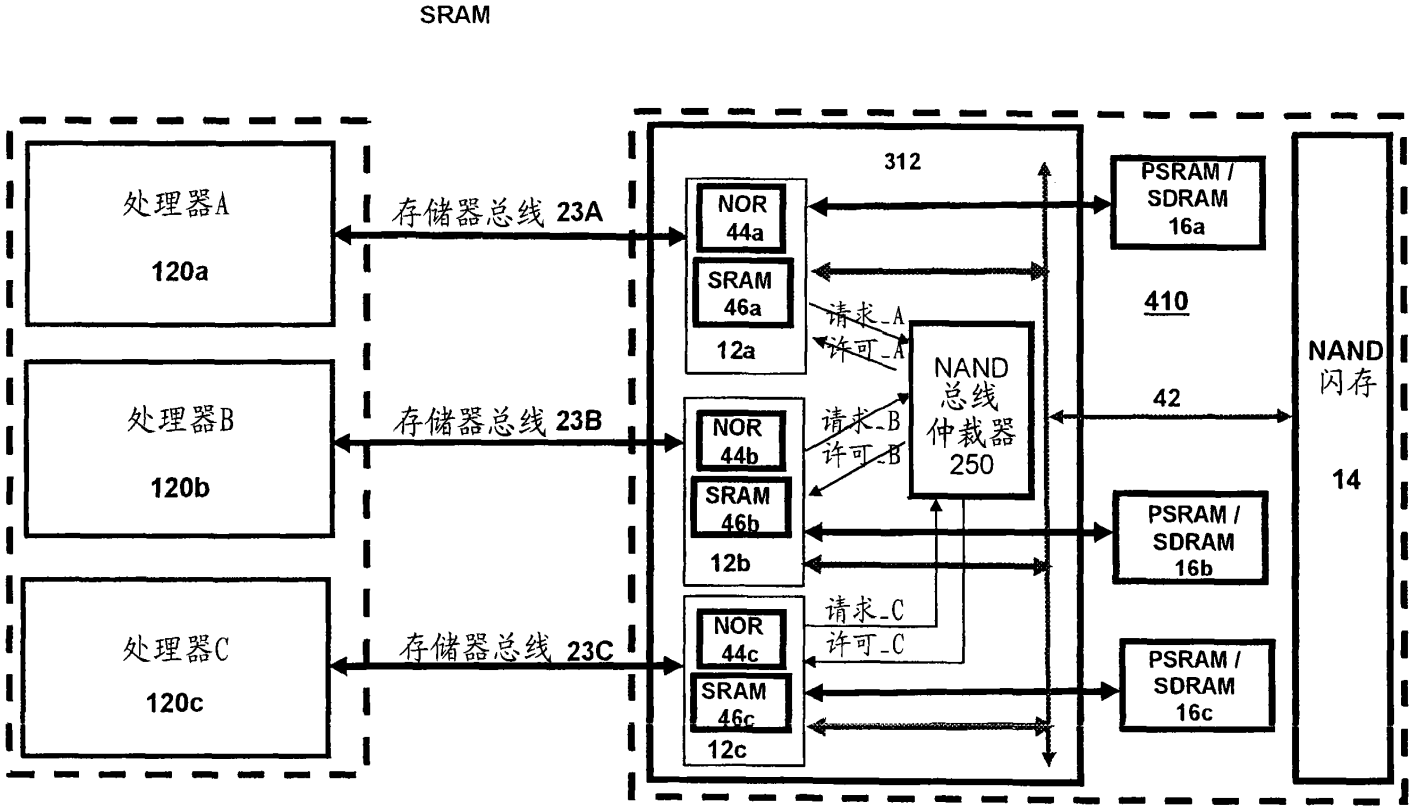


图 8

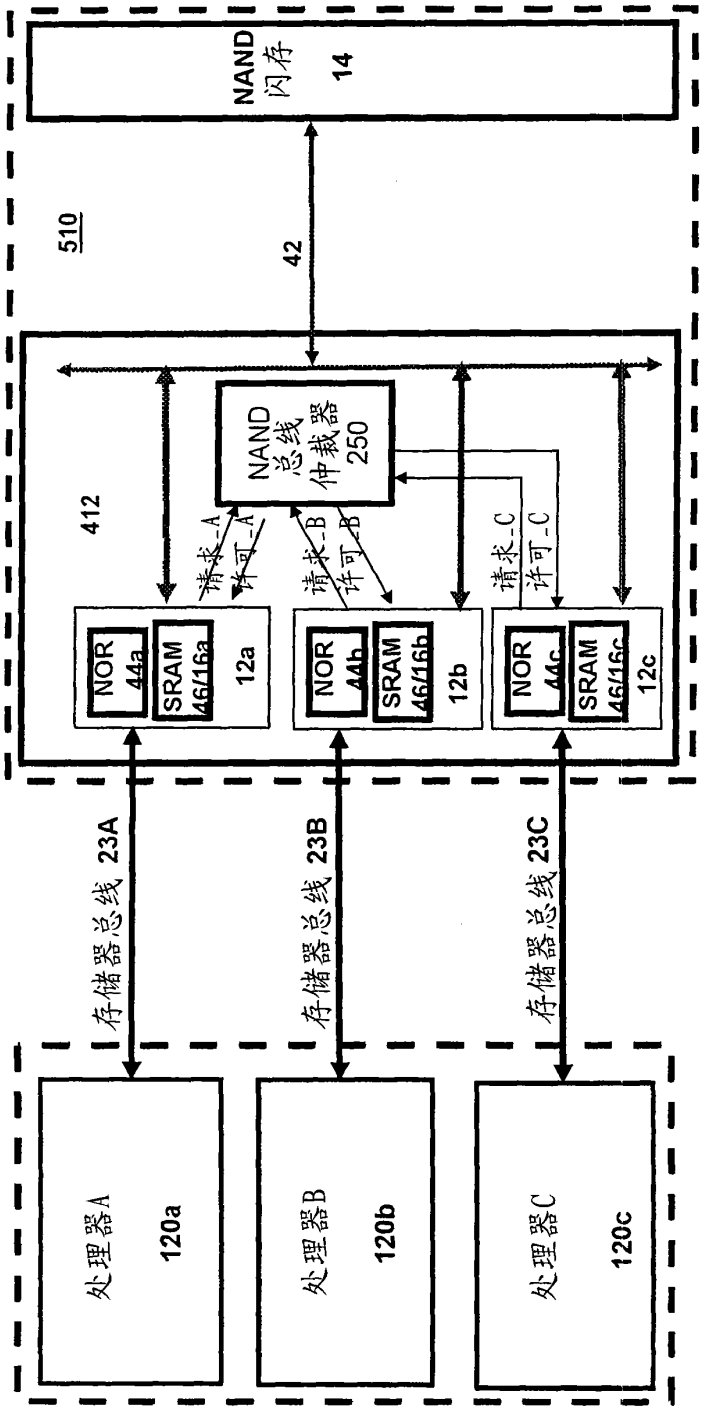


图 9

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Veröffentlichungsnummer:
(11) Publication number: **EP 2 737 383 A0**
(11) Numéro de publication:

Internationale Anmeldung veröffentlicht durch die Weltorganisation für geistiges Eigentum unter der Nummer:

WO 2013/016723 (Art. 153(3) EPÜ).

International application published by the World Intellectual Property Organization under number:

WO 2013/016723 (Art. 153(3) EPC).

Demande internationale publiée par l'Organisation Mondiale de la Propriété Intellectuelle sous le numéro:

WO 2013/016723 (art. 153(3) CBE).

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/934,416

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/934,416	03/23/2018	Hyun Lee	0016.001000G

CONFIRMATION NO. 2728

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

FORMALITIES LETTER

OC000000098882292

Date Mailed: 04/19/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/jmilani/

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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/934,416	03/23/2018	2139	0.00	0016.001000G	1	1

CONFIRMATION NO. 2728

FILING RECEIPT

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

Date Mailed: 04/19/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott H. Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 151145

Domestic Priority data as claimed by applicant

This application is a CON of 14/840,865 08/31/2015 PAT 9928186
which is a CON of 14/489,269 09/17/2014 PAT 9158684
which is a CON of 13/559,476 07/26/2012 PAT 8874831
which claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833
which is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/18/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/934,416**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

FLASH-DRAM HYBRID MEMORY MODULE

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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Electronic Patent Application Fee Transmittal

Application Number:	15934416
Filing Date:	23-Mar-2018
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Stephanie Semler
Attorney Docket Number:	0016.001000G

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 3 months with $0 paid	1253	1	1400	1400
Miscellaneous:				
		Total in USD ($)		**3280**

Electronic Acknowledgement Receipt	
EFS ID:	33768014
Application Number:	15934416
International Application Number:	
Confirmation Number:	2728
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000G
Receipt Date:	19-SEP-2018
Filing Date:	23-MAR-2018
Time Stamp:	15:11:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$3280
RAM confirmation Number	092018INTEFSW15162100
Deposit Account	602034
Authorized User	Michael Messinger
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	15934416-MPTA-Receive_Notice_to_File_Missing_Parts-20180419-09281473-5-1.pdf	1203 89bfbae28d27b83ebd0143dfa6f937fc1257b8e6	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	39068 3162b205718812756c575a227e2e64e10ed362ca	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	40271		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/934,416	03/23/2018	Hyun Lee	0016.001000G

CONFIRMATION NO. 2728

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

FORMALITIES LETTER

OC000000098882292

Date Mailed: 04/19/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/jmilani/

Electronic Acknowledgement Receipt

EFS ID:	33769753
Application Number:	15934416
International Application Number:	
Confirmation Number:	2728
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000G
Receipt Date:	19-SEP-2018
Filing Date:	23-MAR-2018
Time Stamp:	16:17:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	AA15934416-MPTA-Receive_Notice_to_File_Missing_Parts-20180419-09281473-5-1.pdf	301577 ab2d8c1ef5c712578624 11d4eb9d2d17d9983929	no	2

Warnings:

Information:	
Total Files Size (in bytes):	301577

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/934,416

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/934,416	03/23/2018	2139	1880	0016.001000G	1	1

CONFIRMATION NO. 2728

UPDATED FILING RECEIPT

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

OC000000102300740

Date Mailed: 09/24/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott H. Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 151145

Domestic Priority data as claimed by applicant

This application is a CON of 14/840,865 08/31/2015 PAT 9928186
which is a CON of 14/489,269 09/17/2014 PAT 9158684
which is a CON of 13/559,476 07/26/2012 PAT 8874831
which claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833
which is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/18/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/934,416**

Projected Publication Date: 01/03/2019

Non-Publication Request: No

Early Publication Request: No

Title

FLASH-DRAM HYBRID MEMORY MODULE

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc. CONFIRMATION NO.: 2728

SERIAL NO.: 15/934,416 ART UNIT: 2185

FILING DATE: 03-23-2018 EXAMINER: TBA

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Notice of Prior and Concurrent Proceedings

Applicant hereby calls to the attention of the Patent and Trademark Office the following *inter partes* review proceedings involving patents that are commonly-assigned with the patent in the above-identified patent application:

Proceeding	Status
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00365 (P.T.A.B.), filed December 27, 2017	Institution Granted 8/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00364 (P.T.A.B.), filed December 27, 2018	Institution Granted 8/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00363 (P.T.A.B.), filed December 22, 2017	Institution Granted 6/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00362 (P.T.A.B.), filed December 22, 2017	Institution Granted 6/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00303 (P.T.A.B.), filed December 14, 2018	Institution Granted 5/24/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00730 (P.T.A.B.), filed January 20, 2017	Terminated 5/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00692 (P.T.A.B.), filed January 17, 2017	Terminated 7/5/2018

Proceeding	Status
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00668 (P.T.A.B.), filed January 13, 2017	Terminated 7/18/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00667 (P.T.A.B.), filed January 13, 2017	Terminated 7/5/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00649 (P.T.A.B.), filed January 13, 2017	Terminated 5/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00587 (P.T.A.B.), filed January 6, 2017	Terminated 7/20/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00577 (P.T.A.B.), filed January 5, 2017	Terminated 7/5/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00560 (P.T.A.B.), filed January 3, 2017	Terminated 6/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00562 (P.T.A.B.), filed January 17, 2017	Terminated 9/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00561 (P.T.A.B.), filed January 17, 2017	Terminated 9/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00548 (P.T.A.B.), filed January 17, 2017	Terminated 5/3/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00549 (P.T.A.B.), filed January 17, 2017	Terminated 5/3/2018

Information Disclosure Statement

Listed on accompanying IDS Forms PTO/SB/08a equivalent and/or PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

Copies of documents **NPL6 – NPL37** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of U.S. patents and patent application publications are submitted.

It is expected that the examiner will review the prosecution and cited art in the parent application no(s). 14/840,865, filed 08-31-215 (now U.S. Pat. No. 9,928,186); 14/489,269, filed 09-17-2014 (now U.S. Pat. No. 9,158,685); 13/559,476, filed 07-26-2012 (now U.S. Pat. No. 8,874,831); 12/240,916, filed 09-29-2008 (now U.S. Pat. No. 8,301,833); and 12/131,873, filed 06-02-2008 (now abandoned) in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from co-pending U.S. Patent Application No(s). 14/214,652, filed March 24, 2014 as documents **NPL1 – NPL5**.

The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 60-2034.

Respectfully submitted,

SHAMI MESSINGER PLLC

Dated: October 17, 2018

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
Tel: 202-516-6900

Equivalent of Form PTO/SB/08a (07-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	2185
				Examiner Name	To be assigned
Sheet	1	of	1	Attorney Docket Number	0016.001000G

U.S. PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Document Number Number-Kind Code [2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	2012/0110417 A1	05-03-2012	D'Abreu	
	US2	2010/0122200 A1	05-13-2010	Merry, Jr.	
	US3	2009/0235038 A1	09-17-2009	Sartore	
	US4	6839774 B1	01-04-2005	Ahn et al.	
	US5	2003/0206478 A1	11-06-2003	Ayukawa et al.	
	US6	2005/0204091 A1	03-20-2005	Kilbuck et al.	
	US7	9,921,762 B2	03-20-2018	Amidi et al.	
	US8	9,928,186 B2	03-27-2018	Lee et al.	
	US9	6,363,450 B1	03-26-2002	Lash et al.	

FOREIGN PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	2185
				Examiner Name	To be assigned
Sheet	1	of	4	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	NPL1	Copy of Non-Final Office Action for U.S. Appl. No. 14/214,652, mailed March 8, 2018; 41 pages.	
	NPL2	Copy of Examiner Search Notes for U.S. Appl. No. 14/214,652, mailed March 8, 2018; 3 pages.	
	NPL3	Copy of Examiner Notice of References Cited for U.S. Appl. No. 14/214,652, mailed March 8, 2018; 1 page.	
	NPL4	Extended European search report issuing from European Patent Application 17191878.2, August 2, 2018, 9 pgs.	
	NPL5	Copy of Final Office Action for U.S. Appl. No. 15/000,834, mailed May 3, 2018;16 pages.	
	NPL6	Patent Owner's Preliminary Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00365 (P.T.A.B.), filed May 7, 2018; 47 pages.	
	NPL7	Patent Owner's Preliminary Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00364 (P.T.A.B.), filed May 7, 2018; 47 pages.	
	NPL8	Patent Owner's Preliminary Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00363 (P.T.A.B.), filed May 7, 2018; 42 pages.	
	NPL9	Patent Owner's Preliminary Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00362 (P.T.A.B.), filed May 7, 2018; 41 pages.	
	NPL10	Patent Owner's Supplemental Mandatory Notices, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed September 17, 2018; 3 pages.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	2185
				Examiner Name	To be assigned
Sheet	2	of	4	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL11	Patent Owner's Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed August 10, 2018; 65 pages.	
	NPL12	Patent Owner's Preliminary Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed March 19, 2018; 59 pages.	
	NPL13	Netlist Inc.'s Notice of Appeal to the U.S. Court of Appeals for the Federal Circuit and Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00562 (P.T.A.B.), filed September 6, 2018; 56 pages.	
	NPL14	Netlist Inc.'s Notice of Appeal to the U.S. Court of Appeals for the Federal Circuit and Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00561 (P.T.A.B.), filed September 6, 2018; 67 pages.	
	NPL15	Netlist Inc.'s Notice of Appeal to the U.S. Court of Appeals for the Federal Circuit and Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00560 (P.T.A.B.), filed June 29, 2018; 22 pages.	
	NPL16	Patent Owner's Supplemental Mandatory Notices, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00549 (P.T.A.B.), filed April 19, 2018; 4 pages.	
	NPL17	Patent Owner's Supplemental Mandatory Notices, filed in *Sandisk Corp. v. Netlist, Inc.,* Case No. IPR2015-01020 (P.T.A.B.), filed April 19, 2018; 3 pages.	
	NPL18	Netlist Inc.'s Notice of Appeal and Decision on Remand, filed in *Diablo Technologies, Inc. v. Netlist, Inc.,* Case No. IPR2014-01011 (P.T.A.B.), filed May 30, 2018; 33 pages.	
	NPL19	Netlist Inc.'s Notice of Appeal and Decision on Remand, filed in *Diablo Technologies, Inc. v. Netlist, Inc.,* Case No. IPR2014-00883 (P.T.A.B.), filed May 30, 2018; 28 pages.	
	NPL20	Netlist Inc.'s Notice of Appeal and Decision on Remand, filed in *Diablo Technologies, Inc. v. Netlist, Inc.,* Case No. IPR2014-00882 (P.T.A.B.), filed May 30, 2018; 28 pages.	

Examiner Signature		Date Considered	

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	2185
				Examiner Name	To be assigned
Sheet	3	of	4	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL21	Supplemental Declaration of Robert J. Murphy, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed August 10, 2018; 76 pages.	
	NPL22	Deposition of Donald Alpert, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed July 20, 2018; 218 pages.	
	NPL23	Joint List of Claim Terms For Construction and Proposed Constructions, filed as Exhibit 2007 in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed August 10, 2018; 23 pages.	
	NPL24	Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00362 and IPR2018-00363 (P.T.A.B.), entered June 29, 2018; 33 pages.	
	NPL25	"The Authoritative Dictionary of IEEE Standards Terms," 7th Ed. 2000, pp. 1 - 10.	
	NPL26	"The Authoritative Dictionary of IEEE Standards Terms," 6th Ed. 2000, pp. 1 - 8.	
	NPL27	"Orbit Micro News and Notes," available at http://www.orbitmicro.com/company/blog/87; 10 pages.	
	NPL28	Jacob, B. et al, "Memory Systems: Cache, DRAM, Disk, Chapter 30" New York, NY: Morgan Kaufmann Press, 2008; 40 pages.	
	NPL29	Declaration of Robert J. Murphy, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed March 19, 2001; 71 pages.	
	NPL30	Decision Instituting *Inter Partes* Review of U.S. Patent No. 9,535,623, Entered May 24, 2018, 18 pages.	

Examiner Signature		Date Considered	

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	2185
				Examiner Name	To be assigned
Sheet	4	of	4	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL31	Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00587 (P.T.A.B.), entered June 20, 2018; 53 pages.	
	NPL32	Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00692 (P.T.A.B.), entered July 5, 2018; 44 pages.	
	NPL33	Patent Owner's Motion to Strike, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00562 (P.T.A.B.), entered March 28, 2018; 8 pages.	
	NPL34	Petitioner's Opposition to Patent Owner's Motion to Strike, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00562 (P.T.A.B.), entered April 4, 28, 2018; 8 pages.	
	NPL35	Record of Oral Hearing, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00562 (P.T.A.B.), held April 6, 28, 2018; 68 pages.	
	NPL36	Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2017-00548 (P.T.A.B.), entered May 3, 2018; 18 pages.	
	NPL37	Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2017-00549 (P.T.A.B.), entered May 3, 2018; 16 pages.	
	NPL38		
	NPL39		
	NPL40		

Examiner Signature		Date Considered	

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Electronic Acknowledgement Receipt

EFS ID:	34035833
Application Number:	15934416
International Application Number:	
Confirmation Number:	2728
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000G
Receipt Date:	17-OCT-2018
Filing Date:	23-MAR-2018
Time Stamp:	14:53:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	NPL6.pdf	1388925 6a766d1df81ee589da04ed5a0131994b3a43699a	no	47

Warnings:

Information:					
2	Non Patent Literature	NPL7.pdf	1534321 aea004409fbd995ce46a016262f3f72e42cd43a9	no	47
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6	Non Patent Literature	NPL11.pdf	1673733 15c364a60a335f25cedbcdca6fa5ddd40030be5e	no	65
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11	Non Patent Literature	NPL17.pdf	95373 89ea41cfae821ebdde0a92f712bbd7e325f69d52	no	4
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13	Non Patent Literature	NPL18.pdf	387379 62281a35ab423dabc3108313f0d360e42c68a9bb	no	33
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33	Information Disclosure Statement (IDS) Form (SB08)	0016001000G1SIDSSB08.pdf	296652 f80a2e49380ea7a8f341e53ee8f4def633100d67	no	9
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Information:					
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34	Non Patent Literature	NPL1.pdf	1837451 9faa3921d7f29ae67a9e06a9c3753f11e88e229c	no	41
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Information:					
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Information:					

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38	Non Patent Literature	NPL5.pdf	1275344 7f4dd89ab0f8593a6518a934e709ceccc25b0ac5	no	16
Warnings:					
Information:					
			Total Files Size (in bytes):	44917685	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	2185
				Examiner Name	To be assigned
Sheet	1	of	1	Attorney Docket Number	0016.001000G

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	NPL1	Copy of Notice of Submission of Opinion, South Korea Patent Office with English Translation, 6 pages	X
	NPL2	Cop of Notice of Final Rejection, South Korea Patent Office with English Translation, 4 pages.	X
	NPL3		
	NPL4		
	NPL5		
	NPL6		
	NPL7		
	NPL8		
	NPL9		
	NPL10		

Examiner Signature		Date Considered	

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc. CONFIRMATION NO.: 2728

SERIAL NO.: 15/934,416 ART UNIT: 2185

FILING DATE: 03-23-2018 EXAMINER: TBA

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Notice of Prior and Concurrent Proceedings

Applicant hereby calls to the attention of the Patent and Trademark Office the following *inter partes* review proceedings involving patents that are commonly-assigned with the patent in the above-identified patent application:

Proceeding	Status
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00365 (P.T.A.B.), filed December 27, 2017	Institution Granted 8/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00364 (P.T.A.B.), filed December 27, 2018	Institution Granted 8/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00363 (P.T.A.B.), filed December 22, 2017	Institution Granted 6/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00362 (P.T.A.B.), filed December 22, 2017	Institution Granted 6/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00303 (P.T.A.B.), filed December 14, 2018	Institution Granted 5/24/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00730 (P.T.A.B.), filed January 20, 2017	Terminated 5/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00692 (P.T.A.B.), filed January 17, 2017	Terminated 7/5/2018

Proceeding	Status
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00668 (P.T.A.B.), filed January 13, 2017	Terminated 7/18/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00667 (P.T.A.B.), filed January 13, 2017	Terminated 7/5/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00649 (P.T.A.B.), filed January 13, 2017	Terminated 5/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00587 (P.T.A.B.), filed January 6, 2017	Terminated 7/20/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00577 (P.T.A.B.), filed January 5, 2017	Terminated 7/5/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00560 (P.T.A.B.), filed January 3, 2017	Terminated 6/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00562 (P.T.A.B.), filed January 17, 2017	Terminated 9/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00561 (P.T.A.B.), filed January 17, 2017	Terminated 9/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00548 (P.T.A.B.), filed January 17, 2017	Terminated 5/3/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00549 (P.T.A.B.), filed January 17, 2017	Terminated 5/3/2018

Information Disclosure Statement

Listed on accompanying IDS Forms PTO/SB/08a equivalent and/or PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

Copies of documents **NPL1** and **NPL2** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of U.S. patents and patent application publications are submitted.

It is expected that the examiner will review the prosecution and cited art in the parent application no(s). 14/840,865, filed 08-31-215 (now U.S. Pat. No. 9,928,186); 14/489,269, filed 09-17-2014 (now U.S. Pat. No. 9,158,685); 13/559,476, filed 07-26-2012 (now U.S. Pat. No. 8,874,831); 12/240,916, filed 09-29-2008 (now U.S. Pat. No. 8,301,833); and 12/131,873, filed 06-02-2008 (now abandoned) in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 60-2034.

Respectfully submitted,

SHAMI MESSINGER PLLC

Dated: December 17, 2018

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
Tel: 202-516-6900

Electronic Acknowledgement Receipt

EFS ID:	34603030
Application Number:	15934416
International Application Number:	
Confirmation Number:	2728
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000G
Receipt Date:	17-DEC-2018
Filing Date:	23-MAR-2018
Time Stamp:	14:06:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	0016001000G2SIDSSB08b.pdf	82678 013da25201a045f10cf1f8e44d9b353852ea6543	no	1

Warnings:

Information:					
This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	NPL1_KRNon-FinalRejection_wGoogleTranslateA.pdf	353328 f9e8be3c36df300baabe83943f49268134a68460	no	6
Warnings:					
Information:					
3	Non Patent Literature	NPL2_KRFinalRejection_wGoogleTranslateA.pdf	108661 12399115f224eb1b0127a488d72017577ea9a374	no	4
Warnings:					
Information:					
4	Transmittal Letter	0016001000G2SIDSPleading.pdf	130690 9018da89c67e23b5cc51c6a55ffcc2cf60138dab	no	4
Warnings:					
Information:					
		Total Files Size (in bytes):	675357		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/934,416	03/23/2018	Hyun Lee	0016.001000G

CONFIRMATION NO. 2728

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

PUBLICATION NOTICE

OC000000104849851

Title:FLASH-DRAM HYBRID MEMORY MODULE

Publication No.US-2019-0004985-A1
Publication Date:01/03/2019

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/934,416	03/23/2018	Hyun Lee	0016.001000G	2728

151145 7590 03/21/2019

Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2131	

NOTIFICATION DATE	DELIVERY MODE
03/21/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

khaled@shamimessinger.com
mike@shamimessinger.com
stephanie@shamimessinger.com

Office Action Summary	**Application No.** 15/934,416	**Applicant(s)** Lee et al.	
	Examiner HASHEM FARROKH	**Art Unit** 2131	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 03/23/2018.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 03/23/2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 3/23/18,10/17/18,12/17/18.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

The instant application having application No. 15/934,416 has a total of 1 claims pending in the application; there are 1 independent claim and no dependent claims, all of which are ready for examination by the examiner.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b),** no separate citation of the same prior art need be made by the applicants in the instant application.*

INFORMATION CONCERNING IDS:

The information disclosure statements (IDS') submitted on 03/23/2018, 10/17/2018, and 12/17/2018 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the examiner. However, the documents marked by lined-through have not been considered

by the Examiner because the copies and/or English translation copies of foreign documents listed have not been provided.

INFORMATION CONCERNING CLAIMS:

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process... may obtain a patent therefor..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See Miller v. Eagle Mfg. Co., *151 U.S. 186 (1894);* In re Vogel, *422 F.2d 438, 164 USPQ 619 (CCPA 1970);* In re Ockert, *245 F.2d 467, 114 USPQ 330 (CCPA 1957).*

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the claims that are directed to the same invention so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claim 1 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of prior U.S. Patent No. 9,928,186. This is a statutory double patenting rejection.

1. Claim 1 of instant application (US Application No. 15/934,416) is compared to claim 1 of US Patent No. 9,928,186 in the following table:

Patent No. 9,928,186	***Application No. 15/934,416***
Claim 1:	***Claim 1:***

A memory module comprising: a data manager configured to be coupled to a memory controller of a host system using a data bus, the data manager is operable to communicate data signals with the memory controller of the host system by way of the data bus in accordance with a first protocol; a first volatile memory subsystem coupled to the data manager using a first data bus, the first volatile memory subsystem is operable to communicate data signals with the data manager by way of the first data bus in accordance with the first protocol; a second volatile memory subsystem coupled to the data manager using a second data bus, the second volatile memory subsystem is operable to communicate data signals with the data manager by way of the second data bus in accordance with the first protocol;	A memory module comprising: a data manager configured to be coupled to a memory controller of a host system using a data bus, the data manager is operable to communicate data signals with the memory controller of the host system by way of the data bus in accordance with a first protocol; a first volatile memory subsystem coupled to the data manager using a first data bus, the first volatile memory subsystem is operable to communicate data signals with the data manager by way of the first data bus in accordance with the first protocol; a second volatile memory subsystem coupled to the data manager using a second data bus, the second volatile memory subsystem is operable to communicate data signals with the data manager by way of the second data bus in accordance with the first protocol;

a non-volatile memory subsystem coupled to the data manager using a third data bus, the non-volatile memory subsystem is operable to communicate data signals with the data manager by way of the third data bus using a second protocol; and a controller operable to receive one or more commands from the memory controller of the host system in accordance with the first protocol, and in response to the one or more commands received from the memory controller of the host system, the controller generates and transmits one or more control signals to the data manager, wherein, in response to the one or more control signals, the data manager transfers data between the first volatile memory subsystem and the memory controller of the host **system**, and transfers data signals from the non-volatile memory	a non-volatile memory subsystem coupled to the data manager using a third data bus, the non-volatile memory subsystem is operable to communicate data signals with the data manager by way of the third data bus using a second protocol; and a controller operable to receive one or more commands from the memory controller of the host system in accordance with the first protocol, and in response to the one or more commands received from the memory controller of the host system, the controller generates and transmits one or more control signals to the data manager, wherein, in response to the one or more control signals, the data manager transfers data between the first volatile memory subsystem and the memory controller of the host **system 1** and transfers data signals from the non-volatile memory

subsystem to the second volatile memory subsystem by way of the third data bus and the second data bus.	subsystem to the second volatile memory subsystem by way of the third data bus and the second data bus.

Examiner's notes, as highlighted in the table above, numbering the host system as Host system 1 does not make the invention different.

Conclusion

The prior art made of record and not relied upon are as follows:

1. *Cope et al. (US 20080189479 A1).*
2. *Susaki (US 20030137881 A1).*
3. *Ware et al. (US 8214616 B2).*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ann Lo can be reached on (571)272-9767. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/

Primary Examiner, Art Unit 2131

Sunday, March 17, 2019

Notice of References Cited	Application/Control No. 15/934,416	Applicant(s)/Patent Under Reexamination Lee et al.	
	Examiner HASHEM FARROKH	Art Unit 2131	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20080189479-A1	08-2008	Cope; Bryan	G06F12/0607	711/104
*	B	US-20030137881-A1	07-2003	Sasaki, Gen	G06F13/1684	365/189.09
*	C	US-8214616-B2	07-2012	Ware; Frederick A.	G06F13/1684	711/167
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/934,416	Lee et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant			☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		**DATE**								
Final	Original	03/17/2019								
	1	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/934,416	Lee et al.
	Examiner	Art Unit
	HASHEM FARROKH	2131

CPC - Searched*		
Symbol	Date	Examiner
G06F13/1694; G06F12/0246; G06F13/28; G06F13/4243; G06F2212/7208; G06F3/0685; G06F12/0638; G06F13/4027; G06F1/185; G06F2212/205; G06F3/0613; G06F3/0659; G11C7/1072; G11C14/0018	03/17/2019	HF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	110	03/17/2019	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PALM and Inventor Search	03/16/2019	HF
EAST Text Search	03/16/2019	HF
Google Search	03/17/2019	HF

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	~~2185~~ 2131
				Examiner Name	~~To be assigned~~ H. Farrokh
Sheet	1	of	1	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	NPL1	Copy of Notice of Submission of Opinion, South Korea Patent Office with English Translation, 6 pages	X
	NPL2	Cop of Notice of Final Rejection, South Korea Patent Office with English Translation, 4 pages.	X
	NPL3		
	NPL4		
	NPL5		
	NPL6		
	NPL7		
	NPL8		
	NPL9		
	NPL10		

Examiner Signature	/HASHEM FARROKH/	Date Considered	03/16/2019

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.
CONFIRMATION NO.: To be assigned
SERIAL NO.: Filed herewith
ART UNIT: ~~To be assigned~~
FILING DATE: 03-23-2018
EXAMINER: ~~To be assigned~~ H. Farrokh
TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Information Disclosure Statement

Commissioner:

Listed on accompanying IDS Forms PTO/SB/08a equivalent and PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

All References Considered Except Where Lined Through. /H.F/

Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA),. No statement or fee is required.

Copies of documents **FP1-FP4** are submitted herewith. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of U.S. patents and patent application publications cited as documents **US1-US141** on the attached IDS Forms are submitted.

A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

Document **US139** (9,361,250 B2) is submitted herewith as an English-language counterpart to document **FP2** (CN 102110057 A).

Document **US119** (7,519,754 B2) is submitted herewith as an English-language counterpart to document **FP3** (CN 101017460 A).

Copies of the **NPL1-NPL72** documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. 14/840,865, filed 08-31-2015 (now pending), which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

It is expected that the examiner will review the prosecution and cited art in the parent application no(s). 14/840,865, filed 08-31-215 (now pending); 14/489,269, filed 09-17-2014 (now U.S. Pat. No. 9,158,685); 13/559,476, filed 07-26-2012 (now now U.S. Pat. No. 8,874,831); 12/240,916, filed 09-29-2008 (now now U.S. Pat. No. 8,301,833); and 12/131,873, filed 06-02-2008 (now abandoned) in accordance with MPEP 2001.06(b), and indicate in the next communication

All References Considered Except Where Lined Through. /H.F/

from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending, commonly assigned U.S. Patent Applications as documents **NPL36-NPL43** and **NPL45-NPL56**.

The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

Respectfully submitted,

SHAMI MESSINGER PLLC

Dated: 03-23-2018

/ Khaled Shami /
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
Tel: 202-516-6902

All References Considered Except Where Lined Through. /H.F/

Equivalent of Form PTO/SB/08a (07-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	~~Filed herewith~~ 15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	~~To be assigned~~ 2131
				Examiner Name	To be assigned H. Farrokh
Sheet	1	of	8	Attorney Docket Number	0016.001000G

U.S. PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Document Number: Number-Kind Code [2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	2002/0053944 A1	05-09-2002	Brass et al.	
	US2	2002/0083368 A1	06-27-2002	Abe et al.	
	US3	2002/0199061 A1	12-26-2002	Friedman et al.	
	US4	2003/0028733 A1	02-06-2003	Tsunoda et al.	
	US5	2003/0158995 A1	08-21-2003	Lee et al.	
	US6	2004/0088508 A1	05-06-2004	Ballard et al.	
	US7	2004/0163027 A1	08-19-2004	Maclaren et al.	
	US8	2004/0190210 A1	09-30-2004	Leete	
	US9	2005/0044302 A1	02-24-2005	Pauley et al.	
	US10	2005/0060488 A1	03-17-2005	Poechmueller	
	US11	2005/0132250 A1	06-16-2005	Hansen et al.	
	US12	2005/0141273 A1	06-30-2005	Park et al.	
	US13	2005/0249011 A1	11-10-2005	Maeda	
	US14	2005/0273548 A1	12-08-2005	Roohparvar	
	US15	2006/0039197 A1	02-23-2006	Khouri et al.	
	US16	2006/0069896 A1	03-30-2006	Sanders	
	US17	2006/0080515 A1	04-13-2006	Spiers et al.	
	US18	2006/0212651 A1	09-21-2006	Ashmore	
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Sheet	2	of	8	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL11	ELMHURST et al., "A 1.8-V 128-Mb 125-MHz Multilevel Cell Flash Memory With Flexible Read While Write", IEEE Journal of Solid-State Circuits 38(11):1929-1933 (2003).	
	NPL12	Ex. 1004 - IPR2017-00587 Ron Maltiel CV, 7 pages.	
	NPL13	Extended European Search Report for European Application No. 12 817 751.6, mailed June 9, 2015	
	NPL14	File History for Application No. 12/240,916, filed September 29, 2008, 320 pages.	
	NPL15	File History for Application No. 13/905,048 filed May 29, 2013, 181 pages.	
	NPL16	File History for Provisional Application 60/941,586, filed June 1, 2007, 23 pages.	
	NPL17	File History US Patent No. 8,671,243	
	NPL18	Final Office Action, dated June 15, 2016, issued in U.S. Patent Application No. 14/489,281, 10 pages.	
	NPL19	Horowitz, P. et al., "The Art of Electronics", Cambridge Univesity Press 2nd Ed. 1989, pp. 471, 495-496.	
	NPL20	Innis, J., "MPC8560 PowerQUICC Ill Compact Flash Interface Design", Freescale Semiconductor, Inc., 2004-2006, pp. D 1-23.	

Examiner Signature	/HASHEM FARROKH/	Date Considered	03/16/2019

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

All References Considered Except Where Lined Through. /H.F/

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	Filed herewith
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	To be assigned
				Examiner Name	To be assigned
Sheet	3	of	8	Attorney Docket Number	0016.001000G

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	NPL21	Intel 1.8 Volt Intel StrataFlash Wireless Memory (L18).	
	NPL22	International Preliminary Report on Patentabillity in PCT/US12/48750, mailed April 3, 2014, pp.1-8.	
	NPL23	International Search Report and Written Opinion in PCT/US12/48750, dated October 10, 2012 pp.1-10.	
	NPL24	Jacob, B., "Memory Systems Cache, DRAM, Disk", Morgan Kaufman Publishers, Burlington, MA, 2008, Preface and Ch. 7 pp. 315-322.	
	NPL25	Jandhyala, S. et al., "Design-For-Test Analysis of a Buffered SDRAM DIMM", Semiconductor Group, Texas Instruments, Proceedings of International Workshop in Memory Technology, Design and Testing, Singapore, August 13014, 1996, 15 pages.	
	NPL26	JEDEC Standard 21-C, "Configurations for Solid State Memories," pp. 4.5.5-1 to 4.5.5-18.	
	NPL27	JEDEC Standard, "Configurations for Solid State Memories", JEDEC Standard 21-C, Release 9, August 1999, 114 pages.	
	NPL28	JEDEC STANDARD, DDR2 SDRAM Specification, JESD79-2B (Revision of JESD79-2A) January 2005, 113 pages.	
	NPL29	JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79, June 2000, 77 pages.	
	NPL30	JEDEC Standard, Double Data Rate (DDR): SDRAM Specification: JESD79C (Revision JESD79B), March 2003, pp.1-75.	

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				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	To be assigned
				Examiner Name	To be assigned
Sheet	4	of	8	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL31	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification:JESD205, JEDEC SOLID STATE TECH. ASSOC., March 2007, pp. 1-129.	
	NPL32	MetaRAM Develops New Technology That Quadruples Memory Capacity of Servers and Workstations; Reduces Price by Up to 90 Percent", Press Release provided by MetaRAM and published on MarketWired.com, February 25,2008, 3 pages.	
	NPL33	Microsoft Computer Dictionary Fifth Edition, 9 pages.	
	NPL34	Microsoft Windows 2000 Professional Resource Kit, 76 pages.	
	NPL35	Mutnuary, B. et al., "Analysis of Fully Buffered DIMM Interface in High-speed Server Applications", IBM Corp, xSeries eServer Development, 2006 Electronic Components and Technology Conference, pp. 203-208.	
	NPL36	Notice of Allowance in U.S. Application No. 12/240,916, mailed on September 17, 2012.	
	NPL37	Notice of Allowance in U.S. Patent Application No. 13/536,173, mailed July 2, 2013.	
	NPL38	Notice of Allowance in U.S. Patent Application No. 13/559,476, mailed May 6, 2014.	
	NPL39	Notice of Allowance in U.S. Patent Application No. 13/559,476, mailed September 29 ,2014.	
	NPL40	Notice of Allowance in U.S. Patent Application No. 13/905,048, mailed December 19,2013, 8 pages.	

Examiner Signature	/HASHEM FARROKH/	Date Considered	03/16/2019

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				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	To be assigned
				Examiner Name	To be assigned
Sheet	5	of	8	Attorney Docket Number	0016.001000G

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	NPL41	Notice of Allowance in U.S. Patent Application No. 13/905,053, mailed December 11, 2013.	
	NPL42	Notice of Allowance in U.S. Patent Application No. 14/173,219 dated July 7, 2014.	
	NPL43	Notice of Allowance in U.S. Patent Application No. 14/489,269, mailed October 8, 2015.	
	NPL44	Office Action dated August 19, 2016 of the Chinese Patent Application No. 201280047758.X	
	NPL45	Office Action in U.S. Application No. 13/536,176, mailed on April 15, 2013.	
	NPL46	Office Action in U.S. Patent Application No. 12/240,916, mailed April 3, 2012 pp.1-12.	
	NPL47	Office Action in U.S. Patent Application No. 12/240,916, mailed February 1, 2012 pp 1-14.	
	NPL48	Office Action in U.S. Patent Application No. 12/240,916, mailed July 29, 2011 pp.1-8.	
	NPL49	Office Action in U.S. Patent Application No. 13/536,173, mailed April 15, 2013.	
	NPL50	Office Action in U.S. Patent Application No. 13/625,563, mailed August 5, 2013.	

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Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	Filed herewith
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	To be assigned
				Examiner Name	To be assigned
Sheet	6	of	8	Attorney Docket Number	0016.001000G

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	NPL51	Office Action in U.S. Patent Application No. 13/625,563, mailed May 9, 2014.	
	NPL52	Office Action in U.S. Patent Application No. 13/905,048, mailed August 1, 2013.	
	NPL53	Office Action in U.S. Patent Application No. 13/905,053, mailed August 1, 2013.	
	NPL54	Office Action in U.S. Patent Application No. 14/173,219, mailed March 13, 2014, pp.1-7.	
	NPL55	Office Action in U.S. Patent Application No. 14/173,242, mailed March 14, 2014, pp.1-7	
	NPL56	Office Action in U.S. Patent Application No. 14/302,292, mailed December 21, 2015.	
	NPL57	Out of Stealth Mode, Start-Up MetaRAM Unveils New Technology That Quadruples DRAM Capacity, Press Release edited by Storage Newsletter on February 28, 2008 at StorageNewsLetter.com, 8 pages.	
	NPL58	PATTERSON et al., "Computer Organization & Design: The Hardware/Software Interface" Morgan Kaufmann Publishers, Inc. (1998).	
	NPL59	Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SanDisk, Corp.), filed June 20, 2014.	
	NPL60	Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed August 22, 2014.	

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				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	To be assigned
				Examiner Name	To be assigned
Sheet	7	of	8	Attorney Docket Number	0016.001000G

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	NPL61	Petition for Inter Partes Review of U.S. Patent No. 8,301,833, filed September 29, 2008.	
	NPL62	Petition for Inter Partes Review of U.S. Patent No. 8,516,187 (on behalf of SanDisk, Corp.), filed June 19, 2014.	
	NPL63	Petition for Inter Partes Review of U.S. Patent No. 8,516,187 (on behalf of SMART Modular Technologies, Inc.), filed August 22, 2014.	
	NPL64	Petition for Inter Partes Review of U.S. Patent No. 8,671,243, filed May 29, 2013.	
	NPL65	Petition for Inter Partes Review of U.S. Patent No. 8,874,831, filed July 26, 2012.	
	NPL66	Provisional Application No. 60/912,321 filed April 17, 2007	
	NPL67	Provisional Application No. 60/941,586, filed June 1, 2007	
	NPL68	Restriction Requirement in U.S. Patent Application No. 12/240,916, mailed March 31, 2011.	
	NPL69	Smart Storage Systems, Inc's Invalidity Contentions, Case No. 4:13-cv-05889-YGR, dated June 6, 2014.	
	NPL70	Using Two Chip Selects to Enable Quad Rank, an IP.com Prior Art Database Technical Disclosure, IP.com Electronic Publication: December 17, 2005, 2 pages.	

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	NPL71	Webster's II New College Dictionary, Houghton Mifflin Company, Boston, MA, 2001, pp. 259, 1115.	
	NPL72	WONG, A. "The BIOS Optimization Guide", Adrian's Rojak Pot, Rev. 6.2, 1998-2001, 67 pages.	

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All References Considered Except Where Lined Through. /H.F/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	205	(first adj2 memory) with (manager or controller) with (first adj data adj bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/17 11:18
L3	205	(second adj2 memory) with (manager or controller) with (second adj data adj bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/17 11:18
L4	16	(non$1volatile or flash or SSD) with (manager or controller) with (third adj data adj bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/17 11:18
L5	8	(L2 and L3 and L4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/17 11:18
L6	2	4 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/17 11:24
L7	99	(2 and 3) and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/17 11:26
L8	27	7 and (non$1volatile or flash or SSD)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/17 11:27
L9	185	2 and 3	US-PGPUB;	OR	ON	2019/03/17

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:30
L10	121	9 AND ((G06F13/1694 OR G06F12/0246 OR G06F13/28 OR G06F13/4243 OR G06F2212/7208 OR G06F3/0685 OR G06F12/0638 OR G06F13/4027 OR G06F1/185 OR G06F2212/205 OR G06F3/0613 OR G06F3/0659 OR G11C7/1072 OR G11C14/0018).CPC. OR (711/104 OR 711/110).CCLS. OR (G11C7/10 OR G11C14/00 OR G06F13/16 OR G06F3/06 OR G06F12/02 OR G06F13/40 OR G06F13/28 OR G06F12/06 OR G06F13/42 OR G06F1/18).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/17 11:48
L11	55	10 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/17 11:48
L12	7	11 and (non$1volatile or flash or SSD)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/17 11:52
S1	1	"15934416"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 20:24
S2	1200	Lee-Hyun.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 20:28
S3	70	Chen-Chi-She.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 20:28
S4	70	Solomon-Jeffrey-C.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 20:29
S5	31	Milton-Scott-H.in.	US-PGPUB;	OR	ON	2019/03/16

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			20:30
S6	36	Bhakta-Jayesh.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 20:30
S7	205	(first adj2 memory) with (manager or controller) with (first adj data adj bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 20:34
S8	205	(second adj2 memory) with (manager or controller) with (second adj data adj bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 20:36
S9	16	(non$1volatile or flash or SSD) with (manager or controller) with (third adj data adj bus)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 20:39
S10	3	(S7 and S8 and S9).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 20:40
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		"20130086309" "20130254456" "20130254497" "20140032820" "20140059170" "20140156919" "20140156920" "20150058701").pn.				
S12	377	("2,043,099" "3,562,555" "3,916,390" "4,234,920" "4,420,821" "4,449,205" "4,882,709" "4,965,828" "5,430,742" "5,490,155" "5,519,663" "5,519,831" "5,563,839" "5,577,213" "5,619,644" "5,675,725" "5,799,200" "5,813,029" "5,870,350" "5,874,995" "5,890,192" "5,953,215" "5,991,885" "6,023,421" "6,026,465" "6,065,092" "6,112,310" "6,145,068" "6,158,015" "6,199,142" "6,216,247" "6,269,382" "6,336,174" "6,336,176" "6,421,279" "6,459,647" "6,487,102" "6,487,623" "6,614,685" "6,658,507" "6,691,209" "6,693,840" "6,721,860" "6,769,081" "6,799,241" "6,810,513" "6,816,982" "6,944,042" "6,948,029" "6,952,368" "7,053,470" "7,062,618" "7,089,412" "7,102,391" "7,136,978" "7,155,627" "7,200,021" "7,234,099" "7,353,325" "7,409,491" "7,409,590" "7,411,859" "7,421,552" "7,467,251" "7,519,754" "7,716,411" "7,818,488" "7,873,750" "8,086,955" "8,102,614" "8,233,303" "8,301,833" "8,407,395" "8,412,879" "8,516,187" "8,671,243" "8,677,060" "8,874,831" "8,880,791" "8,904,098" "8,904,099" "9,043,677" "9,158,684" "9,361,250" "9,436,600" "9,921,762").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 21:09
S13	0	(S7 and S8 and S9) and (S11 or S12)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 21:10
S14	26	("0090235038" "20100122200" "20120110417" "20030206478" "20050204091" "6,363,450" "9,921,762" "9,928,186").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 21:34
S15	1	(S7 and S8 and S9) and (S14)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 21:34
S16	6	"9928186".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/03/16 21:57

3/ 17/ 2019 12:04:42 PM
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.
CONFIRMATION NO.: 2728
SERIAL NO.: 15/934,416
ART UNIT: ~~2185~~ 2131
FILING DATE: 03-23-2018
EXAMINER: ~~TBA~~ H. Farrokh
TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Notice of Prior and Concurrent Proceedings

Applicant hereby calls to the attention of the Patent and Trademark Office the following *inter partes* review proceedings involving patents that are commonly-assigned with the patent in the above-identified patent application:

Proceeding	Status
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00365 (P.T.A.B.), filed December 27, 2017	Institution Granted 8/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00364 (P.T.A.B.), filed December 27, 2018	Institution Granted 8/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00363 (P.T.A.B.), filed December 22, 2017	Institution Granted 6/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00362 (P.T.A.B.), filed December 22, 2017	Institution Granted 6/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00303 (P.T.A.B.), filed December 14, 2018	Institution Granted 5/24/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00730 (P.T.A.B.), filed January 20, 2017	Terminated 5/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00692 (P.T.A.B.), filed January 17, 2017	Terminated 7/5/2018

All References Considered Except Where Lined Through. /H.F/

Proceeding	Status
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00668 (P.T.A.B.), filed January 13, 2017	Terminated 7/18/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00667 (P.T.A.B.), filed January 13, 2017	Terminated 7/5/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00649 (P.T.A.B.), filed January 13, 2017	Terminated 5/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00587 (P.T.A.B.), filed January 6, 2017	Terminated 7/20/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00577 (P.T.A.B.), filed January 5, 2017	Terminated 7/5/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00560 (P.T.A.B.), filed January 3, 2017	Terminated 6/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00562 (P.T.A.B.), filed January 17, 2017	Terminated 9/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00561 (P.T.A.B.), filed January 17, 2017	Terminated 9/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00548 (P.T.A.B.), filed January 17, 2017	Terminated 5/3/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00549 (P.T.A.B.), filed January 17, 2017	Terminated 5/3/2018

Information Disclosure Statement

Listed on accompanying IDS Forms PTO/SB/08a equivalent and/or PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

All References Considered Except Where Lined Through. /H.F/

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

Copies of documents **NPL6 – NPL37** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of U.S. patents and patent application publications are submitted.

It is expected that the examiner will review the prosecution and cited art in the parent application no(s). 14/840,865, filed 08-31-215 (now U.S. Pat. No. 9,928,186); 14/489,269, filed 09-17-2014 (now U.S. Pat. No. 9,158,685); 13/559,476, filed 07-26-2012 (now U.S. Pat. No. 8,874,831); 12/240,916, filed 09-29-2008 (now U.S. Pat. No. 8,301,833); and 12/131,873, filed 06-02-2008 (now abandoned) in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from co-pending U.S. Patent Application No(s). 14/214,652, filed March 24, 2014 as documents **NPL1 – NPL5**.

All References Considered Except Where Lined Through. /H.F/

The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 60-2034.

Respectfully submitted,

SHAMI MESSINGER PLLC

Dated: October 17, 2018

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
Tel: 202-516-6900

All References Considered Except Where Lined Through. /H.F/

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	2185
				Examiner Name	To be assigned
Sheet	1	of	1	Attorney Docket Number	0016.001000G

U.S. PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Document Number Number-Kind Code [2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US1	2012/0110417 A1	05-03-2012	D'Abreu	
	US2	2010/0122200 A1	05-13-2010	Merry, Jr.	
	US3	2009/0235038 A1	09-17-2009	Sartore	
	US4	6839774 B1	01-04-2005	Ahn et al.	
	US5	2003/0206478 A1	11-06-2003	Ayukawa et al.	
	US6	2005/0204091 A1	03-20-2005	Kilbuck et al.	
	US7	9,921,762 B2	03-20-2018	Amidi et al.	
	US8	9,928,186 B2	03-27-2018	Lee et al.	
	US9	6,363,450 B1	03-26-2002	Lash et al.	

FOREIGN PATENT DOCUMENTS

Examiner initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T 6

Examiner Signature	/HASHEM FARROKH/	Date Considered	03/17/2019

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

All References Considered Except Where Lined Through. /H.F/

Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	2185
				Examiner Name	To be assigned
Sheet	1	of	4	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	NPL1	Copy of Non-Final Office Action for U.S. Appl. No. 14/214,652, mailed March 8, 2018; 41 pages.	
	NPL2	Copy of Examiner Search Notes for U.S. Appl. No. 14/214,652, mailed March 8, 2018; 3 pages.	
	NPL3	Copy of Examiner Notice of References Cited for U.S. Appl. No. 14/214,652, mailed March 8, 2018; 1 page.	
	NPL4	Extended European search report issuing from European Patent Application 17191878.2, August 2, 2018, 9 pgs.	
	NPL5	Copy of Final Office Action for U.S. Appl. No. 15/000,834, mailed May 3, 2018;16 pages.	
	NPL6	Patent Owner's Preliminary Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00365 (P.T.A.B.), filed May 7, 2018; 47 pages.	
	NPL7	Patent Owner's Preliminary Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00364 (P.T.A.B.), filed May 7, 2018; 47 pages.	
	NPL8	Patent Owner's Preliminary Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00363 (P.T.A.B.), filed May 7, 2018; 42 pages.	
	NPL9	Patent Owner's Preliminary Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00362 (P.T.A.B.), filed May 7, 2018; 41 pages.	
	NPL10	Patent Owner's Supplemental Mandatory Notices, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed September 17, 2018; 3 pages.	

Examiner Signature	/HASHEM FARROKH/	Date Considered	03/17/2019

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449/PTO				*Complete if Known*	
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				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	2185
				Examiner Name	To be assigned
Sheet	2	of	4	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL11	Patent Owner's Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed August 10, 2018; 65 pages.	
	NPL12	Patent Owner's Preliminary Response, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed March 19, 2018; 59 pages.	
	NPL13	Netlist Inc.'s Notice of Appeal to the U.S. Court of Appeals for the Federal Circuit and Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00562 (P.T.A.B.), filed September 6, 2018; 56 pages.	
	NPL14	Netlist Inc.'s Notice of Appeal to the U.S. Court of Appeals for the Federal Circuit and Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00561 (P.T.A.B.), filed September 6, 2018; 67 pages.	
	NPL15	Netlist Inc.'s Notice of Appeal to the U.S. Court of Appeals for the Federal Circuit and Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00560 (P.T.A.B.), filed June 29, 2018; 22 pages.	
	NPL16	Patent Owner's Supplemental Mandatory Notices, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00549 (P.T.A.B.), filed April 19, 2018; 4 pages.	
	NPL17	Patent Owner's Supplemental Mandatory Notices, filed in *Sandisk Corp. v. Netlist, Inc.,* Case No. IPR2015-01020 (P.T.A.B.), filed April 19, 2018; 3 pages.	
	NPL18	Netlist Inc.'s Notice of Appeal and Decision on Remand, filed in *Diablo Technologies, Inc. v. Netlist, Inc.,* Case No. IPR2014-01011 (P.T.A.B.), filed May 30, 2018; 33 pages.	
	NPL19	Netlist Inc.'s Notice of Appeal and Decision on Remand, filed in *Diablo Technologies, Inc. v. Netlist, Inc.,* Case No. IPR2014-00883 (P.T.A.B.), filed May 30, 2018; 28 pages.	
	NPL20	Netlist Inc.'s Notice of Appeal and Decision on Remand, filed in *Diablo Technologies, Inc. v. Netlist, Inc.,* Case No. IPR2014-00882 (P.T.A.B.), filed May 30, 2018; 28 pages.	

Examiner Signature	/HASHEM FARROKH/	Date Considered	03/17/2019

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	2185
				Examiner Name	To be assigned
Sheet	3	of	4	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL21	Supplemental Declaration of Robert J. Murphy, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed August 10, 2018; 76 pages.	
	NPL22	Deposition of Donald Alpert, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed July 20, 2018; 218 pages.	
	NPL23	Joint List of Claim Terms For Construction and Proposed Constructions, filed as Exhibit 2007 in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed August 10, 2018; 23 pages.	
	NPL24	Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00362 and IPR2018-00363 (P.T.A.B.), entered June 29, 2018; 33 pages.	
	NPL25	"The Authoritative Dictionary of IEEE Standards Terms," 7th Ed. 2000, pp. 1 - 10.	
	NPL26	"The Authoritative Dictionary of IEEE Standards Terms," 6th Ed. 2000, pp. 1 - 8.	
	NPL27	"Orbit Micro News and Notes," available at http://www.orbitmicro.com/company/blog/87; 10 pages.	
	NPL28	Jacob, B. et al, "Memory Systems: Cache, DRAM, Disk, Chapter 30" New York, NY: Morgan Kaufmann Press, 2008; 40 pages.	
	NPL29	Declaration of Robert J. Murphy, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00303 (P.T.A.B.), filed March 19, 2001; 71 pages.	
	NPL30	Decision Instituting *Inter Partes* Review of U.S. Patent No. 9,535,623, Entered May 24, 2018, 18 pages.	

Examiner Signature	/HASHEM FARROKH/	Date Considered	03/17/2019

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Equivalent of Form PTO/SB/08b (7-09)

Substitute for form 1449/PTO				*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	15/934,416
				Filing Date	03-23-2018
				First Named Inventor	Hyun Lee
				Art Unit	2185
				Examiner Name	To be assigned
Sheet	4	of	4	Attorney Docket Number	0016.001000G

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume number, publisher, city and/or country where published	T[2]
	NPL31	Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.*, Case No. IPR2018-00587 (P.T.A.B.), entered June 20, 2018; 53 pages.	
	NPL32	Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.*, Case No. IPR2018-00692 (P.T.A.B.), entered July 5, 2018; 44 pages.	
	NPL33	Patent Owner's Motion to Strike, filed in *SK HYNIX et al. v. Netlist, Inc.*, Case No. IPR2018-00562 (P.T.A.B.), entered March 28, 2018; 8 pages.	
	NPL34	Petitioner's Opposition to Patent Owner's Motion to Strike, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2018-00562 (P.T.A.B.), entered April 4, 28, 2018; 8 pages.	
	NPL35	Record of Oral Hearing, filed in *SK HYNIX et al. v. Netlist, Inc.*, Case No. IPR2018-00562 (P.T.A.B.), held April 6, 28, 2018; 68 pages.	
	NPL36	Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2017-00548 (P.T.A.B.), entered May 3, 2018; 18 pages.	
	NPL37	Final Written Decision, filed in *SK HYNIX et al. v. Netlist, Inc.,* Case No. IPR2017-00549 (P.T.A.B.), entered May 3, 2018; 16 pages.	
	NPL38		
	NPL39		
	NPL40		

Examiner Signature	/HASHEM FARROKH/	Date Considered	03/17/2019

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

All References Considered Except Where Lined Through. /H.F/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.
CONFIRMATION NO.: 2728
SERIAL NO.: 15/934,416
ART UNIT: ~~2185~~ 2131
FILING DATE: 03-23-2018
EXAMINER: ~~TBA~~ H. Farrokh
TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Notice of Prior and Concurrent Proceedings

Applicant hereby calls to the attention of the Patent and Trademark Office the following *inter partes* review proceedings involving patents that are commonly-assigned with the patent in the above-identified patent application:

Proceeding	Status
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00365 (P.T.A.B.), filed December 27, 2017	Institution Granted 8/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00364 (P.T.A.B.), filed December 27, 2018	Institution Granted 8/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00363 (P.T.A.B.), filed December 22, 2017	Institution Granted 6/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00362 (P.T.A.B.), filed December 22, 2017	Institution Granted 6/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2018-00303 (P.T.A.B.), filed December 14, 2018	Institution Granted 5/24/2018
~~*SK HYNIX et al. v. Netlist, Inc.*, Case No. IPR2017-00730 (P.T.A.B.), filed January 20, 2017~~	~~Terminated 5/29/2018~~
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00692 (P.T.A.B.), filed January 17, 2017	Terminated 7/5/2018

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

Proceeding	Status
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00668 (P.T.A.B.), filed January 13, 2017	Terminated 7/18/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00667 (P.T.A.B.), filed January 13, 2017	Terminated 7/5/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00649 (P.T.A.B.), filed January 13, 2017	Terminated 5/29/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00587 (P.T.A.B.), filed January 6, 2017	Terminated 7/20/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00577 (P.T.A.B.), filed January 5, 2017	Terminated 7/5/2018
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SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00562 (P.T.A.B.), filed January 17, 2017	Terminated 9/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00561 (P.T.A.B.), filed January 17, 2017	Terminated 9/6/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00548 (P.T.A.B.), filed January 17, 2017	Terminated 5/3/2018
SK HYNIX et al. v. Netlist, Inc., Case No. IPR2017-00549 (P.T.A.B.), filed January 17, 2017	Terminated 5/3/2018

/HASHEM FARROKH/ 03/16/2019

Information Disclosure Statement

Listed on accompanying IDS Forms PTO/SB/08a equivalent and/or PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

Copies of documents **NPL1** and **NPL2** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of U.S. patents and patent application publications are submitted.

It is expected that the examiner will review the prosecution and cited art in the parent application no(s). 14/840,865, filed 08-31-215 (now U.S. Pat. No. 9,928,186); 14/489,269, filed 09-17-2014 (now U.S. Pat. No. 9,158,685); 13/559,476, filed 07-26-2012 (now U.S. Pat. No. 8,874,831); 12/240,916, filed 09-29-2008 (now U.S. Pat. No. 8,301,833); and 12/131,873, filed 06-02-2008 (now abandoned) in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 60-2034.

Respectfully submitted,

SHAMI MESSINGER PLLC

Dated: December 17, 2018

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
Tel: 202-516-6900

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.	CONFIRMATION NO: 2728
SERIAL NO: 15/934,416	ART UNIT: 2131
FILING DATE: 3/23/18	EXAMINER: FARROKH, Hashem

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND/OR REPLY TO OFFICE ACTION

Commissioner:

In response to the Office Action mailed March 21, 2019, Applicant submits the following Amendment and Remarks.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page **2**.

Remarks begin on page **6**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2034.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (New) A memory system, comprising:

a memory device including a first memory portion and a second memory portion; and

a controller coupled to a system memory controller of a host system and to the memory device, the controller is configured to transfer data information from the second memory portion to the first memory portion in response to a first command received by the controller from the system memory controller, the controller is further configured to alert the system memory controller when the data information is ready to be retrieved, and wherein the data information is retrieved from the second memory portion in response to a second command received by the controller from the system memory controller.

3. (New) The memory system of claim 1, wherein the first memory portion includes volatile memory, and wherein the second memory portion includes non-volatile memory.

4. (New) The memory system of claim 1, wherein the first memory portion includes dynamic random access memory (DRAM), and wherein the second memory portion includes FLASH memory.

5. (New) The memory system of claim 1, wherein the first command received from the system memory controller corresponds to a memory read operation received from the system memory controller in accordance with a protocol.

6. (New) The memory system of claim 1, wherein the controller is coupled to the system memory controller of the host system via system address lines, wherein the controller is further configured to determine an address of the data information based on a first number of address bits and a second number of address bits, and wherein the controller is configured to receive the first number of address bits and the second number of address bits sequentially over the system address lines.

7. (New) The memory system of claim 6, wherein the controller is configured to concatenate the first number of address bits and the second number of address bits to determine the address of the data information.

8. (New) The memory system of claim 7, wherein the first number of address bits is twelve.

9. (New) The memory system of claim 5, wherein the controller is further configured to receive the second command from the system memory controller according to the protocol.

10. (New) A memory module couplable to a system memory controller of a host system, the memory module comprising:

a controller operable to receive from the system memory controller a first memory access command via system address lines;

a non-volatile memory device; and

a volatile memory device;

wherein, in response to the first memory access command, the controller is configured to determine if data associated with the first memory access command is stored in the volatile memory device or the non-volatile memory device, and if the data associated with the first memory access command does not reside in the volatile memory device, the controller is further configured to perform a data transfer operation of the data associated with the first memory access command from the non-volatile memory device to the volatile memory device; wherein the controller is further configured to alert the system memory controller that the data associated with the first memory access command is ready to be retrieved from the volatile memory device; and wherein the data associated with the first memory access command is retrieved from the volatile memory device in response to a second memory access command received by the controller from the system memory controller.

11. (New) The memory module of claim 10, wherein the volatile memory device includes dynamic random access memory (DRAM), and wherein the volatile memory device includes FLASH memory.

12. (New) The memory module of claim 10, wherein the first memory access command received from the system memory controller corresponds to a memory read operation according to a protocol.

13. (New) The memory module of claim 12, wherein the first memory access command received from the system memory controller includes a first command RC(X) received from the system memory controller over the system address lines and a second command RC(X+1) received after the first command RC(X) from the system memory controller over the system address lines.

14. (New) The memory module of claim 13, wherein the first command RC(X) includes a first number of address bits, and wherein the second command RC(X+1) includes a second number of address bits in accordance with the protocol.

15. (New) The memory module of claim 14, wherein the controller is further configured to determine an address of the data associated with the first memory access command based on the first number of address bits and the second number of address bits.

16. (New) The memory module of claim 14, wherein the first number of address bits is equal to twelve.

17. (New) The memory module of claim 14, wherein the controller is further configured to concatenate the first number of address bits and the second number of address bits to determine an address of the data associated with the first memory access command.

18. (New) The memory module of claim 10, wherein the controller is further configured to receive the second memory access command according to the protocol.

19. (New) A memory module couplable to a system memory controller of a host system, comprising:

a controller operable to receive from the system memory controller a first memory access command, the first memory access command including a first address;

a non-volatile memory device;

a volatile memory device; and

a data manager coupled to the non-volatile memory device and the volatile memory device, the data manager configured to exchange data with the memory controller via a data interface in response to control information received from the controller;

wherein, in response to the first memory access command, the controller is configured to determine if data associated with the first address is stored in the volatile memory device or the non-volatile memory device;

wherein, if the data associated with the first address does not reside in the volatile memory device, the controller is configured to perform a data transfer operation from the non-volatile memory device to the volatile memory device by way of the data manager;

wherein the controller is further configured to alert the memory controller that the data associated with the first address is ready to be retrieved from the volatile memory device; and wherein the data associated with the first address is retrieved from the volatile memory device in response to a second memory access command received by the controller from the system memory controller.

20. (New) The memory module of claim 19, further comprising:

a register configured to register multiple commands or a sequence of commands.

21. (New) The memory module of claim 20, wherein the first memory access command correspond to a memory read operation.

REMARKS

Applicant has received and carefully reviewed the non-final Office Action of May 30, 2019. Applicant respectfully requests reconsideration in view of the following remarks.

Upon entry of the foregoing amendment, claims 2-21 are pending in this application, with claims 2, 10 and 19 being independent.

Amendment to Claims

No amendment made is related to the statutory requirements of patentability unless expressly stated herein. No amendment is made for the purpose of narrowing the scope of any claim, unless Applicant argues herein that such amendment is made to distinguish over a particular identified reference or combination of references. Any remarks made herein with respect to a given claim or amendment is intended only in the context of that specific claim or amendment, and should not be applied to other claims, amendments or aspects of the claimed arrangement.

Canceled Claims

Claim 1 has been canceled without prejudice or disclaimer of the subject matter contained therein.

Double Patenting

Claim 1 stands rejected double patenting as allegedly being unpatentable over claim 1 of U.S. Pat. No. 9,928,186. Claim 1 has been canceled and the rejection thereof is moot.

Newly-Added Claims

Claims 2-21 have been added to further particularly point out and distinctly claim the subject matter of the claimed arrangement.

Conclusion

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 60-2034.

Respectfully submitted,

Dated: July 22, 2019

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
202-516-6900

Electronic Patent Application Fee Transmittal

Application Number:	15934416
Filing Date:	23-Mar-2018
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Stephanie Semler
Attorney Docket Number:	0016.001000G

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
		Total in USD ($)		**200**

Electronic Acknowledgement Receipt	
EFS ID:	36657823
Application Number:	15934416
International Application Number:	
Confirmation Number:	2728
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000G
Receipt Date:	22-JUL-2019
Filing Date:	23-MAR-2018
Time Stamp:	23:21:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$200
RAM confirmation Number	072319INTEFSW23220300
Deposit Account	602034
Authorized User	Stephanie Semler
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		0016001000G_RespNFOA.pdf	91942 2cc862c5551c0260434f9970036299ffeb165558	yes	7

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Claims	2	5
Applicant Arguments/Remarks Made in an Amendment	6	7

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30593 5c426c9eb190d3c17aa70ad845f8f987a2107f4c	no	2

Warnings:

Information:

Total Files Size (in bytes):	122535

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/934,416	Filing Date 03/23/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	07/22/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/BRENDA V HARRISON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.	CONFIRMATION NO: 2728
SERIAL NO: 15/934,416	ART UNIT: 2131
FILING DATE: 3/23/18	EXAMINER: FARROKH, Hashem

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT

Commissioner:

In response to the non-final Office Action mailed March 21, 2019, and as a supplement to the Amendment filed July 22, 2019, Applicant submits the following Supplemental Amendment and Remarks.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page **2**.

Remarks begin on page **7**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2034.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Currently amended) A memory system, comprising:

a memory ~~device~~ subsystem including a first memory portion and a second memory portion; and

a controller configured to be coupled to a system memory controller of a host system and to the memory ~~device~~subsystem, the controller ~~is configured~~operable to transfer data information from the second memory portion to the first memory portion in response to a first command received by the controller from the system memory controller, the controller ~~is~~ further ~~configured~~ operable to alert the system memory controller when the data information is ready to be retrieved, ~~and~~

wherein the data information is retrieved from the ~~second~~ first memory portion in response to a second command received by the controller from the system memory controller.

3. (Currently amended) The memory system of claim 1, wherein the first memory portion includes volatile memory~~,~~ and ~~wherein~~ the second memory portion includes non-volatile memory.

4. (Currently amended) The memory system of claim 1, wherein the first memory portion includes dynamic random access memory (DRAM)~~,~~ and ~~wherein~~ the second memory portion includes FLASH memory.

5. (Previously presented) The memory system of claim 1, wherein the first command received from the system memory controller corresponds to a memory read operation received from the system memory controller in accordance with a protocol.

6. (Currently amended) The memory system of claim 1, wherein the controller is further configured to:

a) be coupled to the system memory controller of the host system via system address lines, ~~wherein the controller is further configured to~~

b) determine an address of the data information to be transferred from the second memory portion to the first memory portion in response to the first command based on a first ~~number~~ set of address bits and a second ~~number~~ set of address bits, and ~~wherein the controller is configured to~~

c) receive the first ~~number~~ set of address bits and the second ~~number~~ set of address bits sequentially over the system address lines.

7. (Currently amended) The memory system of claim 6, wherein the controller is further configured to concatenate the first ~~number~~ set of address bits and the second ~~number~~ set of address bits to determine the address of the data information.

8. (Currently amended) The memory system of claim 7, wherein the first ~~number~~ set of address bits ~~is~~ comprises twelve address bits.

9. (Previously presented) The memory system of claim 5, wherein the controller is further configured to receive the second command from the system memory controller according to the protocol.

10. (Currently amended) A memory module couplable to a system memory controller of a host system via a set of data lines and a set of address and control lines, the memory module comprising:

a controller operable to receive from the system memory controller a first memory ~~access~~ command via the set of system address and control lines;

a non-volatile memory device; and

a volatile memory device~~;~~,

wherein, in response to the first memory ~~access~~ command, the controller is configured to ~~determine if data associated with the first memory access command is stored in the volatile memory device or the non-volatile memory device, and if the data associated with the first~~

~~memory access command does not reside in the volatile memory device, the controller is further configured to~~ :

a) perform a data transfer operation ~~of the data associated with the first memory access command~~ from the non-volatile memory device to the volatile memory device if data information associated with the first memory command does not reside in the volatile memory device, and~~; wherein the controller is further configured to~~

b) alert the system memory controller ~~that~~ when the data information associated with the first memory ~~access~~ command is ready to be retrieved from the volatile memory device; and

wherein the data information associated with the first memory ~~access~~ command is retrieved from the volatile memory device in response to a second memory ~~access~~ command received by the controller from the system memory controller.

11. (Currently amended) The memory module of claim 10, wherein the volatile memory device includes dynamic random access memory (DRAM)~~,~~ and ~~wherein~~ the non-volatile memory device includes FLASH memory.

12. (Currently amended) The memory module of claim 10, wherein the first memory ~~access~~ command received from the system memory controller corresponds to a memory read operation according to a protocol.

13. (Currently amended) The memory module of claim 12, wherein the first memory ~~access~~ command ~~received from the system memory controller~~ includes a first command RC(X) received from the system memory controller over the set of system address and control lines and a second command RC(X+1) received after the first command RC(X) from the system memory controller over the set of system address and control lines.

14. (Currently amended) The memory module of claim 13, wherein the first command RC(X) includes a first number of address bits~~,~~ and ~~wherein~~ the second command RC(X+1) includes a second number of address bits in accordance with the protocol.

15. (Currently amended) The memory module of claim 14, wherein the controller is further configured to determine an address of the data information associated with the first memory ~~access~~ command based on the first number of address bits and the second number of address bits.

16. (Previously presented) The memory module of claim 14, wherein the first number of address bits is equal to twelve.

17. (Currently amended) The memory module of claim 14, wherein the controller is further configured to concatenate the first number of address bits and the second number of address bits to determine an address of the data information associated with the first memory ~~access~~ command.

18. (Currently amended) The memory module of claim ~~10~~12, wherein the controller is further configured to receive the second memory ~~access~~ command according to the protocol.

19. (Currently amended) A memory module couplable to a system memory controller of a host system via a set of data lines and a set of system address and control lines, the memory module, comprising:

a controller operable to receive from the system memory controller a first memory ~~access~~ command via the set of system address and control lines~~, the first memory access command including a first address~~;

a non-volatile memory device;

a volatile memory device; and

a data manager coupled to the system memory controller, the non-volatile memory device, and the volatile memory device, wherein the data manager is configured to exchange data with one or more of the non-volatile memory device, the volatile memory device, and the system memory controller ~~via a data interface~~ in response to control information received from the controller;

wherein, in response to the first memory ~~access~~ command, the controller is configured to: ~~determine if data associated with the first address is stored in the volatile memory device or the non-volatile memory device;~~

~~wherein, if the data associated with the first address does not reside in the volatile memory device, the controller is configured to~~

a) perform a data transfer operation from the non-volatile memory device to the volatile memory device by way of the data manager if data information associated with the first memory command does not reside in the volatile memory device,~~;~~ and

b) ~~wherein the controller is further configured to~~ alert the system memory controller ~~that~~ when the data associated with the first ~~address~~ memory command is ready to be retrieved from the volatile memory device,~~;~~ and

wherein the data associated with the first ~~address~~ memory command is retrieved from the volatile memory device in response to a second memory ~~access~~ command received by the controller from the system memory controller.

20. (Previously presented) The memory module of claim 19, further comprising:

a register configured to register multiple commands or a sequence of commands.

21. (Currently amended) The memory module of claim ~~20~~19, wherein the first memory ~~access~~ command received by the controller from the system memory controller corresponds ~~correspond~~ to a memory read operation comprising a first command including a first set of address bits and a second command including a second set of address bits, wherein the second command is received by the controller after the first command is received by the controller, and wherein the controller is configured to determine an address of the data information associated with the first memory command using the first set of address bits and the second set of address bits.

REMARKS

Applicant has received and carefully reviewed the non-final Office Action mailed March 21, 2019. Applicant respectfully requests reconsideration in view of the following remarks.

Upon entry of the foregoing amendment, claims 2-21 are pending in this application, with claims 2, 10 and 19 being independent.

Amendment to Claims

The claims have been amended for improved readability and to better claim what the Applicant had a right to claim. No amendment made is related to the statutory requirements of patentability unless expressly stated herein. No amendment is made for the purpose of narrowing the scope of any claim, unless Applicant argues herein that such amendment is made to distinguish over a particular identified reference or combination of references. Any remarks made herein with respect to a given claim or amendment is intended only in the context of that specific claim or amendment, and should not be applied to other claims, amendments or aspects of the claimed arrangement.

Conclusion

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 60-2034.

Respectfully submitted,

Dated: August 26, 2019

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
202-516-6900

Electronic Acknowledgement Receipt

EFS ID:	36976175
Application Number:	15934416
International Application Number:	
Confirmation Number:	2728
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000G
Receipt Date:	26-AUG-2019
Filing Date:	23-MAR-2018
Time Stamp:	15:21:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		0016001000G_SuppResp_NFOA_man.pdf	99314 ccf457a170e67c5d14f3ea90707e4b60180003e0	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Supplemental Response or Supplemental Amendment	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	8
Warnings:			
Information:			
	Total Files Size (in bytes):	99314	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/934,416	03/23/2018	Hyun Lee	0016.001000G	2728

151145 7590 10/15/2019

Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2131	

NOTIFICATION DATE	DELIVERY MODE
10/15/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

khaled@shamimessinger.com
mike@shamimessinger.com
stephanie@shamimessinger.com

Office Action Summary	**Application No.** 15/934,416	**Applicant(s)** Lee et al.	
	Examiner HASHEM FARROKH	**Art Unit** 2131	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 08/26/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 2-21 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 2-21 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 03/23/2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

This office action is in response to the communication(s) filed on 08/26/2019. There are a total 21 claims pending in the application; claim 2 has been canceled and claims 2-21 have been added.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b),** no separate citation of the same prior art need be made by the applicants in the instant application.*

INFORMATION CONCERNING SPECIFICATION:

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

1. Claims 7 and 17 recite"

"…**concatenate** the first set of address bits and the second set address bits…"

(Emphasis added).

The specification fails to provide proper antecedent basis for the above limitation.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> *(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.*

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> *The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

Claims 6-8, 13-17, and 21 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

2. Claim 6 recites, in part, the limitation:

"c) "receive the first set of address bits and the second set of address bits sequentially over the system address lines."

The claimed specification does not describe or support the above limitation as claimed. Claims 7-8 are rejected by virtue of their dependency from claim 6.

3. Claim 7 recites the limitation:

"wherein the controller is further configured to concatenate the first set of address bits and the second set of address bits to determine the address of the data information."

The claimed specification does not describe or support the above limitation as claimed. Claim 8 is rejected by virtue of its dependency from claim 7.

4. Claim 13 recites the limitation:

"wherein the first memory command includes a first command RC(X) receive from the system memory controller over the set of system address and control lines and a second command RC(X+1) received after the first command RC(X) from the system memory controller over the set of system address and control lines."

The claimed specification does not describe or support the above limitation as claimed. Claims 14-17 are rejected at least by virtue of their dependency from claim 13.

5. Claim 15 recites the limitation:

"wherein the controller is further configured to determine an address of the data information associated with the first memory command based on the first number of address bits and the second number of address bits."

The claimed specification does not describe or support the above limitation as claimed.

6. Claim 17 recites the limitation:

"wherein the controller is further configured to concatenate the first number of address bits and the second number of address bits to determine an address of the data information associated with the first memory command."

The claimed specification does not describe or support the above limitation as claimed.

7. Claim 21 recites, in part, the limitation:

"wherein the second command is received by the controller after the first command is received by the controller, and wherein the controller is configured to determine an address of the data information associated with the first memory command using the first set of address bits and the second set of address bits."

The claimed specification does not describe or support the above limitation as claimed.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 2-5, 9-12, and 18-19 are rejected under pre-AIA 35 U.S.C. 102 (a)(2) as anticipated by or, in the alternative, under pre-AIA 35 U.S.C. 103(a) as obvious over Fukuzo "Fukuzo" (US 2006/0294295 A1).

8. In regard to claim 2 Fukuzo teaches:

"A memory system **(e.g., Fig. 3)**, comprising:

"a memory subsystem including a first memory portion **(e.g., ¶ 0080, SDRAM memory chip device 40 in Fig. 3)** and a second memory portion;" **(e.g., ¶ 0080, Flash memory device 60 in Fig. 3).**

"and a controller configured to be coupled to a system memory controller **(e.g., ¶ 0082, CPU 50 of the host system in Fig. 3)** of a host system and to the memory sub system **(e.g., ¶¶ 0081-0082; chip device 40 in Fig. 3 in addition to SDRAM array 190, comprises section 10, 20, and 30 that include controller and/or control logic that coupled system memory and host system such as processor 50 in Fig. 3)**, the controller operable to transfer data information from the second memory portion to the first memory portion in response to a first command received by the controller from the system memory controller **(e.g., ¶¶ 0086-0088; Figs. 3-4)**, the controller further operable to alert the system memory controller when the data information is ready to be retrieved," **(e.g., ¶ 0028, ready or busy status signal in Fig. 3).**

"and wherein the data information is retrieved from the first memory portion in response to a second command received by the controller from the system memory controller." **(e.g., ¶ 0104, ¶ 0127; Figs. 3-5; commands issued by or in response to the commands issued by CPU 50).**

9. In regard to claim 10 Fukuzo teaches:

"A memory module couplable to a system memory controller of a host system **(e.g., CPU 50 IN Fig. 3)** via a set of data lines and a set of address and control lines **(e.g., ¶¶ 0080-0083; Fig. 3)**, the memory module comprising:"

"a controller operable to receive from the system memory controller a first memory command via the set of system address and control lines;" **(e.g., ¶¶ 0080-0083, ¶ 0088; Fig. 3).**

"a non-volatile memory device;" **(e.g., ¶ 0080; flash memory device 60 in Fig. 3).**

"and a volatile memory device;" **(e.g., ¶ 0080; SDRAM memory device 40 in Fig. 3).**

"wherein, in response to the first memory command, the controller is configured to:

a) perform a data transfer operation from the non-volatile memory device to the volatile memory device if data information associated with the first memory command does not reside in the volatile memory device," **(e.g., ¶ 0088; Fig. 3).**

b) and alert the system memory controller when the data information associated with the first memory command is ready to be retrieved from the volatile memory device;" **(e.g., ¶ 0028, ready or busy status signal in Fig. 3).**

"and wherein the data information associated with the first memory retrieved from the volatile memory device in response to a second memory received by the controller from the system memory controller." **(e.g., ¶ 0107; Figs. 3-4).**

10. In regard to claim 19 Fukuzo teaches:

"A memory module couplable to a system memory controller of a host system via a set of data lines and a set of system address and control lines **(e.g., ¶¶ 0080-0083; Fig. 3)**, the memory module comprising:"

"a controller operable to receive from the system memory controller a first memory command via the set of system address and control lines;" **(e.g., ¶¶ 0080-0083, ¶ 0088; Fig. 3).**

"a non-volatile memory device;" **(e.g., ¶ 0080; flash memory device 60 in Fig. 3).**

"a volatile memory device;" **(e.g., ¶ 0080; SDRAM memory device 40 in Fig. 3).**

"and a data manager coupled to the system memory controller **(e.g., CPU 50 IN Fig. 3)**, the non-volatile memory device and the volatile memory device **(e.g., SDRAM 40 comprises controller or data manger to control data transfer or exchange between CPU 50 and Flash memory 60 in Fig. 3)** , wherein the data manager is configured to exchange data with one or more of the non-volatile memory device, the volatile memory device, and the system memory controller in response to control information received from the controller;" **(e.g., ¶¶ 0080-0083, ¶ 0088; Fig. 3; Figs. 3-4 and the corresponding text description).**

"wherein, in response to the first memory command, the controller is configured to:

a) perform a data transfer operation from the non-volatile memory device to the volatile memory device by way of the data manager if data information associated with the first memory command does not reside in the volatile memory devices;" **e.g., ¶ 0088; Fig. 3).**

b) and alert the system memory controller that when the data associated with the first memory command is ready to be retrieved from the volatile memory device;" **(e.g., ¶ 0028, ¶ 0107; ready or busy status signal in Fig. 3).**

"and wherein the data associated with the first memory command is retrieved from the volatile memory device in response to a second memory command received by the controller from the system memory controller." **(e.g., ¶ 0107).**

11. In regard to claim 3 Fukuzo further teaches:

"wherein the first memory portion includes volatile memory **(e.g., SDRAM 40)** and the second memory portion includes non-volatile memory." **(e.g., ¶ 0080; Fig. 3; Flash memory 60).**

12. In regard to claims 4 and 11 Fukuzo further teaches:

"wherein the first memory portion includes dynamic random access memory (DRAM) and the second memory portion includes FLASH memory." **(e.g., ¶ 0080; Fig. 3).**

13. In regard to claims 5 and 12 Fukuzo further teaches:

"wherein the first command received from the system memory controller corresponds to a memory read operation received from the system memory controller in accordance with a protocol." **(e.g., ¶ 0024; a standard set of commands for the NAND-flash controller).**

14. In regard to claims 9 and 18 Fukuzo further teaches:

"wherein the controller is further configured to receive the second command from the system memory controller according to the protocol." **(e.g., ¶ 0082; SDRAM standard).**

Claim 20 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Fukuzo in view of Shiota et al "Shiota" (US 2003/0147297 A1).

15. In regard to claim 20 Fukuzo discloses all limitations include in claim 19 but does not expressly teach while Shiota teaches:

"a register configured to register multiple commands or a sequence of commands." **(e.g., ¶ 0042)** *a register for storing read and write commands.*

Disclosures by Fukuzo and Shiota are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the DRAM chip device taught by Fukuzo to include the command register disclosed by Shiota.
The motivation for including the command register as taught by paragraph [0005] of Shiota is to provide a memory system contributing improvement in efficiency of a data process accompanying a memory access.

Therefore, it would have been obvious to combine teaching of Shiota with Fukuzo to obtain the invention as specified in the claim.

Response to Remarks

Applicant arguments have been fully considered but they are not persuasive. Applicant has canceled the claim 1 and added claims 2-21 and amended the claims. However, as shown above claims are rejected under 35 USC 112, first paragraph and prior arts. The Examiner respectfully submits that amendment do not place the claims in

condition for allowance. Accordingly, the Examiner maintains his position and make this Office Action final.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ann Lo can be reached on (571)272-9767. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/

Primary Examiner, Art Unit 2131

Wednesday, October 9, 2019

Notice of References Cited	Application/Control No. 15/934,416	Applicant(s)/Patent Under Reexamination Lee et al.	
	Examiner HASHEM FARROKH	Art Unit 2131	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20060294295-A1	12-2006	Fukuzo; Yukio	G06F13/1673	711/105
*	B	US-20030147297-A1	08-2003	Shiota, Shigemasa	G06F13/161	365/230.03
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/934,416	Lee et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/17/2019	10/09/2019							
	1	✓	-							
	2		✓							
	3		✓							
	4		✓							
	5		✓							
	6		✓							
	7		✓							
	8		✓							
	9		✓							
	10		✓							
	11		✓							
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	15		✓							
	16		✓							
	17		✓							
	18		✓							
	19		✓							
	20		✓							
	21		✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/934,416	Lee et al.
	Examiner	Art Unit
	HASHEM FARROKH	2131

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F13/1694; G06F12/0246; G06F13/28; G06F13/4243; G06F2212/7208; G06F3/0685; G06F12/0638; G06F13/4027; G06F1/185; G06F2212/205; G06F3/0613; G06F3/0659; G11C7/1072; G11C14/0018	03/17/2019	HF
G06F12/0246; G06F3/0685; G06F12/0638; G06F13/28; G06F2212/7208; G06F3/0613; G06F3/0659; G11C7/1072	10/09/2019	HF

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	110	03/17/2019	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
PALM and Inventor Search	03/16/2019	HF
EAST Text Search	03/16/2019	HF
Google Search	03/17/2019	HF
PALM and Inventor Search Updated	10/09/2019	HF
EAST Text Search Updated	10/09/2019	HF

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	140	((transfer$3 or cop$4 or transmi$5 or retriev$3 or read$3) near5 DRAM near5 (flash or non$1volatile)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:12
L2	1255	Lee-Hyun.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:14
L3	71	Chen-Chi-She.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:14
L4	71	Solomon-Jeffrey-C.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:14
L5	32	Milton-Scott-H.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:14
L6	36	Bhakta-Jayesh.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:14
L7	0	1 and (L2 or L3 or L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:14
L8	2764	((DRAM or SDRAM) with (flash or	US-PGPUB;	OR	ON	2019/10/09

		non$1volatile)).clm.	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			14:15
L9	12	8 and (L2 or L3 or L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:15
L11	80144	((volatile or DRAM or SDRAM) with (flash or non$1volatile or non$1volatile)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:20
L12	46	11 and (L2 or L3 or L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:20
L13	80721	((volatile or DRAM or SDRAM) same (flash or non$1volatile or non$1volatile)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:21
L14	46	13 and (L2 or L3 or L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:21
L15	82852	((volatile or DRAM or SDRAM) and (flash or non$1volatile or non$1volatile)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:23
L16	46	15 and (L2 or L3 or L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:23
L17	9922	((transfer$3 or cop$4 or transmi$5 or retriev$3 or read$3) near5 DRAM near5 (flash or non$1volatile))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2019/10/09 14:28

			IBM_TDB			
L18	5039	17 AND ((G06F12/0246 OR G06F3/0685 OR G06F12/0638 OR G06F13/28 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G11C7/1072).CPC. OR (1/1 OR 711/110).CCLS. OR (G06F3/06 OR G06F12/02 OR G06F13/42 OR G06F12/06 OR G06F13/28 OR G06F13/40 OR G06F1/18 OR G11C7/10).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/09 14:47
S28	1732	(non$1volatile adj DIMM) OR NVDIMM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:11
S29	93195	DRAM near5 ((flash or non$1volatile) adj (memory or storage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:13
S30	510	S28 and S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:13
S31	0	S30 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:15
S32	17112	S29 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:16
S33	0	S28 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:17
S34	1574	(transfer$3 or cop$4 or transmi$5 or retriev$3) near5 DRAM near5 (flash or non$1volatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:21
S35	433	S32 and S34	US-PGPUB;	OR	ON	2019/10/01

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:26
S36	11430	((system adj memory) or HUB) adj controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:26
S37	6	S35 and S36	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:27
S38	1644	NVDIMM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:43
S39	0	S38 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:43
S40	2714	DRAM near5 ((flash or non$1volatile) adj (memory or storage)) near5 controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:44
S41	864	S40 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:45
S42	8	S36 and S41	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 11:46
S43	5	"20100110748"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2019/10/01 15:00

			IBM_TDB			
S44	433460	DRAM near5 ((flash or non$1volatile) adj (memory or storage)) (memory adj controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 15:12
S45	294810	(host or system or HUB) adj controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 15:13
S46	32461	S44 and S45	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 15:14
S47	2259	(transfer$4 or exchang$3 or communicat$4 or transmi$4 or cop$4) near5 (flash or non$1volatile) near5 DRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 15:17
S49	618	S47 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 15:18
S50	273	S46 and S47	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 15:18
S51	33	S50 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/01 15:19
S52	2	"20070136523".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/02 14:27
S53	1512	(transfer$3 or read$3 or cop$4) near5 data near5 (non$1volatile or flash) near5 DRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2019/10/02 15:57

			JPO; DERWENT; IBM_TDB			
S54	3000	(transfer$3 or read$3 or cop$4) near5 data near5 DRAM near5 (host or system or hub)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/02 15:59
S55	253	S53 and S54	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/02 16:00
S56	31	S55 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/02 16:00
S57	78294	DRAM near5 (flash or non$1volatle)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/03 10:29
S58	681	S57 and (DRAM near5 (ready or alert$3 or available))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/03 10:30
S59	206	S58 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/03 10:31
S60	319055	(read$3 or retriev$3) near5 (coomand or intruction or request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/03 10:32
S61	38	S59 and S60	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/03 10:33
S62	10	S61 and ((transfer$4 or copy$4 or transmi$4) near2 (request or	US-PGPUB; USPAT;	OR	ON	2019/10/03 11:13

		command or instruction))	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S63	143	S57 and (DRAM near5 (ready or alert$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/03 11:35
S64	82	S60 and S63	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/03 11:36
S65	21	S64 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/03 11:36
S66	21	S65 and request	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/03 11:44
S67	175386	(DRAM with (flash or non$1volatiel))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 10:46
S68	28769	S67 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 10:48
S69	183	S68 and (DRAM near5 (ready or alert or message))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 10:49
S70	169	S69 and ((read$3 or retriev$3) near5 (request or command or intruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 10:51

S71	153	S70 and ((transfer$4 or cop$4 or load$3 or down$1load$3) near5 (request or command or intruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 10:52
S72	6	S68 and (((signal or flag or interrupt) near5 (ready or alert or message)) with ((access$3 or read$3 or retriev$3) near2 DRAM))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 11:04
S73	6	S68 and (((signal or flag or interrupt$4) near5 (ready or alert or message)) with ((access$3 or read$3 or retriev$3) near2 DRAM))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 11:05
S74	139	S69 and (((read$3 or retriev$3) near5 (request or command or intruction)) with DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 11:10
S75	9	S68 and (((signal or flag or interrupt$4) near5 (ready or alert or message)) near5 DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 11:11
S76	1112	DRAM near5 ready	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 11:13
S77	127	S68 and S76	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 11:14
S78	108	S71 and S77	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/04 11:14
S79	2	"20070288683".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/10/04 13:44

			DERWENT; IBM_TDB			
S80	10222	register near5 ((multiple or plurality or sequence) near2 (command or instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/05 18:16
S81	2040	register adj2 ((multiple or plurality or sequence) near2 (command or instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/05 18:17
S82	764	register adj2 ((sequence) near2 (command or instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/05 18:17
S83	93405	DRAM near5 ((flash or non$1volatile) adj (memory or storage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:07
S84	17112	S83 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:07
S85	17112	S84 and ((DRAM OR SDRAM) with (flash or non$1volatile))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:07
S86	764	register adj2 ((sequence) near2 (command or instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:09
S87	137	S86 and ((DRAM OR SDRAM) with (flash or non$1volatile))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:09
S88	73	concatenat$3 near5 (set near2 address$3)	US-PGPUB; USPAT; USOCR;	OR	ON	2019/10/06 11:12

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S89	0	S87 and S88	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:12
S90	0	S85 and S88	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:13
S91	33	S88 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:13
S92	3	S91 and (flash or non$volatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:14
S93	7592	concatenat$3 near5 (address$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:29
S94	55	S85 and S93	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:30
S95	55	S94 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/06 11:30
S96	93405	DRAM near5 ((flash or non$1volatile) adj (memory or storage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 10:05
S97	17112	S96 and (@ad<"20070601")	US-PGPUB;	OR	ON	2019/10/07

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			10:05
S98	17112	S97 and ((DRAM OR SDRAM) with (flash or non$1volatile))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 10:05
S99	7592	concatenat$3 near5 (address$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 10:05
S100	55	S98 and S99	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 10:05
S101	55	S100 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 10:05
S102	37	S101 and (address near2 bits)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 10:05
S103	0	S102 and (sequen$5 near2 command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 10:07
S104	37	S102 and (sequen$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 10:07
S105	93405	DRAM near5 ((flash or non$1volatile) adj (memory or storage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2019/10/07 12:04

			IBM_TDB			
S106	17112	S105 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:04
S107	17112	S106 and ((DRAM OR SDRAM) with (flash or non$1volatile))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:04
S108	7592	concatenat$3 near5 (address$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:04
S109	55	S107 and S108	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:04
S110	55	S109 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:04
S111	37	S110 and (address near2 bits)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:04
S112	37	S111 and (sequen$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:04
S113	6	S112 and (sequen$5 near2 address$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:04
S114	1516	S108 and (sequen$5 near2 address$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2019/10/07 12:33

			JPO; DERWENT; IBM_TDB			
S115	277	S114 and ((DRAM OR SDRAM) with (flash or non$1volatile))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:35
S116	121	S115 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:35
S117	119	S116 and (address near2 bits)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:36
S119	4	S117 and (sequen$5 near2 command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:37
S120	16	S115 and 711/$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:41
S121	5	S120 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:44
S122	1574	(transfer$3 or cop$4 or transmi$5 or retriev$3) near5 DRAM near5 (flash or non$1volatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:49
S123	0	S113 and S122	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:49
S124	54	S122 and (sequen$5 near2 address$3)	US-PGPUB; USPAT;	OR	ON	2019/10/07 12:52

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S125	16	S124 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/07 12:52
S126	20870	sequential$2 adj2 address	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 14:16
S127	875	(transfer$4 or read$3) adj10 data adj10 (non$1volatile or flash) adj10 (DRAM or SDRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 14:19
S129	32	S126 and S127	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 14:21
S130	15	S129 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 14:22
S131	5530	sequen$5 near5 receiv$3 near5 addresses	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 15:30
S132	875	(transfer$4 or read$3) adj10 data adj10 (non$1volatile or flash) adj10 (DRAM or SDRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 15:32
S133	2	S131 and S132	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 15:32

S134	102	S132 and (sequen$5 near5 addresses)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 15:35
S135	23	S134 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 15:35
S136	2	receiv$3 near5 (first near2 (address adj bits)) near5 (second near2 (address adj bits)) near5 (sequen$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 16:17
S137	34246	commands near2 register	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 16:35
S138	92	S137 and S132	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 16:36
S139	35	S138 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/08 16:36
S140	4807	commands near2 register	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/08 16:40
S141	22	S132 and S140	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/08 16:40
S142	4	S141 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/10/08 16:40

			DERWENT; IBM_TDB			

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Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (02-18)
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	15934416	Filing Date	2018-03-23	Docket Number (if applicable)	0016.001000G	Art Unit	2131
First Named Inventor	Hyun Lee			Examiner Name	FARROKH, HASHEM		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 602034

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (02-18)
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Signature of Registered U.S. Patent Practitioner			
Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2020-03-12
Name	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.	CONFIRMATION NO: 2728
SERIAL NO: 15/934,416	ART UNIT: 2131
FILING DATE: 3/23/18	EXAMINER: FARROKH, Hashem
TITLE: FLASH-DRAM HYBRID MEMORY MODULE	

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND/OR REPLY TO OFFICE ACTION

Commissioner:

In response to the Office Action mailed October 15, 2019, Applicant submits the following Amendment and Remarks.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page **2**.

Remarks begin on page **6**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2034.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Currently amended) A memory system, comprising:

a memory device including a first memory portion and a second memory portion; and

a controller coupled to a system memory controller of a host system and to the memory device, the controller is configured to transfer data information from the second memory portion to the first memory portion in response to a first command received by the controller from the system memory controller, the controller is further configured to alert the system memory controller when the data information is ready to be retrieved, and wherein the data information is retrieved from the ~~second~~ first memory portion in response to a second command received by the controller from the system memory controller.

3. (Previously presented) The memory system of claim 2, wherein the first memory portion includes volatile memory, and wherein the second memory portion includes non-volatile memory.

4. (Previously presented) The memory system of claim 2, wherein the first memory portion includes dynamic random access memory (DRAM), and wherein the second memory portion includes FLASH memory.

5. (Previously presented) The memory system of claim 2, wherein the first command received from the system memory controller corresponds to a memory read operation received from the system memory controller in accordance with a protocol.

6. (Previously presented) The memory system of claim 2, wherein the controller is coupled to the system memory controller of the host system via system address lines, wherein the controller is further configured to determine an address of the data information based on a first number of address bits and a second number of address bits, and wherein the controller is

configured to receive the first number of address bits and the second number of address bits sequentially over the system address lines.

7. (Previously presented) The memory system of claim 6, wherein the controller is configured to concatenate the first number of address bits and the second number of address bits to determine the address of the data information.

8. (Previously presented) The memory system of claim 7, wherein the first number of address bits is twelve.

9. (Previously presented) The memory system of claim 5, wherein the controller is further configured to receive the second command from the system memory controller according to the protocol.

10. (Previously presented) A memory module couplable to a system memory controller of a host system, the memory module comprising:

a controller operable to receive from the system memory controller a first memory access command via system address lines;

a non-volatile memory device; and

a volatile memory device;

wherein, in response to the first memory access command, the controller is configured to determine if data associated with the first memory access command is stored in the volatile memory device or the non-volatile memory device, and if the data associated with the first memory access command does not reside in the volatile memory device, the controller is further configured to perform a data transfer operation of the data associated with the first memory access command from the non-volatile memory device to the volatile memory device; wherein the controller is further configured to alert the system memory controller that the data associated with the first memory access command is ready to be retrieved from the volatile memory device; and wherein the data associated with the first memory access command is retrieved from the volatile memory device in response to a second memory access command received by the controller from the system memory controller.

11. (Previously presented) The memory module of claim 10, wherein the volatile memory device includes dynamic random access memory (DRAM), and wherein the volatile memory device includes FLASH memory.

12. (Previously presented) The memory module of claim 10, wherein the first memory access command received from the system memory controller corresponds to a memory read operation according to a protocol.

13. (Previously presented) The memory module of claim 12, wherein the first memory access command received from the system memory controller includes a first command RC(X) received from the system memory controller over the system address lines and a second command RC(X+1) received after the first command RC(X) from the system memory controller over the system address lines.

14. (Previously presented) The memory module of claim 13, wherein the first command RC(X) includes a first number of address bits, and wherein the second command RC(X+1) includes a second number of address bits in accordance with the protocol.

15. (Previously presented) The memory module of claim 14, wherein the controller is further configured to determine an address of the data associated with the first memory access command based on the first number of address bits and the second number of address bits.

16. (Previously presented) The memory module of claim 14, wherein the first number of address bits is equal to twelve.

17. (Previously presented) The memory module of claim 14, wherein the controller is further configured to concatenate the first number of address bits and the second number of address bits to determine an address of the data associated with the first memory access command.

18. (Previously presented) The memory module of claim 10, wherein the controller is further configured to receive the second memory access command according to the protocol.

19. (Previously presented) A memory module couplable to a system memory controller of a host system, comprising:

a controller operable to receive from the system memory controller a first memory access command, the first memory access command including a first address;

a non-volatile memory device;

a volatile memory device; and

a data manager coupled to the non-volatile memory device and the volatile memory device, the data manager configured to exchange data with the memory controller via a data interface in response to control information received from the controller;

wherein, in response to the first memory access command, the controller is configured to determine if data associated with the first address is stored in the volatile memory device or the non-volatile memory device;

wherein, if the data associated with the first address does not reside in the volatile memory device, the controller is configured to perform a data transfer operation from the non-volatile memory device to the volatile memory device by way of the data manager;

wherein the controller is further configured to alert the memory controller that the data associated with the first address is ready to be retrieved from the volatile memory device; and wherein the data associated with the first address is retrieved from the volatile memory device in response to a second memory access command received by the controller from the system memory controller.

20. (Previously presented) The memory module of claim 19, further comprising:

a register configured to register multiple commands or a sequence of commands.

21. (Previously presented) The memory module of claim 20, wherein the first memory access command correspond to a memory read operation.

REMARKS

Applicant has received and carefully reviewed the final Office Action of October 15, 2019. Applicant respectfully requests reconsideration in view of the following remarks.

Upon entry of the foregoing amendment, claims 2-21 are pending in this application, with claims 2, 10 and 19 being independent.

Objection to the Specification

The specification is objected to as allegedly failing to provide proper antecedent basis for the limitations from claims 7 and 17 of "concatenate the first number of address bits and the second number of address bits..."

Applicants respectfully traverse, directing the Examiner's attention to the provisional priority application no. 60/941,586, whose contents are incorporated herein by reference. In the bullet points on page 6 of said provisional, the disclosed arrangement is described as extending addressable memory space by using "concatenated RAS commands" and "concatenated RAS and 1st CAS commands." Such description provides proper antecedent basis for the limitations of claims 7 and 17 and the objection of in the Office Action should be withdrawn.

Rejection(s) Under 35 U.S.C. § 112, First Paragraph

Claims 6-8, 13-17, and 21 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement.

The Office Action alleges that the specification fails to describe or support the limitation from claims 6 "receive the first set of address bits and the second set or address bits sequentially over the system address lines." For support for this feature, Applicant respectfully directs the Examiner's attention to the explanation, in column 16 and FIG. 10, of the mapping of the DRAM address space to Flash memory address space. The Flash target address as received by the CDC

502 from the host memory controller is written into the RC register.[1] In the RC register, the address is in the form of two sets of address bits 1002 and 1004 that are depicted in FIG. 10 to be in sequence ("RX(X)" and "RC(X+1)," emphasis added).

The Office Action alleges that the specification fails to describe or support the limitations from claims 7 "wherein the controller is further configured to concatenate the first set of address bits and the second set of address bits to determine the address of the data information" and the limitation from claim 17 "wherein the controller is further configured to concatenate the first number of address bits and the second number of address bits to determine an address of the data information associated with the first memory command." As explained above, the provisional priority application no. 60/941,586, whose contents are incorporated herein by reference, discloses this feature in the bullet points on page 6 for example, explaining that the disclosed arrangement is capable of extending addressable memory space by using "concatenated RAS commands" and "concatenated RAS and 1st CAS commands." Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 7 and 17 under 35 U.S.C. § 112, first paragraph.

The Office Action alleges that the specification fails to describe or support the limitation from claims 13 "wherein the first memory command includes a first command RC(X) received from the system memory controller over the set of system address and control lines and a second command RC(X+1) received after the first command RC(X) from the system memory controller over the set of system address and control lines." Applicant respectfully directs the Examiner's attention to the discussion of the register 690, which is described as registering "commands received from MCH [memory controller] 510 via C/A [control/address] 560,"[2] and as having the "the ability to register multiple commands, a sequence of commands, or provide a pipeline delay stage for buffering and providing a controlled execution of certain commands received from MCH 510."[3] Further, as explained above, in the register, the address is in the form of two sets of

[1] Paragraph [0098], ll. 2-4, "the memory controller initiates, at step 906, a data move from the Flash 506 to the DRAM 508 by writing target address and size, to a control register in the CDC 502…"; Paragraph [0099], ll. 2-4, "At any time the CDC 502 receives a DRAM load command from a memory controller which writes a Flash target address and/or block size information into the RC register(s) at 922."
[2] Paragraph [0088], ll. 1-2.
[3] *Id.*, ll. 5-7.

address bits 1002 and 1004, depicted in FIG. 10, that are received from the host memory controller (MCH) and stored in sequential registers RX(X) and RC(X+1).

The Office Action alleges that the specification fails to describe or support the limitation from claims 15 "wherein the controller is further configured to determine an address of the data information associated with the first memory command based on the first number of address bits and the second number of address bits." Applicant respectfully directs the Examiner's attention to the explanation of operation of the controller (CDC 502) in Paragraph [0099], wherein it is stated that "The CDC 502 monitors all memory access commands sent by the memory controller using standard DRAM protocol and appropriately configures and manipulates both Flash 506 and DRAM 508 memory subsystems to perform the requested memory access operation."[4] The first and second numbers of address bits can correspond to the two sets of address bits 1002 and 1004 that are depicted in FIG. 10 as explained above.

The Office Action alleges that the specification fails to describe or support the limitation from claims 21 "wherein the second command is received by the controller after the first command is received by the controller, and wherein the controller is configured to determine an address of the data information associated with the first memory command using the first set of address bits and the second set of address bits." As explained above, register 690 is described as having the "the ability to register multiple commands, a sequence of commands, or provide a pipeline delay stage for buffering and providing a controlled execution of certain commands received from MCH 510."[5] (Emphasis added) Further, in Paragraph [0099], it is stated that "The CDC 502 monitors all memory access commands sent by the memory controller using standard DRAM protocol and appropriately configures and manipulates both Flash 506 and DRAM 508 memory subsystems to perform the requested memory access operation." And finally, in the register, the address is in the form of two sets of address bits 1002 and 1004, depicted in FIG. 10, that are received from the host memory controller (MCH) and stored in sequential registers RX(X) and RC(X+1).

[4] Paragraph [0099], ll. 7-11.
[5] Paragraph [0088], ll. 5-7.

It is respectfully submitted that claims *** are now in compliance with 35 U.S.C. § 112, first paragraph, and the rejection thereunder should be withdrawn.

Rejection(s) Under 35 U.S.C. § 103(a)

Claims 2-5, 9-12, and 18-19 stand rejected under pre-A/A 35 U.S.C. 102 (a)(2) as anticipated by or, in the alternative, under pre-A/A 35 U.S.C. 103(a) as obvious over Fukuzo "Fukuzo" (US 2006/0294295 A 1).

Applicants respectfully traverse.

Independent claims 2, 10 and 19, from which the remaining rejected claims variously directly or indirectly depend, recite, for example according to claim 2, "the controller is further configured to alert the system memory controller when the data information is ready to be retrieved." Addressing this feature, the Office Action refers to the ready or busy signals described in ¶ [0028] of Fukuzo.[6] However, ¶ [0028] explains that the ready or busy signals are for use by the host system "**when writing** to the SDRAM array, the FIFO array or the non-volatile memory, respectively."[7] (Emphasis added) By comparison, the claim 1 alerts relate to retrieval (e.g. reading) of data information from. Thus Fukuzo, and specifically ¶ [0028], does not disclose "the controller is further configured to alert the system memory controller when the data information is ready to be retrieved" as presently claimed.

Independent claims 2, 10 and 19 also recite, for example according to claim 2, "the data information is retrieved from the first memory portion in response to a second command received by the controller from the system memory controller." Addressing this feature, the Office Action refers to ¶¶ [0104] and [0127] of Fukuzo, and to alleged "commands issued by or in response to the commands issued by CPU 50."[8] However, neither in these passages, nor anywhere else, does Fukuzo make a distinction between first and second commands received by the controller from the system memory controller; nor does Fukuzo disclose retrieval of data

[6] Office Action, p. 6, l. 17.
[7] Fukuzo, ¶ [0028], last sentence.
[8] Office Action, p. 6, ll. 20-21.

information from the first memory portion "in response to a second command received by the controller from the system memory controller" as presently claimed. Reproduced in their entirety, ¶¶ [0104] and [0127] state:

> **[0104]** These three latter commands CP, BU and DAS are performed automatically, i.e., not as a background operation, directly in response to the command signals issued by the CPU. However, commands /LD and /ST are background operations. Accordingly, the duration of the performance is not previously known and further signals FIFO and FLASH with respective flag signal pins are needed as described below in order to provide a feedback to the CPU 50 of what is currently the status in the background (between FIFO buffer memory section 20, flash controller section 30 and flash memory device 60).

> **[0127]** FIG. 5 provides an overview of the load, store, read and write commands available according to this embodiment of the invention. Command signals /LD and /ST are background operations (on the second data transfer bus) controlled by flash controller 320 and timing generator 211, BU (back-up) and CP (copy) are automatic foreground operations (on the first data transfer bus) directly initiated by the CPU 50 and controlled by SDRAM/FIFO control logic 120. Write and read commands (WR, RD) can be performed alternatively on both the SDRAM core array 190 and the SDRAM FIFO memory array 290 by the CPU 50.

A close reading of these passages reveals that ¶ [0104] is primarily concerned with the signaling to the CPU of the status of automatic vs. background operations; while ¶ [0127] merely explains that write and read commands can be performed on the SDRAM and FIFO arrays, without providing details on the sequence of events involved in such write/read commands, and certainly without disclosing that "data information is retrieved from the first memory portion **in response to a second command** received by the controller from the system memory controller" as presently claimed.

For these reasons at least, Applicant respectfully maintains that the invention as claimed is neither anticipated or rendered obvious by Fukuzo, and the rejection(s) under 35 U.S.C. §§ 102 and/or 103 based on this reference should be withdrawn.

Conclusion

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 60-2034.

Respectfully submitted,

Dated: March 12, 2020

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
202-516-6900

PTO/AIA/22 (03-13)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)	Docket Number (Optional) 0016.001000G
Application Number 15/934,416	Filed 03-23-2018
For FLASH-DRAM HYBRID MEMORY MODULE	
Art Unit 2131	Examiner FARROKH, HASHEM

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	$200	$100	$50	$
☑ Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$ 600.00
☐ Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
☐ Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐ Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☑ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 60-2034.

☐ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 38,745.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Khaled Shami/	March 12, 2020
Signature	Date
Khaled Shami	202-516-6900
Typed or printed name	Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	15934416
Filing Date:	23-Mar-2018
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Marianne Forrest
Attorney Docket Number:	0016.001000G

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	600	600
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
		Total in USD ($)		**1900**

Electronic Acknowledgement Receipt

EFS ID:	38846325
Application Number:	15934416
International Application Number:	
Confirmation Number:	2728
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Marianne Forrest
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000G
Receipt Date:	12-MAR-2020
Filing Date:	23-MAR-2018
Time Stamp:	14:06:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1900
RAM confirmation Number	E20203BE07022050
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	0016_001000G_RCE_sb0030efs.pdf	1349915 0c2a2d769917a507f3ea6ba6bc113da6f950d22f	no	3
Warnings:					
Information:					
2		0016_001000G_reply.pdf	138992 d363de1afff1eb7819d8f6f03e92423a2357f73a	yes	12

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment Submitted/Entered with Filing of CPA/RCE	1	1
Claims	2	5
Applicant Arguments/Remarks Made in an Amendment	6	12

Warnings:					
Information:					
3	Extension of Time	0016_001000G_EOT_aia0022.pdf	158292 322e2fcd66ee54b678cd7b41fa7dc082c8925a8c	no	2
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	32383 fa959a3c088e1b26304ed24ec2cdcdb3b3ead600	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1679582		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/934,416	Filing Date 03/23/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	03/12/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/LAVINIA D JOHNSON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/934,416	Filing Date 03/23/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	03/12/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/LAVINIA D JOHNSON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/934,416	03/23/2018	Hyun Lee	0016.001000G	2728

151145 7590 04/02/2020

Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2131	

NOTIFICATION DATE	DELIVERY MODE
04/02/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

khaled@shamimessinger.com
mike@shamimessinger.com
stephanie@shamimessinger.com

Office Action Summary	Application No. 15/934,416	Applicant(s) Lee et al.	
	Examiner HASHEM FARROKH	Art Unit 2131	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 03/12/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 2-21 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 2-21 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 03/23/2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/12/2020 has been entered.

This office action is in response to the communication(s) filed on 03/12/2020. There are a total 20 claims pending in the application; claim 1 has been canceled, claim 2 has been amended, and no new claims have been added.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by*

M.P.E.P. 707.05 *and* ***904*** *and as stated in* ***M.P.E.P. 2001.06(b),*** *no separate citation of the same prior art need be made by the applicants in the instant application.*

INFORMATION CONCERNING SPECIFICATION:

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

1. Claims 7 and 17 recite"

"…**concatenate** the first set of address bits and the second set address bits…"

(Emphasis added).

The specification fails to provide proper antecedent basis for the above limitation.

INFORMATION CONCERNING CLAIMS:

EXAMINER'S NOTE

It appears that Applicant inadvertently has included the list of claims filed 07/22/2019 instead of the most recent amended version of claims filed on 08/26/2019. If this is the case, it is suggested that Applicant amend the claims to most recent and claims indicator, indicates the change (e.g., "Currently amended").

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> *(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.*

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> *The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

Claims 6-8, 13-17, and 21 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

2. Claim 6 recites, in part, the limitation:

"c) "receive the first set of address bits and the second set of address bits sequentially over the system address lines."

The claimed specification does not describe or support the above limitation as claimed. Claims 7-8 are rejected by virtue of their dependency from claim 6.

3. Claim 7 recites the limitation:

"wherein the controller is further configured to concatenate the first set of address bits and the second set of address bits to determine the address of the data information."

The claimed specification does not describe or support the above limitation as claimed. Claim 8 is rejected by virtue of its dependency from claim 7.

4. *Claim 13 recites the limitation:*

"wherein the first memory command includes a first command RC(X) receive from the system memory controller over the set of system address and control lines and a second command RC(X+1) received after the first command RC(X) from the system memory controller over the set of system address and control lines."

The claimed specification does not describe or support the above limitation as claimed. Claims 14-17 are rejected at least by virtue of their dependency from claim 13.

5. *Claim 15 recites the limitation:*

"wherein the controller is further configured to determine an address of the data information associated with the first memory command based on the first number of address bits and the second number of address bits."

The claimed specification does not describe or support the above limitation as claimed.

6. *Claim 17 recites the limitation:*

"wherein the controller is further configured to concatenate the first number of address bits and the second number of address bits to determine an address of the data information associated with the first memory command."

The claimed specification does not describe or support the above limitation as claimed.

7. *Claim 21 recites, in part, the limitation:*

"wherein the second command is received by the controller after the first command is received by the controller, and wherein the controller is configured to determine an address of the data information associated with the first memory command using the first set of address bits and the second set of address bits."

The claimed specification does not describe or support the above limitation as claimed.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negative by the manner in which the invention was made.*

Claims 2-5, 9-12, and 18-19 are rejected under pre-AIA 35 U.S.C. 102 (a)(2) as anticipated by or, in the alternative, under pre-AIA 35 U.S.C. 103(a) as obvious over Fukuzo "Fukuzo" (US 2006/0294295 A1).

8. In regard to claim 2 Fukuzo teaches:

"A memory system **(e.g., Fig. 3)**, comprising:

"a memory subsystem including a first memory portion **(e.g., ¶ 0080, SDRAM memory chip device 40 in Fig. 3)** and a second memory portion;" **(e.g., ¶ 0080, Flash memory device 60 in Fig. 3).**

"and a controller configured to be coupled to a system memory controller **(e.g., ¶ 0082, CPU 50 of the host system in Fig. 3)** of a host system and to the memory sub system **(e.g., ¶¶ 0081-0082; chip device 40 in Fig. 3 in addition to SDRAM array 190, comprises section 10, 20, and 30 that include controller and/or control logic that coupled system memory and host system such as processor 50 in Fig. 3)**, the controller operable to transfer data information from the second memory portion to the first memory portion in response to a first command received by the controller from the system memory controller **(e.g., ¶¶ 0086-0088; Figs. 3-4)**, the controller further operable to alert the system memory controller when the data information is ready to be retrieved," **(e.g., ¶ 0028; ¶ 0106; ¶ 0126, During this operation, the /FIFO flag is also issued in order to signal to the CPU 50 that the FIFO memory buffer is busy. As a result of that, the CPU 50 is not allowed to store or load data to/from the FIFO memory buffer array 290 until the /FIFO flag returns to the level "high")**.

"and wherein the data information is retrieved from the first memory portion in response to a second command received by the controller from the system memory controller." **(e.g., ¶ 0104, ¶ 0107, ¶ 0127; Figs. 3-5; commands issued by or in response to the commands issued by CPU 50).**

9. In regard to claim 10 Fukuzo teaches:

"A memory module couplable to a system memory controller of a host system **(e.g., CPU 50 IN Fig. 3)** via a set of data lines and a set of address and control lines **(e.g., ¶¶ 0080-0083; Fig. 3)**, the memory module comprising:"

"a controller operable to receive from the system memory controller a first memory command via the set of system address and control lines;" **(e.g., ¶¶ 0080-0083, ¶ 0088; Fig. 3).**

"a non-volatile memory device;" **(e.g., ¶ 0080; flash memory device 60 in Fig. 3).**

"and a volatile memory device;" **(e.g., ¶ 0080; SDRAM memory device 40 in Fig. 3).**

"wherein, in response to the first memory command, the controller is configured to:

a) perform a data transfer operation from the non-volatile memory device to the volatile memory device if data information associated with the first memory command does not

reside in the volatile memory device," **(e.g., ¶ 0088; Fig. 3).**

b) *and* alert the system memory controller when the data information associated with the first memory command is ready to be retrieved from the volatile memory device;" **(e.g., ¶ 0106; ¶ 0126, During this operation, the /FIFO flag is also issued in order to signal to the CPU 50 that the FIFO memory buffer is busy.**

As a result of that, the CPU 50 is not allowed to store or load data to/from the FIFO memory buffer array 290 until the /FIFO flag returns to the level "high").

"and wherein the data information associated with the first memory retrieved from the volatile memory device in response to a second memory received by the controller from the system memory controller." **(e.g., ¶ 0107; Figs. 3-4).**

10. In regard to claim 19 Fukuzo teaches:

"A memory module couplable to a system memory controller of a host system via a set of data lines and a set of system address and control lines **(e.g., ¶¶ 0080-0083; Fig. 3)**, the memory module comprising:"

"a controller operable to receive from the system memory controller a first memory command via the set of system address and control lines;" **(e.g., ¶¶ 0080-0083, ¶ 0088; Fig. 3).**

"a non-volatile memory device;" **(e.g., ¶ 0080; flash memory device 60 in Fig. 3).**

"a volatile memory device;" **(e.g., ¶ 0080; SDRAM memory device 40 in Fig. 3).**

"and a data manager coupled to the system memory controller **(e.g., CPU 50 IN Fig. 3)**, the non-volatile memory device and the volatile memory device **(e.g., SDRAM 40 comprises controller or data manger to control data transfer or exchange between CPU 50 and Flash memory 60 in Fig. 3)** , wherein the data manager is configured to exchange data with one or more of the non-volatile memory device, the

volatile memory device, and the system memory controller in response to control information received from the controller;" **(e.g., ¶¶ 0080-0083, ¶ 0088; Fig. 3; Figs. 3-4 and the corresponding text description).**

"wherein, in response to the first memory command, the controller is configured to:

a) perform a data transfer operation from the non-volatile memory device to the volatile memory device by way of the data manager if data information associated with the first memory command does not reside in the volatile memory devices;" **e.g., ¶ 0088; Fig. 3).**

b) and alert the system memory controller that when the data associated with the first memory command is ready to be retrieved from the volatile memory device;" **(e.g., ¶ 0106; ¶ 0126, During this operation, the /FIFO flag is also issued in order to signal to the CPU 50 that the FIFO memory buffer is busy. As a result of that, the CPU 50 is not allowed to store or load data to/from the FIFO memory buffer array 290 until the /FIFO flag returns to the level "high").**

"and wherein the data associated with the first memory command is retrieved from the volatile memory device in response to a second memory command received by the controller from the system memory controller." **(e.g., ¶ 0107).**

11. In regard to claim 3 Fukuzo further teaches:

"wherein the first memory portion includes volatile memory **(e.g., SDRAM 40)** and the second memory portion includes non-volatile memory." **(e.g., ¶ 0080; Fig. 3; Flash memory 60).**

12. In regard to claims 4 and 11 Fukuzo further teaches:

"wherein the first memory portion includes dynamic random access memory (DRAM) and the second memory portion includes FLASH memory." **(e.g., ¶ 0080; Fig. 3).**

13. In regard to claims 5 and 12 Fukuzo further teaches:

"wherein the first command received from the system memory controller corresponds to a memory read operation received from the system memory controller in accordance with a protocol." **(e.g., ¶ 0024; a standard set of commands for the NAND-flash controller).**

14. In regard to claims 9 and 18 Fukuzo further teaches:

"wherein the controller is further configured to receive the second command from the system memory controller according to the protocol." **(e.g., ¶ 0082; SDRAM standard).**

Claim 20 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Fukuzo in view of Shiota et al "Shiota" (US 2003/0147297 A1).

15. In regard to claim 20 Fukuzo discloses all limitations include in claim 19 but does not expressly teach while Shiota teaches:

"a register configured to register multiple commands or a sequence of commands." **(e.g., ¶ 0042)** a register for storing read and write commands.

Disclosures by Fukuzo and Shiota are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the DRAM chip device taught by Fukuzo to include the command register disclosed by Shiota.

The motivation for including the command register as taught by paragraph [0005] of Shiota is to provide a memory system contributing improvement in efficiency of a data process accompanying a memory access.

Therefore, it would have been obvious to combine teaching of Shiota with Fukuzo to obtain the invention as specified in the claim.

Response to Remarks

Applicant arguments have been fully considered but they are not persuasive.

In regard to objection to the claimed specification as not providing proper antecedent basis for limitation recited in claims 7 and 17, Applicant argues:

"Applicants respectfully traverse, directing the Examiner's attention to **the provisional priority application no. 60/941,586, whose contents are incorporated herein by reference**. In the bullet points on page 6 of said provisional, the disclosed arrangement is described as extending addressable memory space by using "**concatenated RAS commands" and "concatenated RAS and 1st CAS commands." Such description**

provides proper antecedent basis for the limitations of claims 7 and 17 and the objection of in the Office Action should be withdrawn." *(Page 6 of the Remarks, emphasis added).*

Claim 7 recites:

"wherein the controller is configured to **concatenate** the first number of address bits and the second number of address bits to determine the address of the data information." *(Emphasis added).*

However, the Remarks fails to describe as to how by concatenating RAS and 1ST CAS command, Concatenates the first number of address bits and the second number of address bits. One having ordinary skill in the art understands that RAS (e.g., Row Address Strobe) and CAS (e.g., Column Address Strobe) commands are strobe signals that are used to strobe (e.g., latch) the row address and column address, respectfully. They are normally used as timing signals to strobe or latch row and column addresses. The concatenated RAS commands" and "concatenated RAS and 1st CAS commands, does not "concatenate the first number of address bits and the second number of address bits to determine the address of the data information" *as claimed. Claim 17 recites a similar limitation.*

Claim 6 has been rejected under 35 USC § 112(a), first paragraph as failing to comply with the written description requirement.

Claim 6 recites, in part, the limitation:

"...wherein controller is configured to **receive the first number of address bits and the second number of address bits sequentially over the system address lines.**" *(Emphasis added).*

On pages 6-7 of the Remarks, Applicant states that column 16 and Fig. 10 of the claimed specification describes or supports the above limitations. The Examiner respectfully disagrees. Fig. 10 shows mapping DRAM address to flash memory address. It shows extended page memory address including two 12 bits sets of addresses stored in two registers RC(X) and RC (X+1), for example two adjacent registers. There is nothing in the specification related to Fig. 10 that describes or indicates the limitation: the controller configured to receive the first number of address bits and the second number of address bits sequentially over the system address lines as claimed.

Claims 7 and 17 have been rejected under 35 USC § 112(a), first paragraph as failing to comply with the written description requirement.

The Examiner respectfully submits that specification does not describe or support the limitations as claimed. The Examiner response is the same as response to the arguments regarding the antecedent basis described above.

Claim 13 has been rejected under 35 USC § 112(a), first paragraph as failing to comply with the written description requirement.

Claim 13 recites the limitation:

"wherein the first memory access command received from the system memory controller includes a **first command RC(X)** received from the system memory controller over the system address lines and a **second command RC(X+1)** received after the first command RC(X) from the system memory controller over the system address lines." *(Emphasis added).*

Regarding this rejection, pages 7-8 of the Remarks recite:

"The Office Action alleges that the specification fails to describe or support the limitation from claims 13 "wherein the first memory command includes a **first command RC(X)** received from the system memory controller over the set of system address and control lines and a second **command RC(X+1)** received after the first command RC(X) from the system memory

controller over the set of system address and control lines." Applicant respectfully directs the Examiner's attention to the discussion of the **register 690, which is described as registering "commands received from MCH [memory controller] 510 via C/A [control/address] 560,"[2] and as having the "the ability to register multiple commands, a sequence of commands, or provide a pipeline delay stage for buffering and providing a controlled execution of certain commands received from MCH 510.**"[3] Further, as explained above, in the register, the address is in the form of two sets of address bits 1002 and 1004, depicted in FIG. 10, that are received from the host memory controller (MCH) and stored in sequential registers RX(X) and RC(X+1)." *(Emphasis added).*

The Examiner respectfully submits that there is nothing related to the discussion of the register 690 or any other portion(s) of the claimed specification that describe a ***first command RC(X)*** *received from the system memory controller over the set of system address and control lines and a* ***second command RC(X+1)*** *received after the first command RC(X) from the system memory controller over the set of system address and control lines. As previously discussed two registers RC(X) and RC (X+1) are two registers for storing two 12-bits addresses for mapping DDR DIMM page address to flash memory (see Fig. 10).*

Claim 15 has been rejected under 35 USC § 112(a), first paragraph ***as failing to comply with the written description requirement.***

Claim 15 recites the limitation:

"wherein the controller is further **configured to determine an address of the data associated with the first memory access command based on the first number of address bits and the second number of address bits**." *(Emphasis added).*

Applicant states paragraph [0099] of the claimed specification describes the limitation. For convenient, paragraph [0099] of the specification as originally filed is reproduced as shown below:

"[0099] The dashed lines in FIG. 9 indicate independent or parallel activities that can be performed by the CDC 502. At any time the CDC 502 receives a DRAM load command from a memory controller which writes a Flash target address and/or block size information into the RC register(s) at 922, as described above, then the CDC 502 executes a load DRAM w/RC step 906 and initiates another branch (or a thread) of activities that includes steps 908-922. In one embodiment, the CDC 502 controls the data transfer operations between DRAM 508 and Flash 506 such that the Flash 506 is completely hidden from the memory controller. The CDC 502 monitors all memory access commands sent by the memory controller using standard DRAM protocol and appropriately configures and manipulate both Flash 506 and DRAM 508 memory subsystems to perform the requested memory access operation and thus achieve the desired results. The memory controller does not interface directly with the Flash memory subsystem. Instead, the memory controller interfaces with the CDC 502 and/or DMgr 504 as shown in FIG. 5 and FIG. 6. Moreover, the memory controller may use one or more protocol, such as DDR, DDR2, DDR3, DDR4 protocols or the like."

*There is nothing in paragraph [0099] that describes or supports the limitation: "*determine an address of the data associated with the first memory access command based on the first number of address bits and the second number of address bits*" as claimed.*

Claim 21 has been rejected under 35 USC § 112(a), first paragraph as failing to comply with the written description requirement.

Claim 21 recites the limitation:

"wherein the second command is received by the controller after the first command is received by the controller, and wherein the controller is configured to **determine an address of the data information associated with the first memory command using the first set of address bits and the second set of address bits.**" *(Emphasis added).*

*Page 8 of the Remarks states that register 690 and paragraph [0099] of the claimed specification describes the limitation. As previously described register 690, paragraph [0099], or any other portion(s) of the claimed specification does not describe: "*determine

an address of the data information associated with the first memory command using the first set of address bits and the second set of address bits", *as claimed.*

In regard to the prior rejection, on page 9 of the Remarks, Applicant states paragraph [0028] of Fukuzo discloses that ready/busy warning signal is used only for write operation but alert recited in claim 2 is related to retrieving (e.g., reading operation). The Examiner respectfully submits that Fukuzo discloses to additional status signals /FIFO and /FLAS. Based on status these signals, CPU determines whether or not to access the memory system. For example, paragraph [0126] discloses that CPU checks the /FIFO signal to determine whether CPU 50 allowed to store or load (e.g., retrieve) data.

Pages 9-10 of the Remarks states:

"Independent claims 2, 10 and 19 also recite, for example according to claim 2, "**the data information is retrieved from the first memory portion in response to a second command received by the controller from the system memory controller**." Addressing this feature, the Office Action refers to ¶¶ [0104] and [0127] of Fukuzo, and to alleged "commands issued by or in response to the commands issued by CPU 50."[8] However, **neither in these passages, nor anywhere else, does Fukuzo make a distinction between first and second commands received by the controller from the system memory controller**; nor does Fukuzo **disclose retrieval of data information from the first memory portion "in response to a second command received by the controller from the system memory controller**" *(Emphasis added).*

The Examiner respectfully disagrees. First the claimed specifications does not expressly recite a second command (it recites a plurality of commands). Paragraphs [0082], [0107] and [0109] of Fukuzo are reproduced as shown below:

"[0082] The SDRAM core section 10 comprises an interface 12 to a host system such as a central processing unit 50 (CPU). The interface 12 comprises a plurality of pins 14, which are arranged to adhere to the SDRAM standard. According to their functions, the pins may be grouped into those transferring clock signals, address signals, command signals,

bank select signals and data signals. As indicated in FIG. 3 by the double arrows, additional pins are provided to the interface as compared with the SDRAM standard. **These additional pins are arranged to transmit signals, which yield control of background store and load operations with respect to those data intended for permanent storage within the NAND-flash memory, while data are transferred between the host CPU 50 and the SDRAM array 190**."

"[0107] SDRAM core section 10 further comprises--according to this embodiment--a mode register 140 and a bank select component 130. **The bank select component** 130 buffers the bank select signal incoming at a respective pin of **the first interface 12**. Using this signal, **one of the banks 0-3 of the array 190 may be selected for read or write access in agreement with the SDRAM standard**. In addition to the bank select pin (pin definition: BSL), a further pin may optionally be provided to select a bank of the FIFO memory buffer array 290, if this is array 290 as well arranged in terms of banks according to the SDRAM standard. In FIG. 4, a pin definition FBS (FIFO buffer select) is associated with this signal." *(Emphasis added).*

"[0109] A background load operation in accordance with this embodiment may be performed as follows: An /LD command (background load command) is issued (e.g., with /CS and /LD being "low" and /RAS, /CAS, /WE, /ST and CKE being "high") with a source address "SA" of a NAND-flash memory page provided via the address pins ADD by the CPU 50. SA relates to the page of the NAND memory to be loaded into the FIFO buffer section." *(Emphasis added).*

The Examiner respectfully submits that Fukuzo teaches or render obvious all limitations recited in the independent claim 2. The independent claims 10 and 19 recite similar limitations and thus Examiner response to the arguments regarding the independent claim 2 would apply. Accordingly, Examiner maintains his position.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, ***THIS ACTION IS MADE FINAL****. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ann Lo can be reached on (571)272-9767. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/

Primary Examiner, Art Unit 2131

Saturday, March 28, 2020

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/934,416	Lee et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2131

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/17/2019	10/09/2019	03/28/2020						
	1	✓	-	-						
	2		✓	✓						
	3		✓	✓						
	4		✓	✓						
	5		✓	✓						
	6		✓	✓						
	7		✓	✓						
	8		✓	✓						
	9		✓	✓						
	10		✓	✓						
	11		✓	✓						
	12		✓	✓						
	13		✓	✓						
	14		✓	✓						
	15		✓	✓						
	16		✓	✓						
	17		✓	✓						
	18		✓	✓						
	19		✓	✓						
	20		✓	✓						
	21		✓	✓						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/934,416	Lee et al.
	Examiner	Art Unit
	HASHEM FARROKH	2131

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F13/1694; G06F12/0246; G06F13/28; G06F13/4243; G06F2212/7208; G06F3/0685; G06F12/0638; G06F13/4027; G06F1/185; G06F2212/205; G06F3/0613; G06F3/0659; G11C7/1072; G11C14/0018	03/17/2019	HF
G06F12/0246; G06F3/0685; G06F12/0638; G06F13/28; G06F2212/7208; G06F3/0613; G06F3/0659; G11C7/1072	10/09/2019	HF
G06F12/0246; G06F3/0685; G06F13/1694; G06F2212/205; G06F3/0659; G06F13/28; G06F2212/7208; G06F3/0613; G06F12/0638; G06F1/185; G11C14/0018; G11C7/1072	03/28/2020	HF

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	110	03/17/2019	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

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	15/934,416	Lee et al.
	Examiner	Art Unit
	HASHEM FARROKH	2131

Search Notes		
Search Notes	**Date**	**Examiner**
PALM and Inventor Search	03/16/2019	HF
EAST Text Search	03/16/2019	HF
Google Search	03/17/2019	HF
PALM and Inventor Search Updated	10/09/2019	HF
EAST Text Search Updated	10/09/2019	HF
PALM and Inventor Search Updated	03/28/2020	HF
EAST Text Search Updated	03/27/2020	HF

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
711	110	03/28/2020	HF

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	141	((transfer$3 or cop$4 or transmi$5 or retriev$3 or read$3) near5 DRAM near5 (flash or non$1volatile)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 19:54
L2	1277	Lee-Hyun.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 19:54
L3	72	Chen-Chi-She.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 19:54
L4	72	Solomon-Jeffrey-C.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 19:54
L5	33	Milton-Scott-H.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 19:54
L6	36	Bhakta-Jayesh.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 19:54
L7	0	L1 and (L2 or L3 or L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 19:54
L9	2952	(transfer$4 with data with (non$volatile	US-PGPUB;	OR	ON	2020/03/28

		or flash) with (volatile or DRAM or SDRAM or DDR)).CLM.	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			19:59
L11	22	L9 and (L2 or L3 or L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 20:00
L12	10688	((transfer$3 or cop$4 or transmi$5 or retriev$3 or read$3) near5 DRAM near5 (flash or non$1volatile))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 20:07
L13	5804	L12 AND ((G06F12/0246 OR G06F3/0685 OR G06F12/0638 OR G06F13/28 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G11C7/1072).CPC. OR (1/1 OR 711/110).CCLS. OR (G06F3/06 OR G06F12/02 OR G06F13/42 OR G06F12/06 OR G06F13/28 OR G06F13/40 OR G06F1/18 OR G11C7/10).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 20:07
L14	236	(map$4 or translat$3 or conver$4) near5 ((DRAM or SDRAM or DDR) near5 address$3) with ((flash or non$volatile or NVM or NVRAM) near5 address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 20:23
L15	123	12 and 14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 20:24
L16	113	15 AND ((G06F12/0246 OR G06F3/0685 OR G06F13/1694 OR G06F2212/205 OR G06F3/0659 OR G06F13/28 OR G06F2212/7208 OR G06F3/0613 OR G06F12/0638 OR G06F1/185 OR G11C14/0018 OR G11C7/1072).CPC. OR (711/110 OR 711/103).CCLS. OR (G06F12/02 OR G06F3/06 OR G06F13/16 OR G06F13/28 OR G06F12/06 OR G06F13/40 OR G06F13/42 OR G06F1/18 OR G11C14/00 OR G11C7/10).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/28 20:39
S160	2	"20030147297".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/27 15:02

S161	2	(map$4 or translat$3 or conver$4) with ((sequen$4 or adjacent) near5 ((DRAM or SDRAM or DDR) near5 address$3)) with ((flash or non$volatile or NVM or NVRAM) near5 address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/27 17:06
S162	2	(map$4 or translat$3 or conver$4 or concatenat$3 or merg$3 or combin$3) with ((sequen$4 or adjacent) near5 ((DRAM or SDRAM or DDR) near5 address$3)) with ((flash or non$volatile or NVM or NVRAM) near5 address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/27 17:08
S163	183	(map$4 or translat$3 or conver$4 or concatenat$3 or merg$3 or combin$3) with ((sequen$4 or adjacent) near5 address$3) with ((flash or non$volatile or NVM or NVRAM) near5 address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/27 17:10
S164	46	S163 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/27 17:11
S165	19	S164 and (sequen$5 near5 (command or instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/27 17:11

3/28/2020 8:41:23 PM
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PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15934416
Filing Date	2018-03-23
First Named Inventor	Hyun Lee
Art Unit	2131
Examiner Name	Hashem FARROKH
Attorney Docket Number	0016.001000G

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	2	3562555	A	1971-02-09	Ahrons	
	3	3916390	A	1975-10-28	Chang et al.	
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	43	6691209	B1	2004-02-10	O'connell	
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	49	6810513	B1	2004-10-26	Vest	
	50	6816982	B2	2004-11-09	Ravid	
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	Examiner Name	Hashem FARROKH
	Attorney Docket Number	0016.001000G

	86	8904098	B2	2014-12-02	Amidi et al.	
	87	8904099	B2	2014-12-02	Chen et al.	
	88	9043677	B2	2015-05-26	Kong et al.	
	89	9158684	B2	2015-10-13	Lee et al.	
	90	9361250	B2	2016-06-07	Shan et al.	
	91	9436600	B2	2016-09-06	Lee	Entire Document
	92	9921762	B2	2018-03-20	Amidi et al.	Entire Document
	93	9928186	B2	2018-03-27	Lee et al.	Entire Document

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20130086309	A1	2013-04-04	Lee et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15934416
	Filing Date	2018-03-23
	First Named Inventor	Hyun Lee
	Art Unit	2131
	Examiner Name	Hashem FARROKH
	Attorney Docket Number	0016.001000G

	2	20130254456	A1	2013-09-26	Chen et al.	
	3	20130254497	A1	2013-09-26	Chen et al.	
	4	20140032820	A1	2014-01-30	Harasawa et al.	
	5	20140059170	A1	2014-02-27	Gasparakis et al.	
	6	20140156919	A1	2014-06-05	Chen et al.	
	7	20140156920	A1	2014-06-05	Chen et al.	
	8	20150058701	A1	2015-02-26	Xing et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15934416
	Filing Date	2018-03-23
	First Named Inventor	Hyun Lee
	Art Unit	2131
	Examiner Name	Hashem FARROKH
	Attorney Docket Number	0016.001000G

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Webster's II New College Dictionary, Houghton Mifflin Company, Boston, MA, 2001, pp. 259, 1115, 2 pages.	
	2	Wong, A. "The BIOS Optimization Guide", Adrian's Rojak Pot, Rev. 6.2, 1998-2001, 67 pages.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15934416
	Filing Date	2018-03-23
	First Named Inventor	Hyun Lee
	Art Unit	2131
	Examiner Name	Hashem FARROKH
	Attorney Docket Number	0016.001000G

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2020-06-01
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	15934416
Filing Date:	23-Mar-2018
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Stephanie Semler
Attorney Docket Number:	0016.001000G

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	39599998
Application Number:	15934416
International Application Number:	
Confirmation Number:	2728
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000G
Receipt Date:	02-JUN-2020
Filing Date:	23-MAR-2018
Time Stamp:	13:35:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$240
RAM confirmation Number	E202062D36018135
Deposit Account	602034
Authorized User	Stephanie Semler
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	IDS_20200601_0016001000G.pdf	1055806 4d367d9ec47094d17af9f4af3b22169ec674e04f	no	13
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30419 a1683380fe399e717f15539a56202fc554aead15	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1086225		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

USPTO Automated Interview Request (AIR)

Jun 28 2020

This paper requesting to schedule and/or conduct an interview is appropriate because:

This submission is requested to be accepted as an authorization for this interview to communicate via the internet. Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned concerning scheduling of the interview via video conference, instant messaging, or electronic mail, and to conduct the interview in accordance with office practice including video conferencing.

Name(s):
Khaled Shami

S-signature:
/Khaled Shami/

Registration Number:
38745

U.S. Application Number:
15934416

Confirmation Number:
2728

E-mail Address:
khaled@shamimessinger.com

Phone Number:
+1 6507455353

Proposed Time of Interview:
7-9-2020 10:00 AM ET

Alternative Proposed Time(s) of Interview:
7-10-2020 10:00 AM ET

Alternative Proposed Time(s) of Interview:
7-13-2020 10:00 AM ET

Prefered Interview Type:
Video Conference

I am the applicant or applicant's representative for this application.

Topic for Discussion:
Rejections under 35 USC 112 and 103

uspto UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/934,416	03/23/2018	Hyun Lee	0016.001000G	2728

151145 7590 07/29/2020

Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2131	

NOTIFICATION DATE	DELIVERY MODE
07/29/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

khaled@shamimessinger.com
mike@shamimessinger.com
stephanie@shamimessinger.com

Applicant-Initiated Interview Summary	**Application No.** 15/934,416	**Applicant(s)** Lee et al.	
	Examiner HASHEM FARROKH	**Art Unit** 2131	**AIA (FITF) Status** No

All participants (applicant, applicants representative, PTO personnel):

(1) HASHEM FARROKH.

(2) _____.

(3) Khaled Shami.

(4) Marwan Fawal.

Date of Interview: 24 July 2020.

Type: ☑ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☑ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☑102 ☐103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: Fukuzo (US 2006/0294295 A1).

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

See Continuation Sheet.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/HASHEM FARROKH/ Primary Examiner, Art Unit 2131	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiners responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicants correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,-
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicants record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiners version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, Interview Record OK on the paper recording the substance of the interview along with the date and the examiners initials.

Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments:

An applicant Initiated Interview with the Applicant, Mr. Khaled Shami, (Reg. # 38,745), was conducted on 07/24/2020. The interview was in response to the non-final office action mailed on 04/02/2020 (a copy of the interview agenda is attached). Applicant stated that as specified in the newly added claim 22, the access commands received by the controller (e.g., memory system) from the host is accordance to a volatile memory access protocol. However, Fukuzo uses additional commands such as /LD and /ST for transferring data between SDRAM and non-volatile memory. The Examiner stated that Fukuzo discloses additional features so that host also can access the FIFO buffer or non-volatile memory independently. For example FIFO buffer (e.g., a volatile memory) can be considered a buffer for temporary storing data to be written or read from non-volatile memory. Applicant further stated that claim 10 recites transferring data form the non-volatile memory to volatile memory if data associated with the first command does not reside in volatile memory. Examiner stated Fukuzo states that FIFO comprises a ready/busy flag. Ready means that data is ready ready for access. A busy means that data is not ready for access. Thus ready/busy flag indicates the status of data in the FIFO. However, during the interview no agreement reached.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.	CONFIRMATION NO: 2728
SERIAL NO: 15/934,416	ART UNIT: 2131
FILING DATE: 3/23/18	EXAMINER: FARROKH, Hashem

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND/OR REPLY TO OFFICE ACTION

Commissioner:

In response to the non-final Office Action mailed April 2, 2020, Applicant submits the following Amendment and Remarks.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page **2**.

Remarks begin on page **8.**

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2034.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Currently amended) A memory system, comprising:

a memory ~~device~~ subsystem including a ~~first~~ dynamic random access memory (DRAM) ~~portion~~ and a ~~second~~ non-volatile memory ~~portion~~; and

a controller configured to be coupled to a system memory controller of a host system and to the memory ~~device~~subsystem, the controller ~~is~~ configured to control operation of the non-volatile memory and the DRAM in response to a double data rate (DDR) memory access command received from the system memory controller in accordance with a standard DDR protocol for accessing the DRAM,

wherein, in response to a DDR memory access command corresponding to a read operation, the controller is configured to determine if data information requested by the read operation is not stored in the DRAM and is stored in the non-volatile memory, and based on said determination, to initiate and control at least one data transfer operation from the non-volatile memory to the DRAM and, subsequently, at least one data transfer operation from the DRAM to the system memory controller ~~transfer data information from the second memory portion to the first memory portion in response to a first command received by the controller from the system memory controller, the controller is further configured to alert the system memory controller when the data information is ready to be retrieved, and wherein the data information is retrieved from the second memory portion in response to a second command received by the controller from the system memory controller~~.

3. (Currently amended) The memory system of claim 2, wherein the memory system ~~first memory portion includes~~ comprises a dual-inline memory module (DIMM) form factor ~~volatile memory, and wherein the second memory portion includes non-volatile memory~~.

4. (Currently amended) The memory system of claim 2, wherein the DRAM ~~first memory portion~~ includes double data rate ~~dynamic random access memory (~~DRAM~~),~~ and ~~wherein~~ the ~~second memory portion~~non-volatile memory includes FLASH memory.

5. (Currently amended) The memory system of claim 2, wherein the standard DDR protocol for accessing the DRAM includes one or more of DDR2, DDR3, and DDR4 protocols ~~first command received from the system memory controller corresponds to a memory read operation received from the system memory controller in accordance with a protocol~~.

6. (Currently amended) The memory system of claim 2, wherein, in response to the DDR memory access command corresponding to the read operation, ~~the controller is coupled to the system memory controller of the host system via system address lines, wherein~~ the controller is further configured to determine ~~an~~ a target address of where the data information is stored ~~based on a first number of address bits and a second number of address bits, and wherein the controller is configured to receive the first number of address bits and the second number of address bits sequentially over the system address lines~~.

7. (Currently amended) The memory system of claim ~~6~~2, wherein the controller is configured to provide a transparent operation to the system memory controller in accordance with a double data rate protocol, and wherein the system memory controller does not have a direct access to the non-volatile memory~~concatenate the first number of address bits and the second number of address bits to determine the address of the data information~~.

8. (Currently amended) The memory system of claim ~~7~~2, wherein the controller is further configured to map a DRAM address space to a non-volatile memory address space~~first number of address bits is twelve~~.

9. (Currently amended) The memory system of claim ~~5~~2, wherein the controller is further configured to form a non-volatile memory address using a first and second sets of address bits, and wherein the non-volatile memory address includes at least a block address field and a page address field~~receive the second command from the system memory controller according to the protocol~~.

10. (Currently amended) A memory module couplable to a system memory controller of a host system, the memory module comprising:

a controller operable to receive from the system memory controller a first memory access command via system address lines in accordance with a standard double data rate (DDR) protocol;

a non-volatile memory device; and

a volatile memory device;

wherein, in response to the first memory access command, the controller is configured to:

determine a target address of where ~~if~~ data information associated with the first memory access command is located,

~~stored in the volatile memory device or the non-volatile memory device, and if the data associated with the first memory access command does not reside in the volatile memory device, the controller is further configured to~~

perform a data transfer operation ~~of the data associated with the first memory access command~~ from the non-volatile memory device if ~~to the volatile memory device; wherein the controller is further configured to alert the system memory controller that~~ the data information associated with the first memory ~~access~~ command does not reside in ~~is ready to be retrieved from~~ the volatile memory device but resides in the non-volatile memory device, and alert the system memory controller when the data information associated with the first memory command is ready to be retrieved from the volatile memory device~~; and wherein the data associated with the first memory access command is retrieved from the volatile memory device in response to a second memory access command received by the controller from the system memory controller~~.

11. (Currently amended) The memory module of claim 10, wherein the volatile memory device includes double data rate (DDR) dynamic random access memory (DRAM), and wherein the volatile memory device includes FLASH memory.

12. (Currently amended) The memory module of claim 10, wherein the first memory access command received from the system memory controller corresponds to a memory read operation from the volatile memory device in accordance with the standard DDR ~~according to a~~ protocol.

13. (Currently amended) The memory module of claim ~~12~~10, wherein the ~~first memory access command received from the system memory~~ controller is configured to form a non-volatile memory address using first and second sets of address bits, and wherein the non-volatile memory address includes at least a block address field and a page address field~~includes a first command RC(X) received from the system memory controller over the system address lines and a second command RC(X+1) received after the first command RC(X) from the system memory controller over the system address lines~~.

14. (Currently amended) The memory module of claim 13, wherein the controller is configured to receive the first set of address bits and the second set of address bit from the system memory controller using the set of address and control lines~~first command RC(X) includes a first number of address bits, and wherein the second command RC(X+1) includes a second number of address bits in accordance with the protocol~~.

15. (Currently amended) The memory module of claim ~~14~~10, wherein the standard DDR protocol for accessing the DRAM includes one or more of DDR2, DDR3, and DDR4 protocols~~controller is further configured to determine an address of the data associated with the first memory access command based on the first number of address bits and the second number of address bits~~.

16. (Currently amended) The memory module of claim ~~14~~10, wherein the controller is further configured to map a volatile memory address space to a non-volatile memory address space~~first number of address bits is equal to twelve~~.

17. (Currently amended) The memory module of claim ~~14~~10, wherein the controller is further configured to provide a transparent operation to the system memory controller in accordance with the DDR protocol, and wherein the system memory controller does not have a direct access to the non-volatile memory~~concatenate the first number of address bits and the second number of address bits to determine an address of the data associated with the first memory access command~~.

18. (Currently amended) The memory module of claim ~~10~~12, wherein the controller is further configured to form a non-volatile memory address using a first and second sets of address bits, and wherein the non-volatile memory address includes at least a block address field and a page address field~~receive the second memory access command according to the protocol~~.

19. (Currently amended) A memory module couplable to a system memory controller of a host system via a set of data lines and a set of system address and control lines, the memory module~~,~~ comprising:

a controller operable to receive from the system memory controller, via the set of system address and control lines, a first memory ~~access~~ command~~,~~ in accordance with a standard double data rate (DDR) protocol ~~the first memory access command including a first address~~;

a non-volatile memory device;

a volatile memory device; and

a data manager coupled to the controller, the system controller, the non-volatile memory device, and the volatile memory device, the data manager configured to exchange data with one or more of the non-volatile memory device, the volatile memory device, and the system ~~the~~ memory controller in response to control information received from the controller~~via a data interface in response to control information received from the controller~~;

wherein, in response to the first memory access command, the controller is configured to:

determine a target address of where data information associated with the first memory command is located ~~if data associated with the first address is stored in the volatile memory device or the non-volatile memory device~~;

~~wherein, if the data associated with the first address does not reside in the volatile memory device, the controller is configured to~~ perform ~~a~~ at least one data transfer operation from the non-volatile memory device to the volatile memory device by way of the data manager if the data information associated with the first memory command does not reside in the volatile memory device but resides in the non-volatile memory device; and

subsequently perform at least one data transfer operation from the volatile memory device to the system memory controller by way of the data manager via the set of data lines~~wherein the controller is further configured to alert the memory controller that the data associated with the first address is ready to be retrieved from the volatile memory device; and wherein the data associated with the first address is retrieved from the volatile memory device in response to a second memory access command received by the controller from the system memory controller~~.

20. (Currently amended) The memory module of claim 19, further comprising:

a register configured to store memory address space information, wherein the controller is further configured to map a volatile memory address space to a non-volatile memory address space using the memory address space information stored in the register~~register multiple commands or a sequence of commands~~.

21. (Currently amended) The memory module of claim 20, wherein the first memory access command received by the controller from the system memory controller corresponds ~~correspond~~ to a memory read operation.

REMARKS

Applicant has received and carefully reviewed the non-final Office Action of April 2, 2020. Applicant respectfully requests reconsideration in view of the following remarks.

Upon entry of the foregoing amendment, claims 2-21 are pending in this application, with claims 2, 10 and 19 being independent.

Interview Record

Applicant gratefully acknowledges the courtesy and consideration extended to Applicant's undersigned representative during the telephone interview with Examiner Farrokh on July 21, 2020.

During the interview, the undersigned generally explained the difference between the invention and Fukuzo, and in particular the failure of Fukuzo to use DDR protocol, or to transfer data from the nonvolatile to volatile memory if the data does not reside in the DRAM, as argued below. No agreement was reached.

Objection to the Specification

The specification is objected to as allegedly failing to provide proper antecedent basis for the limitations from claims 7 and 17 of "concatenate the first number of address bits and the second number of address bits..." Without conceding the propriety of such objection, Applicant has amended the claims to remove this feature.

Claim Version

Applicant acknowledges the inadvertent use of an outdated version of the claims in the prior response. In the above listing of claims in this response, the claims have been amended to a

current version, with the changes shown in underlining and strikethrough as appropriate. This listing of claims will replace all prior versions, and listings, of claims in the application.

Rejection(s) Under 35 U.S.C. § 112(a)

Claims 6-8, 13-17, and 21 stand rejected under 35 U.S.C. § 112(a) as allegedly failing to comply with the written description requirement.

The Office Action alleges that the specification fails to describe or support the limitation from claims 6 "receive the first set of address bits and the second set or address bits sequentially over the system address lines." Without conceding the propriety of this allegation, and merely to expedite prosecution, Applicant has amended the claim to remove this feature.

The Office Action alleges that the specification fails to describe or support the limitations from claims 7 "wherein the controller is further configured to concatenate the first set of address bits and the second set of address bits to determine the address of the data information" and the limitation from claim 17 "wherein the controller is further configured to concatenate the first number of address bits and the second number of address bits to determine an address of the data information associated with the first memory command." Without conceding the propriety of this allegation, and merely to expedite prosecution, Applicant has amended the claims to remove this feature.

The Office Action alleges that the specification fails to describe or support the limitation from claims 13 "wherein the first memory command includes a first command RC(X) received from the system memory controller over the set of system address and control lines and a second command RC(X+1) received after the first command RC(X) from the system memory controller over the set of system address and control lines." Without conceding the propriety of this allegation, and merely to expedite prosecution, Applicant has amended the claim to remove this feature.

The Office Action alleges that the specification fails to describe or support the limitation from claims 15 "wherein the controller is further configured to determine an address of the data information associated with the first memory command based on the first number of address bits and the second number of address bits." Without conceding the propriety of this allegation, and merely to expedite prosecution, Applicant has amended the claim to remove this feature.

The Office Action alleges that the specification fails to describe or support the limitation from claims 21 "wherein the second command is received by the controller after the first command is received by the controller, and wherein the controller is configured to determine an address of the data information associated with the first memory command using the first set of address bits and the second set of address bits." Without conceding the propriety of this allegation, and merely to expedite prosecution, Applicant has amended the claim to remove this feature.

It is respectfully submitted that claims 6-8, 13-17, and 21 are now in compliance with 35 U.S.C. § 112(a) and the rejection should be withdrawn.

Rejection(s) Under 35 U.S.C. § 103(a)

Claims 2-5, 9-12, and 18-19 stand rejected under pre-AIA 35 U.S.C. 102(a)(2) as anticipated by or, in the alternative, under pre-AIA 35 U.S.C. 103(a) as obvious over Fukuzo "Fukuzo" (US 2006/0294295 A1).

Applicant respectfully traverses.

Independent claims 2, 10 and 19, from which the remaining claims variously depend, have been amended to recite, for example according to claim 2:

> a controller configured to be coupled to a system memory controller of a host system and to the memory subsystem, the controller configured to control operation of the non-volatile memory and the DRAM in response to a double data rate (DDR)

> memory access command received from the system memory controller in accordance with a standard DDR protocol for accessing the DRAM,

This feature, described for example in ¶[0079] of the present application, is not disclosed in Fukuzo. As seen in FIG. 2 of Fukuzo, NAND-flash controller section 514a requires "4 additional pins provided via the first interface 504' [that] serve to yield additional commands for operating the flash controller section 514a as well as a FIFO memory buffer section provided with the SDRAM memory chip device." (¶[0079], emphasis added) By requiring the additional pins, NAND-flash controller is no longer compliant with a standard DDR protocol, and cannot be considered "configured to control operation of the non-volatile memory and the DRAM in response to a double data rate (DDR) memory access command received from the system memory controller in accordance with a standard DDR protocol for accessing the DRAM" as presently claimed.

It will appreciated that Fukuzo's interface combines a conventional volatile memory (SDRAM) interface having 60 Data/Address/Control signal lines with additional dedicated signals for commanding the operation of nonvolatile memory (FLASH). Fukuzo thus does not teach operating the nonvolatile memory subsystem using the well-known protocol of the volatile memory interface. The additional pins in Fukuzo are expressly provided for control of the non-volatile (FLASH) memory, and their use is contrasted against conventional SDRAM protocol. Fukuzo thus explains that "additional pins are provided to the interface as compared with the SDRAM standard. These additional pins are arranged to transmit signals, which yield control of background store and load operations with respect to those data intended for permanent storage within the NAND-flash memory, while data are transferred between the host CPU 50 and the SDRAM array 190." (¶[0082], emphasis added) Thus Fukuzo establishes and discloses his own defined rules for controlling the operation of the nonvolatile memory subsystem (Fukuzo ¶[0110]), which are not part of the conventional and standard volatile memory SDRAM interface. (Fukuzo ¶[0022]). Fukuzo, provides clear disclosure of the distinct operation of the nonvolatile memory subsystem (FLASH) using the dedicated command signal lines and feedback signal lines /LD, /ST, /FIFO, and /FLASH (Fukuzo [0101]-[0105]). Various examples of store and load operations between host system CPU 50 and nonvolatile memory (Flash) are described in Fukuzo paragraphs: [0021]-[0024], [0028], [0109]-[0113], and [0126].

Thus Fukuzo does not disclose a "controller configured to control operation of the non-volatile memory and the DRAM in response to a double data rate (DDR) memory access command received from the system memory controller in accordance with a standard DDR protocol for accessing the DRAM" as presently claimed.

Independent claims 2, 10 and 19 have also been amended to recite, for example according to claim 2:

> wherein, in response to a DDR memory access command corresponding to a read operation, the controller is configured to determine if data information requested by the read operation is not stored in the DRAM and is stored in the non-volatile memory, and based on said determination, to initiate and control at least one data transfer operation from the non-volatile memory to the DRAM and, subsequently, at least one data transfer operation from the DRAM to the system memory controller.

As explained above, Fukuzo's operation is not consistent with DDR memory access protocol. Moreover, does not teach transfer of data from the nonvolatile memory subsystem (FLASH) to the volatile memory subsystem (DRAM) if the data does not reside in the DRAM. Fukuzo provides a detailed description of memory operations required to access and retrieve data from nonvolatile memory. Fukuzo discloses his nine proprietary commands formed by the combination of Fukuzo's additional signals, namely /LD and /ST, and conventional DDR control signals, namely /CS, /CAS, /RAS, /WE, and /CKE. These new commands are decoded in Command Decoder 150 (FIG. 3). Nowhere in Fukuzo is there a disclosure, teaching, or suggestion of a data transfer from the nonvolatile memory subsystem to the volatile memory subsystem based on a determination "if data information requested by the read operation is not stored in the DRAM" as presently claimed. Rather, Fukuzo's CPU fully manages retrieval of data from nonvolatile memory using other proprietary commands. (Fukuzo ¶¶[0109] – [0126]). Specifically, Fukuzo describes data processor 210 for controlling the respective data transfer buses internal to the Fukuzo chip (FIG. 5), and complete details operation in Fig. 3, and Fig. 4 corresponding paragraphs. Fukuzo controls data transfer from nonvolatile memory to volatile memory by sending the source address (where the data is to be copied from Flash) and by sending the destination address of SDRAM core (where the data is to be transferred to) (Fukuzo

¶¶ [0109], [0110], [0113], and [0125]. Fukuzo's CPU50 sends the source and destination addresses for use by the nonvolatile memory controller using Fukuzo's proprietary commands and the address bus ADD[0-20] of interface 14 (FIG. 4). Thus Fukuzo does not teach anywhere or even suggest that data is transferred from nonvolatile memory to volatile memory if data does not reside in volatile memory.

For these reasons at least, Applicant respectfully maintains that the invention as claimed is neither anticipated or rendered obvious by Fukuzo, and the rejection of claims 2-5, 9-12, and 18-19 under 35 U.S.C. §§ 102 and/or 103 based on this reference should be withdrawn.

Claim 20 stands rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over as Fukuzo in view of "Shiota" (US 2003/0147297 A1).

Claim 20 depends from claim 19 addressed above. Shiota fails to remedy the above-mentioned shortcomings of Fukuzo with respect to base claim 19. Accordingly, claim 20, which by definition include all the limitations of the base claim, is patentable over the combination of these references.

Conclusion

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 60-2034.

Respectfully submitted,

Dated: October 2, 2020

/Khaled Shami/_____
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
202-516-6900

Electronic Patent Application Fee Transmittal

Application Number:	15934416
Filing Date:	23-Mar-2018
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Stephanie Semler
Attorney Docket Number:	0016.001000G

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1480	1480
Miscellaneous:				
		Total in USD ($)		**1480**

Electronic Acknowledgement Receipt	
EFS ID:	40744505
Application Number:	15934416
International Application Number:	
Confirmation Number:	2728
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000G
Receipt Date:	02-OCT-2020
Filing Date:	23-MAR-2018
Time Stamp:	11:39:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1480
RAM confirmation Number	E202002B42082007
Deposit Account	602034
Authorized User	Stephanie Semler
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		0016001000G_Resp_NFOA.pdf	170208 5889a6fb503aea83b40ec0c11152b5820a042b16	yes	14

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Claims	2	7
Applicant Arguments/Remarks Made in an Amendment	8	14

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30726 17a7f5862a8405f934a5ad9f22e11d9480c1a9c9	no	2

Warnings:

Information:

Total Files Size (in bytes):	200934

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/934,416	Filing Date 03/23/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	10/02/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/EMORY T LANE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/934,416	03/23/2018	Hyun Lee	0016.001000G	2728

151145 7590 01/01/2021

Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2135	

NOTIFICATION DATE	DELIVERY MODE
01/01/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

khaled@shamimessinger.com
mike@shamimessinger.com
stephanie@shamimessinger.com

Office Action Summary	Application No. 15/934,416	Applicant(s) Lee et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 10/02/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 2-21 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 2-21 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 03/23/2018 is/are: a)☐ accepted or b)☑ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 6/2/20.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

This office action is in response to the communication(s) filed on 10/02/2020. There are a total 21 claims pending in the application; claim 1 has been canceled, claims 2-21 have been amended, and no new claims have been added.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: reference numeral codes in Fig. 8A of Drawing does match the specification description. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

INFORMATION CONCERNING IDS:

The information disclosure statement (IDS) submitted on 06/02/2020 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner. However, the documents listed under the heading of "Non-patent Literature Documents" have not been considered by the Examiner because a copy of the documents have not been provided.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.*

Claims 2, 6-7, 10, 12, 17, and 19 are rejected under pre-AIA 35 U.S.C. 102(a)(2) as being anticipated by Bonella et al. "Bonella" (US 2007/0136523 A1).

1. *In regard to claim 2 Bonella teaches:*

"A memory system **(e.g., Figs 1-2)**, comprising: a memory subsystem including a dynamic random access memory (DRAM) **(e.g., DRAM memory in Fig. 1)** and a non-volatile memory;" **(e.g., ¶ 0029, flash memory in Fig. 1).**

"and a controller configured to be coupled to a system memory controller of a host system **(e.g., ¶ 0065, Fig. 3, host system main memory and cache hierarchy)** and to the memory subsystem **(e.g., ¶¶ 0029-0030, memory module controller in Figs 1-2)**, the controller configured to control operation of the nonvolatile memory **(e.g., flash memory in Fig. 1)** and the DRAM **(e.g., DRAM memory in Fig. 1)** in response to a double data rate (DDR) memory access command received from the system memory controller in accordance with a standard DDR protocol for accessing the DRAM," **(e.g., ¶ 0036, The DRAM interface in the illustrative embodiment of FIG. 2 conforms to the IEEE DDR2 DRAM specification; ¶ 0043, Fig. 2, illustrative embodiment shown in FIG. 2 is made up of path multiplexers for Address, Command and Data; ¶ 0077, A data set request is issued from the host system and the driver determines if that data set is available in the memory module).**

"wherein, in response to a DDR memory access command corresponding to a read operation, the controller is configured to determine if data information requested by the read operation is not stored in the DRAM and is stored in the non-volatile memory, and based on said determination, to initiate and control at least one data transfer operation from the non-volatile memory to the DRAM and, subsequently, at least one data transfer operation from the DRAM to the system memory controller." **(e.g., claim 8, responsive thereto determine whether data set is stored in the volatile memory or non-**

volatile memory; ¶ 0077, A data set request is issued from the host system and the driver determines if that data set is available in the memory module. If that data set is available, the request is issued to the memory module where it checks the pointers for where to retrieve that data); ¶ 0086, Fig. 7, If the request is sourced from FLASH, then a series of checks are made and data movement may be initiated to DRAM if the appropriate flags are set and all criteria are met as previously described).

2. In regard to claim 10 Bonella teaches:

"A memory module **(e.g., memory module in Figs. 1-2)** couplable to a system memory controller of a host system **(e.g., ¶¶ 0029, 0065)**, the memory module comprising: a controller operable to receive from the system memory controller a first memory access command via system address lines in accordance with a standard double data rate (DDR) protocol;" **(e.g., ¶ 0036, The DRAM interface in the illustrative embodiment of FIG. 2 conforms to the IEEE DDR2 DRAM specification; ¶ 0043, Fig. 2, illustrative embodiment shown in FIG. 2 is made up of path multiplexers for Address, Command and Data; ¶ 0077, A data set request is issued from the host system and the driver determines if that data set is available in the memory module).**

"a non-volatile memory device;" **(e.g., ¶ 0029, flash memory in Fig. 1).**

"and a volatile memory device;" **(e.g., DRAM memory in Fig. 1).**

"wherein, in response to the first memory access command, the controller is configured to: determine a target address of where data information associated with the first memory access command is located," **(e.g., claim 8, responsive thereto determine whether data set is stored in the volatile memory or non-volatile memory; ¶ 0077, A data set request is issued from the host system and the driver determines if that data set is available in the memory module. If that data set is available, the request is issued to the memory module where it checks the pointers for where to retrieve that data)**.

"perform a data transfer operation from the non-volatile memory device if the data information associated with the first memory command does not reside in volatile memory device but resides in the non-volatile memory device, and alert the system memory controller when the data information associated with the first memory command is ready to be retrieved from the volatile memory device." **(e.g., claim 8, responsive thereto determine whether data set is stored in the volatile memory or non-volatile memory; ¶ 0077, A data set request is issued from the host system and the driver determines if that data set is available in the memory module. If that data set is available, the request is issued to the memory module where it checks the pointers for where to retrieve that data); ¶ 0086, Fig. 7, If the request is sourced from FLASH, then a series of checks are made and data movement may be initiated to DRAM if the appropriate flags are set and all criteria are met as previously described).**

3. In regard to claim 19 Bonella teaches:

"A memory module couplable to a system memory controller of a host system via a set of data lines and a set of system address and control lines, the memory controller comprising: a controller operable to receive from the system memory controller, via the set of system address and control lines, a first memory command; in accordance with a standard double data rate (DDR) protocol;" **(e.g., ¶ 0036, The DRAM interface in the illustrative embodiment of FIG. 2 conforms to the IEEE DDR2 DRAM specification; ¶ 0043, Fig. 2, illustrative embodiment shown in FIG. 2 is made up of path multiplexers for Address, Command and Data; ¶ 0077, A data set request is issued from the host system and the driver determines if that data set is available in the memory module).**

"a non-volatile memory device;" **(e.g., flash memory in Fig. 1).**

"a volatile memory device;" **(e.g., DRAM memory in Fig. 1).**

"and a data manager **(e.g., ¶ 0043, router)** coupled to the controller **(e.g., memory module or MM controller in Fig. 1)**, the system controller **(e.g., host CPU)**, the non-volatile memory device **(e.g., flash memory in Fig. 1)** and the volatile memory device **(e.g., DRAM memory in Fig. 1)**, the data manager configured to exchange data with one or more of the non-volatile memory device, the volatile memory device, and the system memory controller in response to control information received from the controller;" **(e.g., ¶¶ 0043 and 0065; Figs. 1-2 and corresponding text description).**

"wherein, in response to the first memory access command, the controller is configured to: determine a target address of where data information associated with the first memory

command is located;" **e.g., claim 8, responsive thereto determine whether data set is stored in the volatile memory or non-volatile memory; ¶ 0077, A data set request is issued from the host system and the driver determines if that data set is available in the memory module. If that data set is available, the request is issued to the memory module where it checks the pointers for where to retrieve that data**).

"perform at least one data transfer operation from the non-volatile memory device to the volatile memory device by way of the data manager if the data information associated with the first memory command does not reside in the volatile memory device but resides in the non-volatile memory device;" **(e.g., claim 8, responsive thereto determine whether data set is stored in the volatile memory or non-volatile memory; (e.g., ¶ 0077, A data set request is issued from the host system and the driver determines if that data set is available in the memory module. If that data set is available, the request is issued to the memory module where it checks the pointers for where to retrieve that data); (e.g., ¶ 0086, Fig. 7, If the request is sourced from FLASH, then a series of checks are made and data movement may be initiated to DRAM if the appropriate flags are set and all criteria are met as previously described).**

"and subsequently perform at least one data transfer operation from the volatile memory device to the system memory controller by way of the data manager via the set of data lines." **(e.g., ¶ 0086, Fig. 7).** *The flow diagram in Fig. 7 of Bonella show when data resides or located in DRAM it's read from DRAM, and if resides in flash data is moved from flash to DRAM and then is loaded from flash to the system (e.g., host).*

4. In regard to claims 6 and 12 Bonella further teaches:

"wherein, in response to the DDR memory access command corresponding to the read operation, the controller is further configured to determine a target address of where the data information is stored." **(e.g., ¶ 0077, check the pointer for location or target address where data is stored in memory module – DRAM or flash).**

5. In regard to claims 7 and 17 Bonella further teaches:

"wherein the controller is configured to provide a transparent operation to the system memory controller in accordance with a double data rate protocol **(e.g., ¶ 0036, Fig. 2, IEEE DDR2 Specification)**, and wherein the system memory controller does not have a direct access to the non-volatile memory." **(e.g., ¶ 0041, Figs. 1-2).** *Bonella does not expressly recites a transparent operation, but teaches memory module controller (e.g., Fig. 1) comprising a router (Fig. 2) receives address, command, and data from the host and manages the operation of DRAM and Flash independent from the host. The system CPU or controller does not have direct access to non-volatile memory (or DRAM (e.g., see Fig. 2). Therefore, Bonella inherently teaches memory controller provide a transparent operation to the host.*

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of

rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claim 3-5, 11 and 15 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bonella in view of Prete et al. "Prete" (US 2008/0126624 A1).

6. In regard to claim 3 Bonella teaches all limitations included in claim 2 but does not appear to expressly teach while Prete discloses:

"Wherein the memory system comprises a dual-inline memory module (DIMM) form factor." **(e.g., ¶ 0033, Fig. 2)** *using Dual Inline Memory Module (DIMM).*

Disclosures by Bonella and Prete are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the memory module taught by Bonella to include the DIMM disclosed by Prete.

The motivation for including the DIMM as taught by paragraph [0033] of Prete is to allow accessing one or more memory modules from a single memory controller.

Therefore, it would have been obvious to combine teaching of Prete with Bonella to obtain the invention as specified in the claim.

7. In regard to claims 4 and 11 Prete further teaches:

"wherein the DRAM includes double data rate DRAM and non-volatile memory includes FLASH memory." **(e.g., ¶ 0017).**

8. In regard to claims 5 and 15 Prete further teaches:

"wherein the standard DDR protocol for accessing the DRAM includes one or more of DDR2, DDR3, and DDR4 protocols." **(e.g., ¶ 0017).**

Claims 8 and 16 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bonella in view of Randell et al. "Randell" (US 2005/0183472 A1).

9. In regard to claims 8 and 16 Bonella teaches all limitation claims 2 and 10 but does not expressly teach while Randell disclose:

"wherein the controller is further configured to map a DRAM address space to a non-volatile memory address space." **(e.g., ¶¶ 0012, 0052, and 0063; Fig. 4)** *using SDRAM as cache and mapping or correlating address space of cache with address space of flash memory.*

Disclosures by Bonella and Randell are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the memory module taught by Bonella to include the SDRAM used as cache disclosed by Randell.

The motivation for including the SDRAM used as cache as taught by paragraph [0052] of Randell is for reducing the burden on the memory system.

Therefore, it would have been obvious to combine teaching of Randell with Bonella to obtain the invention as specified in the claim.

Claims 9, 13-14, 18, and 20-21 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bonella in view of Kita "Kita" (US 2005/0144418 A1).

10. In regard to claims 9 and 13 Bonella teaches all limitations included in claims 2, 10, and 12 but does not exclusively teach while Kita discloses"

"wherein the controller is further configured to form a non-volatile memory address using a first and second sets of address bits, and wherein the non-volatile memory address includes at least a block address field and a page address field." **(e.g., ¶¶ 0112-0115; Fig. 9)** *forming a physical page address, wherein the physical page address comprises a physical block address (PBA) portion (e.g., field) and page number portion (e.g., field).*

Disclosures by Bonella and Kita are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the memory module taught by Bonella to include the forming of the physical page address disclosed by Kita.

The motivation for including the forming of the physical page address as taught by paragraphs [00113]-[00115] of Kita is to minimize a maximum number of defective blocks to be classified into each of the plurality of zones.

Therefore, it would have been obvious to combine teaching of Kita with Bonella to obtain the invention as specified in the claim.

11. In regard to claim 14 Kita further teaches:

"wherein the controller is configured to receive the first set of address bits and the second set of address bit from the system memory controller using the set of address and control lines." **(e.g., ¶¶ 0077, 0112-0115; Figs. 8-9).** *Virtual page address comprises the first set of address bits (e.g., VBA) and the second set address bits (e.g., page number, see Fig. 9).*

12. In regard to claim 18 Kita further teaches:

"wherein the controller is further configured to form a non-volatile memory address using a first and second sets of address bits **(e.g., Fig. 9, set address bits corresponding PBA and page number)**, and wherein the non-volatile memory address includes at least a block address field and a page address field." **(e.g., ¶¶ 0112-0115; Fig. 9).**

13. In regard to claim 20 Kita further teaches:

"a register configured to store memory address space information, wherein the controller is further configured to map a volatile memory address space to a non-volatile memory address space using the memory address space information stored in the register." **(e.g., ¶ 0113, Fig. 8, The process setting register 34 stores information representing the correspondence between the virtual block address VBA and the physical block address PBA).**

14. In regard to claim 21 Bonella further teaches:

"wherein the first memory access command received by the controller from the system memory controller corresponds to a memory read operation." **(e.g., ¶ 0041; Fig. 2).** *Commands from the PCIe and the USB 2.0 buses comprises RD/WR commands including the first memory access command recited in the claim.*

Response to Remarks

Applicant arguments have been fully considered and they have been persuasive. Thus, the previous rejections are withdrawn. However, the amendments have change the scope of claims and claims are now rejected in new ground of rejections. The applicant arguments regarding the previous rejections are considered moot.

The Examiner respectfully submits that Bonella alone and/or in combination with the other prior art record as set forth in this Office Action teach or render obvious all

limitations including the newly added limitations in the claims. Accordingly, Examiner maintains his position.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ann Lo can be reached on (571)272-9767. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/

Primary Examiner, Art Unit 2131

Wednesday, December 30, 2020

Notice of References Cited	Application/Control No. 15/934,416	Applicant(s)/Patent Under Reexamination Lee et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20070136523-A1	06-2007	Bonella; Randy M.	G06F12/0866	711/113
*	B	US-20080126624-A1	05-2008	Prete; Edoardo	G11C7/106	710/53
*	C	US-20050183472-A1	08-2005	Choi, Kang Mo	D06F37/22	68/23.1
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	E					
	F					
	G					
	H					
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	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/934,416	Lee et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/17/2019	10/09/2019	03/28/2020	12/29/2020					
	1	✓	-	-	-					
	2		✓	✓	✓					
	3		✓	✓	✓					
	4		✓	✓	✓					
	5		✓	✓	✓					
	6		✓	✓	✓					
	7		✓	✓	✓					
	8		✓	✓	✓					
	9		✓	✓	✓					
	10		✓	✓	✓					
	11		✓	✓	✓					
	12		✓	✓	✓					
	13		✓	✓	✓					
	14		✓	✓	✓					
	15		✓	✓	✓					
	16		✓	✓	✓					
	17		✓	✓	✓					
	18		✓	✓	✓					
	19		✓	✓	✓					
	20		✓	✓	✓					
	21		✓	✓	✓					

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/934,416	Lee et al.
	Examiner	Art Unit
	HASHEM FARROKH	2135

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F13/1694; G06F12/0246; G06F13/28; G06F13/4243; G06F2212/7208; G06F3/0685; G06F12/0638; G06F13/4027; G06F1/185; G06F2212/205; G06F3/0613; G06F3/0659; G11C7/1072; G11C14/0018	03/17/2019	HF
G06F12/0246; G06F3/0685; G06F12/0638; G06F13/28; G06F2212/7208; G06F3/0613; G06F3/0659; G11C7/1072	10/09/2019	HF
G06F12/0246; G06F3/0685; G06F13/1694; G06F2212/205; G06F3/0659; G06F13/28; G06F2212/7208; G06F3/0613; G06F12/0638; G06F1/185; G11C14/0018; G11C7/1072	03/28/2020	HF

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	110	03/17/2019	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/934,416	Lee et al.
	Examiner	Art Unit
	HASHEM FARROKH	2135

Search Notes		
Search Notes	**Date**	**Examiner**
PALM and Inventor Search	03/16/2019	HF
EAST Text Search	03/16/2019	HF
Google Search	03/17/2019	HF
PALM and Inventor Search Updated	10/09/2019	HF
EAST Text Search Updated	10/09/2019	HF
PALM and Inventor Search Updated	03/28/2020	HF
EAST Text Search Updated	03/27/2020	HF
PALM and Inventor Search Updated	12/29/2020	HF
EAST Text Search Updated	12/29/2020	HF

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
711	110	03/28/2020	HF

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15934416
Filing Date	2018-03-23
First Named Inventor	Hyun Lee
Art Unit	~~2131~~ 2135
Examiner Name	Hashem FARROKH
Attorney Docket Number	0016.001000G

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	First Named Inventor	Hyun Lee
	Art Unit	2131
	Examiner Name	Hashem FARROKH
	Attorney Docket Number	0016.001000G

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

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	Examiner Name	Hashem FARROKH
	Attorney Docket Number	0016.001000G

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

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	Art Unit	2131
	Examiner Name	Hashem FARROKH
	Attorney Docket Number	0016.001000G

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	36	6421279	B1	2002-07-16	Tobita et al.	
	37	6459647	B1	2002-10-01	Kengeri	
	38	6487102	B1	2002-11-26	Halbert et al.	
	39	6487623	B1	2002-11-26	Emerson et al.	
	40	6571244	B1	2003-05-27	Larson	
	41	6614685	B2	2003-09-02	Wong	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15934416
	Filing Date	2018-03-23
	First Named Inventor	Hyun Lee
	Art Unit	2131
	Examiner Name	Hashem FARROKH
	Attorney Docket Number	0016.001000G

	42	6658507	B1	2003-12-02	Chan	
	43	6691209	B1	2004-02-10	O'connell	
	44	6693840	B2	2004-02-17	Shimada et al.	
	45	6721860	B2	2004-04-13	Klein	
	46	6769081	B1	2004-07-27	Parulkar	
	47	6799241	B2	2004-09-28	Kahn et al.	
	48	6799244	B2	2004-09-28	Tanaka et al.	
	49	6810513	B1	2004-10-26	Vest	
	50	6816982	B2	2004-11-09	Ravid	
	51	6839774	B1	2005-01-04	Ahn et al.	Entire Document
	52	6944042	B2	2005-09-13	Komatsuzaki	

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	53	6948029	B2	2005-09-20	Yano	
	54	6952368	B2	2005-10-04	Miura et al.	
	55	7053470	B1	2006-05-30	Sellers et al.	
	56	7062618	B2	2006-06-13	Tsunoda et al.	
	57	7089412	B2	2006-08-08	Chen	
	58	7102391	B1	2006-09-05	Sun et al.	
	59	7111142	B2	2006-09-19	Spencer et al.	
	60	7136978	B2	2006-11-14	Miura et al.	
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	62	7200021	B2	2007-04-03	Raghuram	
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	64	7353325	B2	2008-04-01	Lofgren et al.	
	65	7409491	B2	2008-08-05	Doblar et al.	
	66	7409590	B2	2008-08-05	Moshayedi et al.	
	67	7411859	B2	2008-08-12	Sohn et al.	
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	69	7467251	B2	2008-12-16	Park et al.	
	70	7519754	B2	2009-04-14	Wang et al.	
	71	7600142	B2	2009-10-06	Ichikawa	
	72	7716411	B2	2010-05-11	Panabaker et al.	
	73	7818488	B2	2010-10-19	Park et al.	
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	Attorney Docket Number	0016.001000G

	75	8086955	B2	2011-12-27	Zhou et al.	
	76	8102614	B2	2012-01-24	Song et al.	
	77	8233303	B2	2012-07-31	Best et al.	
	78	8301833	B1	2012-10-30	Chen et al.	
	79	8407395	B2	2013-03-26	Kim et al.	
	80	8412879	B2	2013-04-02	Chang et al.	
	81	8516187	B2	2013-08-20	Chen et al.	
	82	8671243	B2	2014-03-11	Chen et al.	
	83	8677060	B2	2014-03-18	Chen et al.	
	84	8874831	B2	2014-10-28	Lee et al.	
	85	8880791	B2	2014-11-04	Chen et al.	

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	Attorney Docket Number	0016.001000G

	86	8904098	B2	2014-12-02	Amidi et al.	
	87	8904099	B2	2014-12-02	Chen et al.	
	88	9043677	B2	2015-05-26	Kong et al.	
	89	9158684	B2	2015-10-13	Lee et al.	
	90	9361250	B2	2016-06-07	Shan et al.	
	91	9436600	B2	2016-09-06	Lee	Entire Document
	92	9921762	B2	2018-03-20	Amidi et al.	Entire Document
	93	9928186	B2	2018-03-27	Lee et al.	Entire Document

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20130086309	A1	2013-04-04	Lee et al.	

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	2	20130254456	A1	2013-09-26	Chen et al.	
	3	20130254497	A1	2013-09-26	Chen et al.	
	4	20140032820	A1	2014-01-30	Harasawa et al.	
	5	20140059170	A1	2014-02-27	Gasparakis et al.	
	6	20140156919	A1	2014-06-05	Chen et al.	
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	8	20150058701	A1	2015-02-26	Xing et al.	

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	First Named Inventor	Hyun Lee
	Art Unit	2131
	Examiner Name	Hashem FARROKH
	Attorney Docket Number	0016.001000G

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	~~1~~	~~Webster's II New College Dictionary, Houghton Mifflin Company, Boston, MA, 2001, pp. 259, 1115, 2 pages.~~	
	~~2~~	~~Wong, A. "The BIOS Optimization Guide", Adrian's Rojak Pot, Rev. 6.2, 1998-2001, 67 pages.~~	

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EXAMINER SIGNATURE

Examiner Signature	/HASHEM FARROKH/	Date Considered	12/21/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Art Unit	2131
	Examiner Name	Hashem FARROKH
	Attorney Docket Number	0016.001000G

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2020-06-01
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	149	((transfer$3 or cop$4 or transmi$5 or retriev$3 or read$3) near5 DRAM near5 (flash or non$1volatile)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:35
L2	1,316	Lee-Hyun.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:35
L3	72	Chen-Chi-She.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:35
L4	72	Solomon-Jeffrey-C.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:35
L5	33	Milton-Scott-H.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:35
L6	36	Bhakta-Jayesh.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:35

L7	0	L1 and (L2 or L3 or L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:35
L9	11,512	(transfer$4 or cop$4 or transmi$5 or mov$3) with data with (non$1volatile or flash or SSD or NVM) with (volatile or ?RAM or ?DRAM memory).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:42
L10	34	L9 and (L2 or L3 or L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:43
L11	11,512	((transfer$4 or cop$4 or transmi$5 or mov$3) with data with (non$1volatile or flash or SSD or NVM) with (volatile or ?RAM or ?DRAM memory)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:47
L12	477	(((transfer$4 or cop$4 or transmi$5 or mov$3) with data with (non$1volatile or flash or SSD or NVM) with (volatile or ?RAM or ?DRAM memory)) and ((determin$3 or check$3 or judg$3 or identif$4) with whether with data with (stored or recid$3 or located or recorded) with (non$1volatile or flash or SSD or NVM) with (volatile or ?RAM or ?DRAM memory))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:53
L13	0	12 and (L2 or L3 or L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:54
L14	1,318	((determin$3 or check$3 or judg$3 or identif$4) with whether with data with (stored or recid$3 or located or recorded) with (non$1volatile or flash	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2020/12/29 15:55

		or SSD or NVM) with (volatile or ?RAM or ?DRAM memory)).clm.	JPO; DERWENT; IBM_TDB			
L15	0	14 and (L2 or L3 or L4 or L5 or L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 15:56
L17	213	NETLIST.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 16:04
L18	21	9 and 17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 16:05
L19	120,401	(transfer$4 or cop$4 or transmi$5 or mov$3) with data with (non$1volatile or flash or SSD or NVM) with (volatile or ?RAM or ?DRAM memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 16:11
L20	4,838	((determin$3 or check$3 or judg$3 or identif$4) with whether with data with (stored or recid$3 or located or recorded) with (non$1volatile or flash or SSD or NVM) with (volatile or ?RAM or ?DRAM memory))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 16:17
L21	12,108	((transfer$3 or cop$4 or transmi$5 or retriev$3 or read$3) near5 DRAM near5 (flash or non$1volatile))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 16:22
L22	7,218	L21 AND ((G06F12/0246 OR G06F3/0685 OR G06F12/0638 OR G06F13/28 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G11C7/1072).CPC. OR (1/1 OR	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/29 16:22

		711/110).CCLS. OR (G06F3/06 OR G06F12/02 OR G06F13/42 OR G06F12/06 OR G06F13/28 OR G06F13/40 OR G06F1/18 OR G11C7/10).IPCR.)	DERWENT; IBM_TDB			
S181	3	"20180059966".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 10:43
S182	0	S181 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 10:43
S183	803	hybrid near3 ((memory or storage) near2 controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 10:44
S184	115	S183 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 10:45
S185	0	S184 and ((double adj data adj rate) near5 (command or instruction or request))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 10:47
S186	0	S184 and (((double adj data adj rate) or DDR) near5 (command or instruction or request))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 10:49
S187	2,713	(((double adj data adj rate) or DDR) near5 (command or instruction or request))	US-PGPUB; USPAT; USOCR;	OR	ON	2020/12/21 10:49

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S188	446	S187 and 711/$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 10:50
S189	49	S188 and 711/103.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 10:51
S190	6	S189 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 10:51
S191	6	S190 and ?DRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 10:54
S192	1	S191 and DRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 10:57
S193	18,371	DRAM with SSD	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 11:13
S194	170	S193 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2020/12/21 11:13

			JPO; DERWENT; IBM_TDB			
S195	0	S187 and S194	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 11:14
S196	45	S194 and (DDR or DDR2 or DDR3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 11:15
S198	44	S184 and (DDR or DDR2 or DDR3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 11:21
S199	39	S198 and (non$1volatile or flash or SSD)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 11:24
S200	165,711	(DRAM near2 (cache or buffer or memory)) with (SSD or non$1volatile OR flash)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 11:29
S201	25,503	S200 and (DDR or DDR2 or DDR3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 11:30
S202	2,006	S201 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/21 11:30

			DERWENT; IBM_TDB			
S203	19	S187 and S202	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 11:31
S204	3	S203 and host	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 11:48
S205	59	("2043099" "3562555" "3916390" "4234920" "4420821" "4449205" "4882709" "4965828").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:01
S206	44	("5430742" "5490155" "5519663" "5519831" "5563839" "5577213" "5619644" "5675725" "5799200" "5813029" "5870350").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:03
S207	49	("5874995" "5890192" "5953215" "5991885" "6023421" "6023421" "6026465" "6065092" "6112310" "6145068" "6158015" "6199142").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:06
S208	45	("6216247" "6269382" "6336174" "6336176" "6363450" "6421279" "6459647" "6487102" "6487623" "6571244" "6614685").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:09
S209	32	("6658507" "6691209" "6693840" "6721860" "6721860" "6769081" "6799241" "6799244" "6810513" "6816982" "68339774" "6944042").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/21 15:13

			DERWENT; IBM_TDB			
S210	42	("6948029" "6952368" "7053470" "7062618" "7089412" "7102391" "7111142" "7136978" "7155627" "7200021" "7234099").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:15
S211	51	("7353325" "7409491" "7409590" "7411859" "7421552" "7467251" "7519754" "7600142" "7716411" "7818488" "7873750").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:18
S212	64	("8086955" "8102614" "8233303" "8301833" "8407395" "8412879" "8516187" "8671243" "8677060" "8874831" "8880791").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:20
S213	47	("8904098" "8904099" "9043677" "9158684" "9361250" "9436600" "9921762" "9928186" "20130086309").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:23
S214	17	("15934416" "20130254456" "20130254497" "20140032820" "20140059170" "20140156919" "20140156920" "20150058701").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:24
S215	21,766	??DRAM and (SSD or non$1volatile or flash)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:26
S216	1	S215 and (S205 or S206 or S207 or S208 or S209 or S210 or S211 or S212 or S213 or S214)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/21 15:27

			DERWENT; IBM_TDB			
S217	2,433	((double$1data adj rate) or DDR) near5 (command or instruction or request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:46
S218	103	(determin$3 or check or judg or identif$4) near5 (whether or "if") near5 data near5 stored near5 ((dynamic adj random adj access adj memory) or DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:50
S219	195	(determin$3 or check$3 or judg$3 or identif$4) near5 (whether or "if") near5 data near5 (stored or recorded or written or saved or ready or maintained) near5 ((dynamic adj random adj access adj memory) or DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:52
S220	63	S219 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:53
S221	0	S217 and S220	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:53
S222	25	S220 and (SSD or non$1volatile or flash)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/21 15:55
S223	521	(DDR near2 DIMM) same (SSD or flash or non$1volatile OR NVM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/22 08:47

			DERWENT; IBM_TDB			
S224	14	S223 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 08:48
S225	1,083	(DDR near2 DIMM) and (SSD or flash or non$1volatile OR NVM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 08:52
S226	160	S225 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 08:52
S227	146	S226 not S224	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 08:52
S230	1,363	(miss$1hit or miss$3) near5 ((dynamic adj random adj access adj memory) or DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 09:04
S231	703	S230 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 09:04
S232	269	S231 and (SSD or flash or non$1volatile OR NVM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/22 09:05

			DERWENT; IBM_TDB			
S233	17	S231 and 711/103.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 09:06
S234	0	S232 and (DDR near5 (command or instruction or request))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 09:09
S235	70	S232 and DDR	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 09:09
S236	347	(miss$1hit or miss$3) near5 (((dynamic adj random adj access adj memory) or DRAM) near2 cache)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 09:12
S237	181	S236 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 09:13
S238	35	S237 and (SSD or flash or non$1volatile OR NVM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 09:13
S239	2	(?DRAM adj cache) with ((back$1up or main) near2 (SSD or NVM or flash or non$volatile))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/22 09:41

			DERWENT; IBM_TDB			
S240	40	(?DRAM adj cache) with (SSD or NVM or flash or non$volatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 09:43
S241	15	S240 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 09:44
S242	27,219	DDR near5 (access$3 or command or instruction or request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 10:49
S243	254	(?DRAM adj cache) and (SSD or NVM or flash or non$volatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 10:50
S244	2	S242 and S243	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 10:50
S245	165,736	(?DRAM) and (SSD or NVM or flash or non$volatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 10:51
S246	8,568	S242 and S245	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/22 10:51

			DERWENT; IBM_TDB			
S247	1,484	S246 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 10:51
S248	0	S247 and (?DRAM near5 miss$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 10:52
S249	5	S247 and (?DRAM near5 cache)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 10:53
S250	174	(((double adj data adj rate) or DDR) near5 (protocol or method)) near5 access$3 near5 ?DRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 11:39
S251	84	S250 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 11:40
S252	7	S251 and (SSD or NVM or flash or non$volatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/22 11:45
S253	25	"12240916"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/22 12:28

			DERWENT; IBM_TDB			
S256	2,381	(determin$3 or check$3 or judg$3 or identif$4) near5 (whether or "if") near5 data near5 (stored or recorded or written or saved or ready or maintained or ready) near5 (((dynamic adj random adj access adj memory) or ?DRAM) or (SSD OR flash or non$volatile or NVM))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/23 10:45
S257	622	S256 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/23 10:46
S258	17	S257 and ((double adj data adj rate) or DDR)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/23 10:48
S259	53	(determin$3 or check$3 or judg$3 or identif$4) near5 (whether or "if") near5 data near5 (stored or recorded or written or saved or ready or maintained or ready) near5 ((dynamic adj random adj access adj memory) or ?DRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/23 10:52
S260	2,330	(determin$3 or check$3 or judg$3 or identif$4) near5 (whether or "if") near5 data near5 (stored or recorded or written or saved or ready or maintained or ready) near5 (SSD OR flash or non$volatile or NVM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/23 10:54
S261	2	S259 and S260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/23 10:56
S262	32	S259 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/23 10:56

			DERWENT; IBM_TDB			
S263	1,369	((double adj data adj rate) or DDR) adj (protocol or standard)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/23 15:08
S264	702	S263 and (DDR2 or DDR3 or DDR4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/23 15:10
S265	26	S264 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/23 15:10
S266	3	S265 and (SSD or NVM or flash or non$volatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/23 15:12
S267	9,155	((dual$1inline adj memory adj module) or DIMM) same (flash or non$1volatile or SSD)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/24 17:57
S268	788	S267 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/24 17:59
S269	14	S268 and 711/103.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/24 17:59

			DERWENT; IBM_TDB			
S270	1,983	((memory adj controller adj hub) or MCH) and ((((dual adj inline) or dual$1inline) adj memory adj module) or DIMM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 12:42
S271	9	S270 and (transparent adj operation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 12:44
S272	0	S271 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 12:44
S273	33,899	((((dual adj inline) or dual$1inline) adj memory adj module) or DIMM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 12:45
S274	395	S270 and (transparen$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 12:45
S275	16	S274 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 12:46
S276	57	((((dual adj inline) or dual$1inline) adj memory adj module) or DIMM) with transparent	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/26 13:03

			DERWENT; IBM_TDB			
S277	30	S276 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:03
S278	20	S277 and DDR	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:03
S279	0	(?DRAM$1flash or (?DRAM adj flash)) near2 hybrid	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:16
S280	40	(flash$1?DRAM or (?DRAM near1 flash)) near2 hybrid	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:18
S281	0	S280 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:18
S282	40	(flash$1?DRAM or (?DRAM near1 (flash or non$1volatile or SSD))) near2 hybrid	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:19
S283	1	((((dual adj inline) or dual$1inline) adj memory adj module) or DIMM) same transparent same ((memory adj controller adj hub) or MCH)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/26 13:21

			DERWENT; IBM_TDB			
S284	394	((((dual adj inline) or dual$1inline) adj memory adj module) or DIMM) and transparent and ((memory adj controller adj hub) or MCH)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:24
S285	16	S284 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:25
S289	21	controller same transparent same ((memory adj controller adj hub) or MCH)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:28
S290	29	(DIMM adj2 controller) and transparent and ((memory adj controller adj hub) or MCH)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:28
S291	128	(module near2 controller) and transparent and ((memory adj controller adj hub) or MCH)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:29
S292	1	S289 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:29
S293	4	S290 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/26 13:31

			DERWENT; IBM_TDB			
S294	10	S291 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:32
S295	1,783	((memory adj controller adj hub) or MCH) and ((((dual adj inline) or dual$1inline) adj memory adj module) or DIMM) and (flash or non$1volatile or SSD)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:36
S296	279	S295 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:37
S297	8	S296 and transparen$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/26 13:38
S298	1,373	((double adj data adj rate) or DDR) adj (protocol or standard)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/27 12:26
S299	704	S298 and (DDR2 or DDR3 or DDR4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/27 12:26
S300	26	S299 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/27 12:26

			DERWENT; IBM_TDB			
S301	20	S300 and DIMM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/27 12:26
S302	3	S301 and flash	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/27 12:28
S303	25	(block adj address adj field) and (page adj address adj field)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 11:51
S304	6	S303 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 11:52
S305	2,143	(block adj address) with (page adj address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 11:55
S306	276	S305 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 11:56
S307	24	S306 and ?DRAM and flash	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/28 11:56

			DERWENT; IBM_TDB			
S308	178	((map$4 or translat$3 or conver$4) near2 table) with (block adj address) with (page adj address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 12:03
S309	16	S308 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 12:04
S310	0	(?DRAM adj (address or memory) adj space) near5 ((flash or non$1volatile) adj (address or memory) adj space)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 14:02
S311	785	(?DRAM adj (address or memory)) near5 ((flash or non$1volatile) adj (address or memory))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 14:06
S312	6	(?DRAM adj (address)) near5 ((flash or non$1volatile) adj (address))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 14:07
S313	2	S312 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 14:07
S314	0	(map$4 or translat$3 or conver$4) near5 (?DRAM adj (address)) near5 ((flash or non$1volatile) adj (address))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/28 14:09

			DERWENT; IBM_TDB			
S315	12	(map$4 or translat$3 or conver$4) near5 ((volatile or RAM or ?DRAM) adj (address)) near5 ((flash or non$1volatile or SSD) adj (address))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 14:11
S316	1	S315 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 14:12
S317	0	(DDR adj address) near5 ((flash or non$1volatile or SSD) adj address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 15:07
S320	210	((DDR or ?DRAM or volatile) adj2 address) near5 ((flash or non$1volatile or SSD) adj address)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 15:11
S321	48	S320 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 15:12
S322	2	S321 and (?DRAM near2 cache)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/28 15:38
S323	48	S320 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/12/28 15:41

			DERWENT; IBM_TDB			
S324	2	"20050185472".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 09:38
S325	1	S324 and (SDRAM near5 cach$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/12/29 09:39

12/29/2020 4:24:37 PM
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/934,416	03/23/2018	Hyun Lee	0016.001000G	2728

151145 7590 07/21/2021

Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2135	

NOTIFICATION DATE	DELIVERY MODE
07/21/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

khaled@shamimessinger.com
mike@shamimessinger.com
stephanie@shamimessinger.com

Notice of Abandonment	Application No. 15/934,416	Applicant(s) Lee et al.
	Examiner HASHEM FARROKH	Art Unit 2135

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. ☑ Applicant's failure to timely file a proper reply to the Office letter mailed on 01 January 2021.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☐ A proposed reply was received on _____, but it does not constitute a proper reply under 37 CFR 1.113 to the final rejection. (A proper reply under 37 CFR 1.113 to a final rejection consists only of:(1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) if this is utility or plant application, a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. Note that RCEs are not permitted in design applications.)
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a *bona fide* attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 8 below).
   (d) ☑ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $ _____ is insufficient. A balance of $ _____ is due.
   The issue fee required by 37CFR 1.18 is $ _____ . The publication fee, if required by 37 CFR 1.18(d), is $ _____ .
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record or other party authorized under 37 CFR 1.33 (b). See 37 CFR 1.138(b).

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34) upon the filing of a continuing application.

6. ☐ The decision by the Patent Trial and Appeal Board rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☐ The dismissal of the appeal in an application having no allowed claims. (When an appeal is dismissed in an application having no allowed claims the application stands abandoned. See MPEP 1215.04 subsections I-V for an explanation of the reasons why an appeal is dismissed.)

8. ☑ The reason(s) below:

The Examiner made a telephone call to the applicant to inquire information regarding the status of the Applicant response to the final office action mailed 01/01/2021. The Examiner was informed that a reply will not be filed

/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	

Petitions to revive under 37 CFR 1.137, or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.