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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.040C1
	Application Number	
Title of Invention	NON-VOLATILE MEMORY MODULE	

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Application Information:

Title of the Invention	NON-VOLATILE MEMORY MODULE		
Attorney Docket Number	NETL.040C1	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
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Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☒	**Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	12/131873	2008-06-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
12/131873	non provisional of	60/941586	2007-06-01

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	Application Number	
Title of Invention	NON-VOLATILE MEMORY MODULE	

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Assignee 1

If the Assignee is an Organization check here. ☒

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Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature				Date (YYYY-MM-DD)	2008-09-29
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NON-VOLATILE MEMORY MODULE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, which claims the benefit of U.S. Provisional Application No. 60/941,586, filed June 1, 2007. Each of these applications is incorporated in its entirety by reference herein.

BACKGROUND

[0002] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the computer system to provide volatile memory to the computer system.

[0003] Volatile memory generally maintains stored information only when it is powered. Batteries have been used to provide power to volatile memory during power failures or interruptions. However, batteries may require maintenance, may need to be replaced, are not environmentally friendly, and the status of batteries can be difficult to monitor.

[0004] Non-volatile memory can generally maintain stored information while power is not applied to the non-volatile memory. In certain circumstances, it can therefore be useful to backup volatile memory using non-volatile memory.

SUMMARY

[0005] In certain embodiments, a memory system coupled to a computer system is provided which includes a volatile memory subsystem, a non-volatile memory subsystem, and a controller operatively coupled to the non-volatile memory subsystem. The memory system can also include at least one circuit configured to selectively operatively decouple the controller from the volatile memory subsystem.

[0006] In some embodiments, a power module for providing a plurality of voltages to a memory system is described. The power module includes non-volatile and volatile memory, and the plurality of voltages include at least a first voltage and a second

voltage. The power module of certain embodiments includes an input providing a third voltage to the power module and a voltage conversion element configured to provide the second voltage to the memory system. The power module also includes a first power element configured to selectively provide a fourth voltage to the conversion element. The power module further includes a second power element configured to selectively provide a fifth voltage to the conversion element. The power module can be configured to selectively provide the first voltage to the memory system either from the conversion element or from the input.

[0007] The power module can be configured to be operated in at least three states in certain embodiments. In a first state, the first voltage is provided to the memory system from the input and the fourth voltage is provided to the conversion element from the first power element. In a second, state the fourth voltage is provided to the conversion element from the first power element and the first voltage is provided to the memory system from the conversion element. In a third state, the fifth voltage is provided to the conversion element from the second power element and the first voltage is provided to the memory system from the conversion element.

[0008] A method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems is provided in certain embodiments. The method includes, during a first condition, providing the first voltage to the memory system from an input power supply and providing the second voltage to the memory system from a first power subsystem. The method further includes detecting a second condition and, during the second condition, providing the first voltage and the second voltage to the memory system from the first power subsystem. The method also includes charging a second power subsystem and detecting a third condition. During the third condition, the method includes providing the first voltage and the second voltage to the memory system from the second power subsystem.

[0009] In certain embodiments, a method is provided for controlling a memory system operatively coupled to a host system and which includes a volatile memory subsystem and a non-volatile memory subsystem. The method can include operating the volatile memory subsystem at a first frequency when the memory system is in a first mode of

operation in which data is communicated between the volatile memory subsystem and the host system. In certain embodiments, the method further includes operating the non-volatile memory subsystem at a second frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem. The method can also include operating the volatile memory subsystem at a third frequency when the memory system is in the second mode of operation, the third frequency less than the first frequency.

[0010] In certain embodiments, a method is provided for controlling a memory system operatively coupled to a host system. The memory system includes a volatile memory subsystem and a non-volatile memory subsystem. In certain embodiments, the method includes communicating data words between the volatile memory subsystem and the host system when the memory system is in a first mode of operation. The method can further include transferring data words from the volatile memory subsystem to the non-volatile memory subsystem when the memory system is in a second mode of operation. Transferring each data word can include storing a first portion of the data word in a buffer, storing a second portion of the data word in the buffer, and writing the entire data word from the buffer to the non-volatile memory subsystem.

[0011] A memory system operatively coupled to a host system is provided in certain embodiments. The memory system can include a volatile memory subsystem and a non-volatile memory subsystem comprising at least 100 percent more storage capacity than does the volatile memory subsystem. The memory system includes a controller operatively coupled to the volatile memory subsystem and operatively coupled to the non-volatile memory subsystem, the controller configured to allow data to be communicated between the volatile memory subsystem and the host system when the memory system is operating in a first state and to allow data to be communicated between the volatile memory subsystem and the non-volatile memory subsystem when the memory system is operating in a second state.

[0012] A method of controlling a memory system operatively coupled to a host system is provided in certain embodiments. The memory system includes a volatile memory subsystem and a non-volatile memory subsystem. The method can include communicating data between the volatile memory subsystem and the host system when the memory system is

in a first mode of operation. The method of certain embodiments further includes storing a first copy of data from the volatile memory subsystem to the non-volatile memory subsystem at a first time when the memory system is in a second mode of operation. The method may further include restoring the first copy of data from the non-volatile memory subsystem to the volatile memory subsystem and erasing the first copy of data from the non-volatile memory subsystem. In certain embodiments, the method also includes storing a second copy of data from the volatile memory subsystem to the non-volatile memory subsystem at a second time when the memory system is in the second mode of operation, wherein storing the second copy begins before the first copy is completely erased from the non-volatile memory subsystem.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figure 1 is a block diagram of an example memory system compatible with certain embodiments described herein.

[0014] Figure 2 is a block diagram of an example memory module with ECC (error-correcting code) having a volatile memory subsystem with nine volatile memory elements and a non-volatile memory subsystem with five non-volatile memory elements in accordance with certain embodiments described herein.

[0015] Figure 3 is a block diagram of an example memory module having a microcontroller unit and logic element integrated into a single device in accordance with certain embodiments described herein.

[0016] Figures 4A-4C schematically illustrate example embodiments of memory systems having volatile memory subsystems comprising registered dual in-line memory modules in accordance with certain embodiments described herein.

[0017] Figure 5 schematically illustrates an example power module of a memory system in accordance with certain embodiments described herein.

[0018] Figure 6 is a flowchart of an example method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems.

[0019] Figure 7 is a flowchart of an example method of controlling a memory system operatively coupled to a host system and which includes at least 100 percent more storage capacity in non-volatile memory than in volatile memory.

[0020] Figure 8 schematically illustrates an example clock distribution topology of a memory system in accordance with certain embodiments described herein.

[0021] Figure 9 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including operating a volatile memory subsystem at a reduced rate in a back-up mode.

[0022] Figure 10 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments of a volatile memory subsystem of a memory system to a controller of the memory system.

[0023] Figure 11 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including backing up and/or restoring a volatile memory subsystem in slices.

DETAILED DESCRIPTION

[0024] Certain embodiments described herein include a memory system which can communicate with a host system such as a disk controller of a computer system. The memory system can include volatile and non-volatile memory, and a controller. The controller backs up the volatile memory using the non-volatile memory in the event of a trigger condition. Trigger conditions can include, for example, a power failure, power reduction, request by the host system, etc. In order to power the system in the event of a power failure or reduction, the memory system can include a secondary power source which does not comprise a battery and may include, for example, a capacitor or capacitor array.

[0025] In certain embodiments, the memory system can be configured such that the operation of the volatile memory is not adversely affected by the non-volatile memory or by the controller when the volatile memory is interacting with the host system. For example, one or more isolation devices may isolate the non-volatile memory and the controller from the volatile memory when the volatile memory is interacting with the host system and may allow communication between the volatile memory and the non-volatile memory when the data of the volatile memory is being restored or backed-up. This configuration generally

protects the operation of the volatile memory when isolated while providing backup and restore capability in the event of a trigger condition, such as a power failure.

[0026] In certain embodiments described herein, the memory system includes a power module which provides power to the various components of the memory system from different sources based on a state of the memory system in relation to a trigger condition (e.g., a power failure). The power module may switch the source of the power to the various components in order to efficiently provide power in the event of the power failure. For example, when no power failure is detected, the power module may provide power to certain components, such as the volatile memory, from system power while charging a secondary power source (e.g., a capacitor array). In the event of a power failure or other trigger condition, the power module may power the volatile memory elements using the previously charged secondary power source.

[0027] In certain embodiments, the power module transitions relatively smoothly from powering the volatile memory with system power to powering it with the secondary power source. For example, the memory system may power volatile memory with a third power source from the time the memory system detects that power failure is likely to occur until the time the memory system detects that the power failure has actually occurred.

[0028] In certain embodiments, the volatile memory system can be operated at a reduced frequency during backup and/or restore operations which can improve the efficiency of the system and save power. In some embodiments, during backup and/or restore operations, the volatile memory communicates with the non-volatile memory by writing and/or reading data words in bit-wise slices instead of by writing entire words at once. In certain embodiments, when each slice is being written to or read from the volatile memory the unused slice(s) of volatile memory is not active, which can reduce the power consumption of the system.

[0029] In yet other embodiments, the non-volatile memory can include at least 100 percent more storage capacity than the volatile memory. This configuration can allow the memory system to efficiently handle subsequent trigger conditions.

[0030] **Figure 1** is a block diagram of an example memory system 10 compatible with certain embodiments described herein. The memory system 10 can be coupled to a host

computer system and can include a volatile memory subsystem 30, a non-volatile memory subsystem 40, and a controller 62 operatively coupled to the non-volatile memory subsystem 40. In certain embodiments, the memory system 10 includes at least one circuit 52 configured to selectively operatively decouple the controller 62 from the volatile memory subsystem 30.

[0031] In certain embodiments, the memory system 10 comprises a memory module. The memory system 10 may comprise a printed-circuit board (PCB) 20. In certain embodiments, the memory system 10 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, or 8-GB. Other volatile memory capacities are also compatible with certain embodiments described herein. In certain embodiments, the memory system 10 has a non-volatile memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or 32-GB. Other non-volatile memory capacities are also compatible with certain embodiments described herein. In addition, memory systems 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the PCB 20 has an industry-standard form factor. For example, the PCB 20 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 20 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 20 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), mini-DIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. For example, in other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[0032] In certain preferred embodiments, the memory system 10 is in electrical communication with the host system. In other embodiments, the memory system 10 may communicate with a host system using some other type of communication, such as, for example, optical communication. Examples of host systems include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is

constrained or limited. The memory system 10 can be in communication with a disk controller of a computer system, for example. The PCB 20 can comprise an interface 22 that is configured to be in electrical communication with the host system (not shown). For example, the interface 22 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 22 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 10 and the host system. For example, the interface 22 can comprise a standard 240-pin DDR2 edge connector.

[0033] The volatile memory subsystem 30 comprises a plurality of volatile memory elements 32 and the non-volatile memory subsystem 40 comprises a plurality of non-volatile memory elements 42. Certain embodiments described herein advantageously provide non-volatile storage via the non-volatile memory subsystem 40 in addition to high-performance (e.g., high speed) storage via the volatile memory subsystem 30. In certain embodiments, the first plurality of volatile memory elements 32 comprises two or more dynamic random-access memory (DRAM) elements. Types of DRAM elements 32 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and synchronous DRAM (SDRAM). For example, in the block diagram of Figure 1, the first memory bank 30 comprises eight 64Mx8 DDR2 SDRAM elements 32. The volatile memory elements 32 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, volatile memory elements 32 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Volatile memory elements 32 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[0034] In certain embodiments, the second plurality of non-volatile memory elements 42 comprises one or more flash memory elements. Types of flash memory elements 42 compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC). For example, in the block diagram of Figure 1, the second memory bank 40 comprises 512 MB of flash

memory organized as four 128Mbx8 NAND flash memory elements 42. In addition, non-volatile memory elements 42 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Non-volatile memory elements 42 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[0035] **Figure 2** is a block diagram of an example memory module 10 with ECC (error-correcting code) having a volatile memory subsystem 30 with nine volatile memory elements 32 and a non-volatile memory subsystem 40 with five non-volatile memory elements 42 in accordance with certain embodiments described herein. The additional memory element 32 of the first memory bank 30 and the additional memory element 42 of the second memory bank 40 provide the ECC capability. In certain other embodiments, the volatile memory subsystem 30 comprises other numbers of volatile memory elements 32 (e.g., 2, 3, 4, 5, 6, 7, more than 9). In certain embodiments, the non-volatile memory subsystem 40 comprises other numbers of non-volatile memory elements 42 (e.g., 2, 3, more than 5).

[0036] Referring to Figure 1, in certain embodiments, the logic element 70 comprises a field-programmable gate array (FPGA). In certain embodiments, the logic element 70 comprises an FPGA available from Lattice Semiconductor Corporation which includes an internal flash. In certain other embodiments, the logic element 70 comprises an FPGA available from another vendor. The internal flash can improve the speed of the memory system 10 and save physical space. Other types of logic elements 70 compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element 70 is a custom device. In certain embodiments, the logic element 70 comprises various discrete electrical elements, while in certain other embodiments, the logic element 70 comprises one or more integrated circuits. **Figure 3** is a block diagram of an example memory module 10 having a microcontroller unit 60 and logic element 70 integrated into a single controller 62 in accordance with certain embodiments

described herein. In certain embodiments, the controller 62 includes one or more other components. For example, in one embodiment, an FPGA without an internal flash is used and the controller 62 includes a separate flash memory component which stores configuration information to program the FPGA.

[0037] In certain embodiments, the at least one circuit 52 comprises one or more switches coupled to the volatile memory subsystem 30, to the controller 62, and to the host computer (e.g., via the interface 22, as schematically illustrated by Figures 1-3). The one or more switches are responsive to signals (e.g., from the controller 62) to selectively operatively decouple the controller 62 from the volatile memory subsystem 30 and to selectively operatively couple the controller 62 to the volatile memory subsystem 30. In addition, in certain embodiments, the at least one circuit 52 selectively operatively couples and decouples the volatile memory subsystem 30 and the host system.

[0038] In certain embodiments, the volatile memory subsystem 30 can comprise a registered DIMM subsystem comprising one or more registers 160 and a plurality of DRAM elements 180, as schematically illustrated by **Figure 4A**. In certain such embodiments, the at least one circuit 52 can comprise one or more switches 172 coupled to the controller 62 (e.g., logic element 70) and to the volatile memory subsystem 30 which can be actuated to couple and decouple the controller 62 to and from the volatile memory subsystem 30, respectively. The memory system 10 further comprises one or more switches 170 coupled to the one or more registers 160 and to the plurality of DRAM elements 180 as schematically illustrated by Figure 4A. The one or more switches 170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 30 to the host system 150. In certain other embodiments, as schematically illustrated by **Figure 4B**, the one or more switches 174 are also coupled to the one or more registers 160 and to a power source 162 for the one or more registers 160. The one or more switches 174 can be selectively switched to turn power on or off to the one or more registers 160, thereby selectively operatively coupling the volatile memory subsystem 30 to the host system 150. As schematically illustrated by **Figure 4C**, in certain embodiments the at least one circuit 52 comprises a dynamic on-die termination (ODT) 176 circuit of the logic element 70. For example, the logic element 70 can comprise a dynamic ODT circuit 176 which selectively operatively couples and

decouples the logic element 70 to and from the volatile memory subsystem 30, respectively. In addition, and similar to the example embodiment of Figure 4A described above, the one or more switches 170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 30 to the host system 150.

[0039] Certain embodiments described herein utilize the non-volatile memory subsystem 40 as a flash "mirror" to provide backup of the volatile memory subsystem 30 in the event of certain system conditions. For example, the non-volatile memory subsystem 40 may backup the volatile memory subsystem 30 in the event of a trigger condition, such as, for example, a power failure or power reduction or a request from the host system. In one embodiment, the non-volatile memory subsystem 30 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition. In certain embodiments, the trigger condition occurs when the memory system 10 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. In various, a backup and/or restore operation may occur in reboot and/or non-reboot trigger conditions.

[0040] As schematically illustrated by Figures 1 and 2, in certain embodiments, the controller 62 may comprise a microcontroller unit (MCU) 60 and a logic element 70. In certain embodiments, the MCU 60 provides memory management for the non-volatile memory subsystem 40 and controls data transfer between the volatile memory subsystem 30 and the non-volatile memory subsystem 40. The MCU 60 of certain embodiments comprises a 16-bit microcontroller, although other types of microcontrollers are also compatible with certain embodiments described herein. As schematically illustrated by Figures 1 and 2, the logic element 70 of certain embodiments is in electrical communication with the non-volatile memory subsystem 40 and the MCU 60. The logic element 70 can provide signal level

translation between the volatile memory elements 32 (e.g., 1.8V SSTL-2 for DDR2 SDRAM elements) and the non-volatile memory elements 42 (e.g., 3V TTL for NAND flash memory elements). In certain embodiments, the logic element 70 is also programmed to perform address/address translation between the volatile memory subsystem 30 and the non-volatile memory subsystem 40. In certain preferred embodiments, 1-NAND type flash are used for the non-volatile memory elements 42 because of their superior read speed and compact structure.

[0041] The memory system 10 of certain embodiments is configured to be operated in at least two states. The at least two states can comprise a first state in which the controller 62 and the non-volatile memory subsystem 40 are operatively decoupled (e.g., isolated) from the volatile memory subsystem 30 by the at least one circuit 52 and a second state in which the volatile memory subsystem 30 is operatively coupled to the controller 62 to allow data to be communicated between the volatile memory subsystem 30 and the non-volatile memory subsystem 40 via the controller 62. The memory system 10 may transition from the first state to the second state in response to a trigger condition, such as when the memory system 10 detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up.

[0042] The memory system 10 may further comprise a voltage monitor 50. The voltage monitor circuit 50 monitors the voltage supplied by the host system via the interface 22. Upon detecting a low voltage condition (e.g., due to a power interruption to the host system), the voltage monitor circuit 50 may transmit a signal to the controller 62 indicative of the detected condition. The controller 62 of certain embodiments responds to the signal from the voltage monitor circuit 50 by transmitting a signal to the at least one circuit 52 to operatively couple the controller to the volatile memory system 30, such that the memory system 10 enters the second state. For example, the voltage monitor 50 may send a signal to the MCU 60 which responds by accessing the data on the volatile memory system 30 and by executing a write cycle on the non-volatile memory subsystem 40. During this write cycle, data is read from the volatile memory subsystem 30 and is transferred to the non-volatile memory subsystem 40 via the MCU 60. In certain embodiments, the voltage monitor circuit 50 is part of the controller 62 (e.g., part of the MCU 60) and the voltage monitor circuit 50

transmits a signal to the other portions of the controller 62 upon detecting a power threshold condition.

[0043] The isolation or operational decoupling of the volatile memory subsystem 30 from the non-volatile memory subsystem in the first state can preserve the integrity of the operation of the memory system 10 during periods of operation in which signals (e.g., data) are transmitted between the host system and the volatile memory subsystem 30. For example, in one embodiment during such periods of operation, the controller 62 and the non-volatile memory subsystem 40 do not add a significant capacitive load to the volatile memory system 30 when the memory system 10 is in the first state. In certain such embodiments, the capacitive load of the controller 62 and the non-volatile memory subsystem 40 do not significantly affect the signals propagating between the volatile memory subsystem 30 and the host system. This can be particularly advantageous in relatively high-speed memory systems where loading effects can be significant. In one preferred embodiment, the at least one circuit 52 comprises an FSA1208 Low-Power, Eight-Port, Hi-Speed Isolation Switch from Fairchild Semiconductor. In other embodiments, the at least one circuit 52 comprises other types of isolation devices.

[0044] Power may be supplied to the volatile memory subsystem 30 from a first power supply (e.g., a system power supply) when the memory system 10 is in the first state and from a second power supply 80 when the memory system 10 is in the second state. In certain embodiments, the memory system 10 is in the first state when no trigger condition (e.g., a power failure) is present and the memory system 10 enters the second state in response to a trigger condition. In certain embodiments, the memory system 10 has a third state in which the controller 62 is operatively decoupled from the volatile memory subsystem 30 and power is supplied to the volatile memory subsystem 30 from a third power supply (not shown). For example, in one embodiment the third power supply may provide power to the volatile memory subsystem 30 when the memory system 10 detects that a trigger condition is likely to occur but has not yet occurred.

[0045] In certain embodiments, the second power supply 80 does not comprise a battery. Because a battery is not used, the second power supply 80 of certain embodiments may be relatively easy to maintain, does not generally need to be replaced, and is relatively

environmentally friendly. In certain embodiments, as schematically illustrated by Figures 1-3, the second power supply 80 comprises a step-up transformer 82, a step-down transformer 84, and a capacitor bank 86 comprising one or more capacitors (e.g., double-layer capacitors). In one example embodiment, capacitors may take about three to four minutes to charge and about two minutes to discharge. In other embodiments, the one or more capacitors may take a longer time or a shorter time to charge and/or discharge. For example, in certain embodiments, the second power supply 80 is configured to power the volatile memory subsystem 30 for less than thirty minutes. In certain embodiments, the second power supply 80 may comprise a battery. For example, in certain embodiments, the second power supply 80 comprises a battery and one or more capacitors and is configured to power the volatile memory subsystem 30 for no more than thirty minutes.

[0046] In certain embodiments, the capacitor bank 86 of the second power supply 80 is charged by the first power supply while the memory system 10 is in the first state. As a result, the second power supply 80 is fully charged when the memory system 10 enters the second state. The memory system 10 and the second power supply 80 may be located on the same printed circuit board 20. In other embodiments, the second power supply 80 may not be on the same printed circuit board 20 and may be tethered to the printed circuit board 20, for example.

[0047] When operating in the first state, in certain embodiments, the step-up transformer 82 keeps the capacitor bank 86 charged at a peak value. In certain embodiments, the step-down transformer 84 acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 32 and 3.0V to the non-volatile flash memory elements 42) when operating in the second state (e.g., during power down). In certain embodiments, as schematically illustrated by Figures 1-3, the memory module 10 further comprises a switch 90 (e.g., FET switch) that switches power to the controller 62 the volatile memory subsystem 30, and the non-volatile memory subsystem 40 between the power from the second power supply 80 and the power from the first power supply (e.g., system power) received via the interface 22. For example, the switch 90 may switch from the first power supply to the second power supply 80 when the voltage monitor 50 detects a low voltage condition. The switch 90 of certain embodiments advantageously

ensures that the volatile memory elements 32 and non-volatile memory elements 42 are powered long enough for the data to be transferred from the volatile memory elements 32 and stored in the non-volatile memory elements 42. In certain embodiments, after the data transfer is complete, the switch 90 then switches back to the first power supply and the controller 62 transmits a signal to a the at least one circuit 50 to operatively decouple the controller 62 from the volatile memory subsystem 30, such that the memory system 10 re-enters the first state.

[0048] When the memory system 10 re-enters the first state, data may be transferred back from the non-volatile memory subsystem 40 to the volatile memory subsystem 30 via the controller 62. The host system can then resume accessing the volatile memory subsystem 30 of the memory module 10. In certain embodiments, after the memory system 10 enters or re-enters the first state (e.g., after power is restored), the host system accesses the volatile memory subsystem 30 rather than the non-volatile memory subsystem 40 because the volatile memory elements 32 have superior read/write characteristics. In certain embodiments, the transfer of data from the volatile memory bank 30 to the non-volatile memory bank 40, or from the non-volatile memory bank 40 to the volatile memory bank 30, takes less than one minute per GB.

[0049] In certain embodiments, the memory system 10 protects the operation of the volatile memory when communicating with the host-system and provides backup and restore capability in the event of a trigger condition such as a power failure. In certain embodiments, the memory system 10 copies the entire contents of the volatile memory subsystem 30 into the non-volatile memory subsystem 40 on each backup operation. Moreover, in certain embodiments, the entire contents of the non-volatile memory subsystem 40 are copied back into the volatile memory subsystem 30 on each restore operation. In certain embodiments, the entire contents of the non-volatile memory subsystem 40 are accessed for each backup and/or restore operation, such that the non-volatile memory subsystem 40 (e.g., flash memory subsystem) is used generally uniformly across its memory space and wear-leveling is not performed by the memory system 10. In certain embodiments, avoiding wear-leveling can decrease cost and complexity of the memory system 10 and can improve the performance of the memory system 10. In certain other embodiments, the entire

contents of the volatile memory subsystem 30 are not copied into the non-volatile memory subsystem 40 on each backup operation, but only a partial copy is performed. In certain embodiments, other management capabilities such as bad-block management and error management for the flash memory elements of the non-volatile memory subsystem 40 are performed in the controller 62.

[0050] The memory system 10 generally operates as a write-back cache in certain embodiments. For example, in one embodiment, the host system (e.g., a disk controller) writes data to the volatile memory subsystem 30 which then writes the data to non-volatile storage which is not part of the memory system 10, such as, for example, a hard disk. The disk controller may wait for an acknowledgment signal from the memory system 10 indicating that the data has been written to the hard disk or is otherwise secure. The memory system 10 of certain embodiments can decrease delays in the system operation by indicating that the data has been written to the hard disk before it has actually done so. In certain embodiments, the memory system 10 will still be able to recover the data efficiently in the event of a power outage because of the backup and restore capabilities described herein. In certain other embodiments, the memory system 10 may operated as a write-through cache or as some other type of cache.

[0051] **Figure 5** schematically illustrates an example power module 100 of the memory system 10 in accordance with certain embodiments described herein. The power module 100 provides power to the various components of the memory system 10 using different elements based on a state of the memory system 10 in relation to a trigger condition. In certain embodiments, the power module 100 comprises one or more of the components described above with respect to Figure 1. For example, in certain embodiments, the power module 100 includes the second power supply 80 and the switch 90.

[0052] The power module 100 provides a plurality of voltages to the memory system 10 comprising non-volatile and volatile memory subsystems 30, 40. The plurality of voltages comprises at least a first voltage 102 and a second voltage 104. The power module 100 comprises an input 106 providing a third voltage 108 to the power module 100 and a voltage conversion element 120 configured to provide the second voltage 104 to the memory system 10. The power module 100 further comprises a first power element 130 configured to

selectively provide a fourth voltage 110 to the conversion element 120. In certain embodiments, the first power element 130 comprises a pulse-width modulation power controller. For example, in one example embodiment, the first power element 130 is configured to receive a 1.8V input system voltage as the third voltage 108 and to output a modulated 5V output as the fourth voltage 110.

[0053] The power module 100 further comprises a second power element 140 can be configured to selectively provide a fifth voltage 112 to the conversion element 120. The power module 100 can be configured to selectively provide the first voltage 102 to the memory system 110 either from the conversion element 120 or from the input 106.

[0054] The power module 100 can be configured to be operated in at least three states in certain embodiments. In a first state, the first voltage 102 is provided to the memory system 10 from the input 106 and the fourth voltage 110 is provided to the conversion element 120 from the first power element 130. In a second state, the fourth voltage 110 is provided to the conversion element 120 from the first power element 130 and the first voltage 102 is provided to the memory system 10 from the conversion element 120. In the third state, the fifth voltage 112 is provided to the conversion element 120 from the second power element 140 and the first voltage 104 is provided to the memory system 10 from the conversion element 120.

[0055] In certain embodiments, the power module 100 transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third state upon detecting that the trigger condition has occurred. For example, the power module 100 may transition to the second state when it detects that a power failure is about to occur and transitions to the third state when it detects that the power failure has occurred. In certain embodiments, providing the first voltage 102 in the second state from the first power element 130 rather than from the input 106 allows a smoother transition from the first state to the third state. For example, in certain embodiments, providing the first voltage 102 from the first power element 130 has capacitive and other smoothing effects. In addition, switching the point of power transition to be between the conversion element 120 and the first and second power elements 130, 140 (e.g.,

the sources of the pre-regulated fourth voltage 110 in the second state and the pre-regulated fifth voltage 112 in the third state) can smooth out potential voltage spikes.

[0056] In certain embodiments, the second power element 140 does not comprise a battery and may comprise one or more capacitors. For example, as schematically illustrated in Figure 4, the second power element 140 comprises a capacitor array 142, a buck-boost converter 144 which adjusts the voltage for charging the capacitor array and a voltage/current limiter 146 which limits the charge current to the capacitor array 142 and stops charging the capacitor array 142 when it has reached a certain charge voltage. In one example embodiment, the capacitor array 142 comprises two 50 farad capacitors capable of holding a total charge of 4.6V. For example, in one example embodiment, the buck-boost converter 144 receives a 1.8V system voltage (first voltage 108) and boosts the voltage to 4.3V which is outputted to the voltage current limiter 146. The voltage/current limiter 146 limits the current going to the capacitor array 142 to 1A and stops charging the array 142 when it is charged to 4.3V. Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the second power element 140 may include alternative embodiments. For example, different components and/or different value components may be used. For example, in other embodiments, a pure boost converter may be used instead of a buck-boost converter. In another embodiment, only one capacitor may be used instead of a capacitor array 142.

[0057] The conversion element 120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 120 may comprise a plurality of sub-blocks 122, 124, 126 as schematically illustrated by Figure 4, which can provide more voltages in addition to the second voltage 104 to the memory system 10. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 10. For example, in one embodiment, sub-block 122 comprises a buck converter, sub-block 124 comprises a dual buck converter, and sub-block 126 comprises a buck-boost converter as schematically illustrated by Figure 4. Various other components for the sub-blocks 122, 124, 126 of the conversion element 120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 120 receives

as input either the fourth voltage 110 from the first power element 130 or the fifth voltage 112 from the second power element 140, depending on the state of the power module 100, and reduces the input to an appropriate amount for powering various components of the memory system. For example, the buck-converter of sub-block 122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 32 (e.g., DRAM), the non-volatile memory elements 42 (e.g., flash), and the controller 62 (e.g., an FPGA) in one embodiment. The sub-block 124 can provide the second voltage 104 as well as another reduced voltage 105 to the memory system 10. In one example embodiment, the second voltage 104 is 2.5V and is used to power the at least one circuit 52 (e.g., isolation device) and the other reduced voltage 105 is 1.2V and is used to power the controller 62 (e.g., FPGA). The sub-block 126 can provide yet another voltage 107 to the memory system 10. For example, the voltage 107 may be 3.3V and may be used to power both the controller 62 and the at least one circuit 52.

[0058] Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the conversion element 120 may include alternative embodiments. For example, there may be more or less sub-blocks which may comprise other types of converters (e.g., pure boost converters) or which may produce different voltage values. In one embodiment, the volatile memory elements 32 and non-volatile memory elements 42 are powered using independent voltages and are not both powered using the first voltage 102.

[0059] **Figure 6** is a flowchart of an example method 200 of providing a first voltage 102 and a second voltage 104 to a memory system 10 including volatile and non-volatile memory subsystems 30, 40. While the method 200 is described herein by reference to the memory system 10 schematically illustrated by Figures 1-4, other memory systems are also compatible with embodiments of the method 200. During a first condition, the method 200 at comprises providing the first voltage 102 to the memory system 10 from an input power supply 106 and providing the second voltage 104 to the memory system 10 from a first power subsystem in operational block 210. For example, in one embodiment, the first power subsystem comprises the first power element 130 and the voltage conversion element 120 described above with respect to Figure 4. In other embodiments, other first power subsystems are used.

[0060] The method 200 further comprises detecting a second condition in operational block 220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. During the second condition, the method 200 comprises providing the first voltage 102 and the second voltage 104 to the memory system 10 from the first power subsystem in an operational block 230. For example, referring to Figure 4, a switch 148 can be toggled to provide the first voltage 102 from the conversion element 120 rather than from the input power supply.

[0061] The method 200 further comprises charging a second power subsystem in operational block 240. In certain embodiments, the second power subsystem comprises the second power element 140 or another power supply that does not comprise a battery. For example, in one embodiment, the second power subsystem comprises the second power element 140 and the voltage conversion element 120 described above with respect to Figure 4. In other embodiments, some other second power subsystem is used.

[0062] The method 200 further comprises detecting a third condition in an operational block 250 and during the third condition, providing the first voltage 102 and the second voltage 104 to the memory system 10 from the second power subsystem 140 in an operational block 250. In certain embodiments, detecting the third condition comprises detecting that the trigger condition has occurred. The trigger condition may comprise various conditions described herein. In various embodiments, for example, the trigger condition comprises a power reduction, power failure, or system hang-up. The operational blocks of the method 200 may be performed in different orders in various embodiments. For example, in certain embodiments, the second power subsystem 140 is charged before detecting the second condition.

[0063] In certain embodiments, the memory system 10 comprises a volatile memory subsystem 30 and a non-volatile memory subsystem 40 comprising at least 100 percent more storage capacity than does the volatile memory subsystem. The memory system 10 also comprises a controller 62 operatively coupled to the volatile memory subsystem 30 and operatively coupled to the non-volatile memory subsystem 40. The controller 62 can be configured to allow data to be communicated between the volatile memory subsystem 30 and the host system when the memory system 10 is operating in a first state and to allow data to

be communicated between the volatile memory subsystem 30 and the non-volatile memory subsystem 40 when the memory system 10 is operating in a second state.

[0064] Although the memory system 10 having extra storage capacity of the non-volatile memory subsystem 40 has been described with respect to certain embodiments, alternative configurations exist. For example, in certain embodiments, there may be more than 100 percent more storage capacity in the non-volatile memory subsystem 40 than in the volatile memory subsystem 30. In various embodiments, there may be at least 200, 300, or 400 percent more storage capacity in the non-volatile memory subsystem 40 than in the volatile memory subsystem 30. In other embodiments, the non-volatile memory subsystem 40 includes at least some other integer multiples of the storage capacity of the volatile memory subsystem 30. In some embodiments, the non-volatile memory subsystem 40 includes a non-integer multiple of the storage capacity of the volatile memory subsystem 30. In one embodiment, the non-volatile memory subsystem 40 includes less than 100 percent more storage capacity than does the volatile memory subsystem 30.

[0065] The extra storage capacity of the non-volatile memory subsystem 40 can be used to improve the backup capability of the memory system 10. In certain embodiments in which data can only be written to portions of the non-volatile memory subsystem 40 which do not contain data (e.g., portions which have been erased), the extra storage capacity of the non-volatile memory subsystem 40 allows the volatile memory subsystem 30 to be backed up in the event of a subsequent power failure or other trigger event. For example, the extra storage capacity of the non-volatile memory subsystem 40 may allow the memory system 10 to backup the volatile memory subsystem 30 efficiently in the event of multiple trigger conditions (e.g., power failures). In the event of a first power failure, for example, the data in the volatile memory system 30 is copied to a first, previously erased portion of the non-volatile memory subsystem 40 via the controller 62. Since the non-volatile memory subsystem 40 has more storage capacity than does the volatile memory subsystem 30, there is a second portion of the non-volatile memory subsystem 40 which does not have data from the volatile memory subsystem 30 copied to it and which remains free of data (e.g., erased). Once system power is restored, the controller 62 of the memory system 10 restores the data to the volatile memory subsystem 30 by copying the backed-up data from the non-volatile

memory subsystem 40 back to the volatile memory subsystem 30. After the data is restored, the memory system 10 erases the non-volatile memory subsystem 40. While the first portion of the non-volatile memory subsystem 40 is being erased, it may be temporarily un-accessible.

[0066] If a subsequent power failure occurs before the first portion of the non-volatile memory subsystem 40 is completely erased, the volatile memory subsystem 30 can be backed-up or stored again in the second portion of the non-volatile memory subsystem 40 as described herein. In certain embodiments, the extra storage capacity of the non-volatile memory subsystem 40 may allow the memory system 10 to operate more efficiently. For example, because of the extra storage capacity of the non-volatile memory subsystem 40, the memory system 10 can handle a higher frequency of trigger events that is not limited by the erase time of the non-volatile memory subsystem 40.

[0067] **Figure 7** is a flowchart of an example method 300 of controlling a memory system 10 operatively coupled to a host system and which includes a volatile memory subsystem 30 and a non-volatile memory subsystem 40. In certain embodiments, the non-volatile memory subsystem 40 comprises at least 100 percent more storage capacity than does the volatile memory subsystem 30 as described herein. While the method 300 is described herein by reference to the memory system 10 schematically illustrated by Figures 1-3, the method 300 can be practiced using other memory systems in accordance with certain embodiments described herein. In an operational block 310, the method 300 comprises communicating data between the volatile memory subsystem 30 and the host system when the memory system 10 is in a first mode of operation. The method 300 further comprises storing a first copy of data from the volatile memory subsystem 30 to the non-volatile memory subsystem 40 at a first time when the memory system 10 is in a second mode of operation in an operational block 320.

[0068] In an operational block 330, the method 300 comprises restoring the first copy of data from the non-volatile memory subsystem 40 to the volatile memory subsystem 30. The method 300 further comprises erasing the first copy of data from the non-volatile memory subsystem 40 in an operational block 340. The method further comprises storing a second copy of data from the volatile memory subsystem 30 to the non-volatile memory

subsystem 40 at a second time when the memory system 10 is in the second mode of operation in an operational block 350. Storing the second copy begins before the first copy is completely erased from the non-volatile memory subsystem 40.

[0069] In some embodiments, the memory system 10 enters the second mode of operation in response to a trigger condition, such as a power failure. In certain embodiments, the first copy of data and the second copy of data are stored in separate portions of the non-volatile memory subsystem 40. The method 300 can also include restoring the second copy of data from the non-volatile memory subsystem 40 to the volatile memory subsystem 30 in an operational block 360. The operational blocks of method 300 referred to herein may be performed in different orders in various embodiments. For example, in some embodiments, the restoring the second copy of data to the volatile memory subsystem 30 at operational block 360 before the first copy of data is completely erased in the operational block 340.

[0070] **Figure 8** schematically illustrates an example clock distribution topology 400 of a memory system 10 in accordance with certain embodiments described herein. The clock distribution topology 400 generally illustrates the creation and routing of the clock signals provided to the various components of the memory system 10. A clock source 402 such as, for example, a 25 MHz oscillator, generates a clock signal. The clock source 402 may feed a clock generator 404 which provides a clock signal 406 to the controller 62, which may be an FPGA. In one embodiment, the clock generator 404 generates a 125 MHz clock signal 406. The controller 62 receives the clock signal 406 and uses it to clock the controller 62 master state control logic. For example, the master state control logic may control the general operation of an FPGA controller 62.

[0071] The clock signal 406 can also be input into a clock divider 410 which produces a frequency-divided version of the clock signal 406. In an example embodiment, the clock divider 410 is a divide by two clock divider and produces a 62.5 MHz clock signal in response to the 125 MHz clock signal 406. A non-volatile memory phase-locked loop (PLL) block 412 can be included (e.g., in the controller 62) which distributes a series of clock signals to the non-volatile memory subsystem 40 and to associated control logic. For example, a series of clock signals 414 can be sent from the controller 62 to the non-volatile memory subsystem 40. Another clock signal 416 can be used by the controller logic which is

dedicated to controlling the non-volatile memory subsystem 40. For example, the clock signal 416 may clock the portion of the controller 62 which is dedicated to generating address and/or control lines for the non-volatile memory subsystem 40. A feedback clock signal 418 is fed back into the non-volatile memory PLL block 412. In one embodiment, the PLL block 412 compares the feedback clock 418 to the reference clock 411 and varies the phase and frequency of its output until the reference 411 and feedback 418 clocks are phase and frequency matched.

[0072] A version of the clock signal 406 such as the backup clock signal 408 may be sent from the controller to the volatile memory subsystem 30. The clock signal 408 may be, for example, a differential version of the clock signal 406. As described herein, the backup clock signal 408 may be used to clock the volatile memory subsystem 30 when the memory system 10 is backing up the data from the volatile memory subsystem 30 into the non-volatile memory subsystem 40. In certain embodiments, the backup clock signal 408 may also be used to clock the volatile memory subsystem 30 when the memory system 10 is copying the backed-up data back into the volatile memory subsystem 30 from the non-volatile memory subsystem 40 (also referred to as restoring the volatile memory subsystem 30). The volatile memory subsystem 30 may normally be run at a higher frequency (e.g., DRAM running at 400MHz) than the non-volatile memory subsystem 40 (e.g., flash memory running at 62.5MHz) when communicating with the host system (e.g., when no trigger condition is present). However, in certain embodiments the volatile memory subsystem 30 may be operated at a reduced frequency (e.g., at twice the frequency of the non-volatile memory subsystem 40) without introducing significant delay into the system during backup operation and/or restore operations. Running the volatile memory subsystem 30 at the reduced frequency during a backup and/or restore operation may advantageously reduce overall power consumption of the memory system 10.

[0073] In one embodiment, the backup clock 408 and the volatile memory system clock signal 420 are received by a multiplexer 422, as schematically illustrated by Figure 7. The multiplexer 422 can output either the volatile memory system clock signal 420 or the backup clock signal 408 depending on the backup state of the memory system 10. For example, when the memory system 10 is not performing a backup or restore operation and is

communicating with the host system (e.g., normal operation), the volatile memory system clock signal 420 may be provided by the multiplexer 422 to the volatile memory PLL block 424. When the memory system 10 is performing a backup (or restore) operation, the backup clock signal 408 may be provided.

[0074] The volatile memory PLL block 424 receives the volatile memory reference clock signal 423 from the multiplexer 422 and can generate a series of clock signals which are distributed to the volatile memory subsystem 30 and associated control logic. For example, in one embodiment, the PLL block 424 generates a series of clock signals 426 which clock the volatile memory elements 32. A clock signal 428 may be used to clock control logic associated with the volatile memory elements, such as one or more registers (e.g., the one ore more registers of a registered DIMM). Another clock signal 430 may be sent to the controller 62. A feedback clock signal 432 is fed back into the volatile memory PLL block 424. In one embodiment, the PLL block 424 compares the feedback clock signal 432 to the reference clock signal 423 and varies the phase and frequency of its output until the reference clock signal 423 and the feedback clock signal 432 clocks are phase and frequency matched.

[0075] The clock signal 430 may be used by the controller 62 to generate and distribute clock signals which will be used by controller logic which is configured to control the volatile memory subsystem 30. For example, control logic in the controller 62 may be used to control the volatile memory subsystem 30 during a backup or restore operation. The clock signal 430 may be used as a reference clock signal for the PLL block 434 which can generate one or more clocks 438 used by logic in the controller 62. For example, the PLL block 424 may generate one or more clock signals 438 used to drive logic circuitry associated with controlling the volatile memory subsystem 30. In certain embodiments, the PLL block 434 includes a feedback clock signal 436 and operates in a similar manner to other PLL blocks described herein.

[0076] The clock signal 430 may be used as a reference clock signal for the PLL block 440 which may generate one or more clock signals used by a sub-block 442 to generate one or more other clock signals 444. In one embodiment, for example, the volatile memory subsystem 30 comprises DDR2 SDRAM elements and the sub-block 442 generates one or

more DDR2 compatible clock signals 444. A feedback clock signal 446 is fed back into the PLL block 440. In certain embodiments, the PLL block 440 operates in a similar manner to other PLL blocks described herein.

[0077] While described with respect to the example embodiment of Figure 7, various alternative clock distribution topologies are possible. For example, one or more of the clock signals have a different frequency in various other embodiments. In some embodiments, one or more of the clocks shown as differential signals are single ended signals. In one embodiment, the volatile memory subsystem 30 operates on the volatile memory clock signal 420 and there is no backup clock signal 408. In some embodiments, the volatile memory subsystem 30 is operated at a reduced frequency during a backup operation and not during a restore operation. In other embodiments, the volatile memory subsystem 30 is operated at a reduced frequency during a restore operation and not during a backup operation.

[0078] **Figure 9** is a flowchart of an example method 500 of controlling a memory system 10 operatively coupled to a host system. Although described with respect to the memory system 10 described herein with respect to Figures 1-3 and 7, the method 500 is compatible with other memory systems. The memory system 10 may include a clock distribution topology 400 similar to the one described above with respect to Figure 7 or another clock distribution topology. The memory system 10 can include a volatile memory subsystem 30 and a non-volatile memory subsystem 40.

[0079] In an operational block 510, the method 500 comprises operating the volatile memory subsystem 40 at a first frequency when the memory system 10 is in a first mode of operation in which data is communicated between the volatile memory subsystem 30 and the host system. In an operational block 520, the method 500 comprises operating the non-volatile memory subsystem 40 at a second frequency when the memory system 10 is in a second mode of operation in which data is communicated between the volatile memory subsystem 30 and the non-volatile memory subsystem 40. The method 500 further comprises operating the volatile memory subsystem 30 at a third frequency in an operational block 530 when the memory system 10 is in the second mode of operation. In certain embodiments, the memory system 10 is not powered by a battery when it is in the second mode of operation.

The memory system 10 may switch from the first mode of operation to the second mode of operation in response to a trigger condition. The trigger condition may be any trigger condition described herein such as, for example, a power failure condition. In certain embodiments, the second mode of operation includes both backup and restore operations as described herein. In other embodiments, the second mode of operation includes backup operations but not restore operations. In yet other embodiments, the second mode of operation includes restore operations but not backup operations.

[0080] The third frequency can be less than the first frequency. For example, the third frequency can be approximately equal to the second frequency. In certain embodiments, the reduced frequency operation is an optional mode. In yet other embodiments, the first, second and/or third frequencies are configurable by a user or by the memory system 10.

[0081] **Figure 10** schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 630, 640 of a volatile memory subsystem 30 of a memory system 10 to a controller 62 of the memory system 10. While the example of Figure 10 shows a topology including two DRAM segments 630, 640 for the purposes of illustration, each address location of the volatile memory subsystem 30 comprises more than the two segments in certain embodiments. The data lines 632, 642 from the first DRAM segment 630 and the second DRAM segment 640 of the volatile memory subsystem 30 are coupled to switches 650, 652 which are coupled to the controller 62 (e.g., logic element 70) of the memory system 10. The chip select lines 634, 644 and the self-refresh lines 636, 646 (e.g., CKe signals) of the first and second DRAM segments 630, 640, respectively, are coupled to the controller 62. In certain embodiments, the controller 62 comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem 30. In certain embodiments, the buffer is a first-in, first out buffer (FIFO). In certain embodiments, data slices from each DRAM segment 630, 640 comprise a portion of the volatile memory subsystem data bus. In one embodiment, for example, the volatile memory subsystem 30 comprises a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 640 may comprise the remaining 32 bits

of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.

[0082] In certain embodiments, the switches 650, 652 can each be selectively switched to selectively operatively couple the data lines 632, 642, respectively from the first and second DRAM segments 630, 640 to the controller 62. The chip select lines 634, 644 enable the first and second DRAM segments 630, 640, respectively, of the volatile memory subsystem 30, and the self-refresh lines 636, 646 toggle the first and second DRAM segments 630, 640, respectively, from self-refresh mode to active mode. In certain embodiments, the first and second DRAM segments 630, 640 maintain stored information but are not accessible when they are in self-refresh mode, and maintain stored information and are accessible when they are in active mode.

[0083] In certain embodiments, when the memory system 10 is backing up the volatile memory system 30, data slices from only one of the two DRAM segments 630, 640 at a time are sent to the controller 62. For example, when the first slice is being written to the controller 62 during a back-up, the controller 62 sends a signal via the CKe line 636 to the first DRAM segment 630 to put the first DRAM segment 630 in active mode. In certain embodiments, the data slice from the first DRAM segment 630 for multiple words (e.g., a block of words) is written to the controller 62 before writing the second data slice from the second DRAM segment 640 to the controller 62. While the first data slice is being written to the controller 62, the controller 62 also sends a signal via the CKe line 646 to put the second DRAM segment 640 in self-refresh mode. Once the first data slice for one word or for a block of words is written to the controller 62, the controller 62 puts the first DRAM segment 630 into self-refresh mode by sending a signal via the CKe line 636 to the first DRAM segment 640. The controller 62 also puts the second DRAM segment 640 into active mode by sending a signal via the CKe line 646 to the DRAM segment 640. The second slice for a word or for a block of words is written to the controller 62. In certain embodiments, when the first and second data slices are written to the buffer in the controller 62, the controller 62 combines the first and second data slices 630, 640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem

40. In certain embodiments, this process is called "slicing" the volatile memory subsystem 30.

[0084] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the non-volatile memory elements 42 write each backed-up data word to the controller 62 which writes a first slice of the data word to the volatile memory subsystem 30 and then a second slice of the data word to the volatile memory subsystem 30. In certain embodiments, slicing the volatile memory subsystem 30 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 30 during a backup operation.

[0085] **Figure 11** is a flowchart of an example method 600 of controlling a memory system 10 operatively coupled to a host system and which includes a volatile memory subsystem 30 and a non-volatile memory subsystem 40. Although described with respect to the memory system 10 described herein with respect to Figures 1-3 and 10, the method 600 is compatible with other memory systems. The method 600 comprises communicating data words between the volatile memory subsystem 40 and the host system when the memory system 10 is in a first mode of operation in an operational block 610. For example, the memory system 10 may be in the first mode of operation when no trigger condition has occurred and the memory system is not performing a backup and/or restore operation or is not being powered by a secondary power supply.

[0086] In an operational block 620, the method further comprises transferring data words from the volatile memory subsystem 30 to the non-volatile memory subsystem 40 when the memory system 10 is in a second mode of operation. In certain embodiments, each data word comprises the data stored in a particular address of the memory system 10. The memory system 10 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 622, storing a second portion of the data word in the buffer in an operational block 624, and writing the entire data word from the buffer to the non-volatile memory subsystem 40 in an operational block 626.

[0087] In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 62. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 62 which comprises an FPGA. The method 600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 62 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).

[0088] In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In certain other embodiments, the data word may comprise more than three portions.

[0089] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the non-volatile memory elements 40 write each backed-up data word to the controller 62 which writes a first portion of the data word to the volatile memory subsystem 30 and then a second portion of the data word to the volatile memory 30. In certain embodiments, slicing the volatile memory subsystem 30 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 30 during a backup operation.

[0090] The method 600 can advantageously provide significant power savings and can lead to other advantages. For example, in one embodiment where the volatile

memory subsystem 30 comprises DRAM elements, only the slice of the DRAM which is currently being accessed (e.g., written to the buffer) during a backup is configured in full-operational mode. The slice or slices that are not being accessed may be put in self-refresh mode. Because DRAM in self-refresh mode uses significantly less power than DRAM in full-operational mode, the method 600 can allow significant power savings. In certain embodiments, each slice of the DRAM includes a separate self-refresh enable (e.g., CKe) signal which allows each slice to be accessed independently.

[0091] In addition, the connection between the DRAM elements and the controller 62 may be as large as the largest slice instead of as large as the data bus. In the example embodiment, the connection between the controller 62 and the DRAM may be 40 bits instead of 72 bits. As a result, pins on the controller 62 may be used for other purposes or a smaller controller may be used due to the relatively low number of pin-outs used to connect to the volatile memory subsystem 30. In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem 30 and the controller 62 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.

[0092] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined in the appended claims.

WHAT IS CLAIMED IS:

1. A memory system coupled to a computer system, comprising:

a volatile memory subsystem;

a non-volatile memory subsystem;

a controller operatively coupled to the non-volatile memory subsystem;

at least one circuit configured to selectively operatively decouple the controller from the volatile memory subsystem.

2. The memory system of Claim 1, wherein the memory system is configured to be operated in at least two states, the at least two states comprising:

a first state in which the controller and the non-volatile memory subsystem are decoupled from the volatile memory subsystem by the at least one circuit; and

a second state in which the volatile memory subsystem is operatively coupled to the controller to allow data to be communicated between the volatile memory subsystem and the non-volatile memory subsystem via the controller.

3. The memory system of Claim 2, wherein power is supplied to the volatile memory subsystem from a first power supply when the memory system is in the first state and power is supplied to the volatile memory subsystem from a second power supply when the memory system is in the second state.

4. The memory system of Claim 3, wherein the second power supply does not comprise a battery.

5. The memory system of Claim 3, wherein the second power supply comprises one or more capacitors.

6. The memory system of Claim 5, wherein the second power supply comprises a battery and is configured to power the volatile memory subsystem for less than thirty minutes.

7. The memory system of Claim 5, wherein the one or more capacitors comprises one or more double layered capacitors.

8. The memory system of Claim 5, wherein the one or more capacitors are charged by the first power supply while the memory system is in the first state.

9. The memory system of Claim 3, further comprising a printed circuit board, wherein the second power supply and the memory system are located on the printed circuit board.

10. The memory system of Claim 3, wherein the at least two states further comprise a third state in which power is supplied to the volatile memory subsystem from a third power supply.

11. The memory system of Claim 2, wherein the controller and the non-volatile memory subsystem do not add a significant capacitive load to the volatile memory system when the memory system is in the first state.

12. The memory system of Claim 1, wherein the volatile memory subsystem comprises one or more DRAM memory elements.

13. The memory system of Claim 1, wherein the volatile memory subsystem comprises one or more SRAM memory elements.

14. The memory system of Claim 1, wherein the non-volatile memory subsystem comprises one or more flash memory elements.

15. The memory system of Claim 1, wherein the memory system is implemented on a memory module.

16. The memory system of Claim 1, wherein the at least one circuit comprise one or more switches coupled to the controller, to the volatile memory subsystem, and to the host computer.

17. The memory system of Claim 1, wherein the volatile memory subsystem comprises a registered DIMM comprising one or more registers and a plurality of DRAM elements, wherein the one or more registers are coupled to the computer system.

18. The memory system of Claim 17, wherein the at least one circuit comprise one or more switches coupled to the one or more registers and to the plurality of DRAM elements and configured to selectively operatively couple the volatile memory subsystem and to the computer system.

19. The memory system of Claim 17, wherein the one or more registers are coupled to the plurality of DRAM elements and the at least one circuit comprises one or more switches coupled to the one or more registers and to a power source for the one or more

registers, wherein the one or more switches are configured to selectively operatively couple the one or more registers to the power source for the one or more registers.

20. The memory system of Claim 1, wherein the non-volatile memory subsystem comprises at least 100 percent more storage capacity than does the volatile memory subsystem.

21. A power module for providing a plurality of voltages to a memory system comprising non-volatile and volatile memory, the plurality of voltages comprising at least a first voltage and a second voltage, the power module comprising:

an input providing a third voltage to the power module;

a voltage conversion element configured to provide the second voltage to the memory system;

a first power element configured to selectively provide a fourth voltage to the conversion element;

a second power element configured to selectively provide a fifth voltage to the conversion element, wherein the power module is configured to selectively provide the first voltage to the memory system either from the conversion element or from the input, wherein the power module is configured to be operated in at least three states comprising:

a first state in which the first voltage is provided to the memory system from the input and the fourth voltage is provided to the conversion element from the first power element;

a second state in which the fourth voltage is provided to the conversion element from the first power element and the first voltage is provided to the memory system from the conversion element;

a third state in which the fifth voltage is provided to the conversion element from the second power element and the first voltage is provided to the memory system from the conversion element.

22. The power module of Claim 21, wherein the first power element comprises a pulse-width modulation power controller.

23. The power module of Claim 21, wherein the second power element does not comprise a battery.

24. The power module of Claim 21, wherein the second power element comprises one or more capacitors.

25. The power module of Claim 24, wherein the second power element comprises a battery and is configured to power the volatile memory for less than thirty minutes.

26. The power module of Claim 21, wherein the conversion element comprises one or more buck converters.

27. The power module of Claim 21, wherein the conversion element comprises one or more buck-boost converters.

28. A method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems, the method comprising:

during a first condition, providing the first voltage to the memory system from an input power supply and providing the second voltage to the memory system from a first power subsystem;

detecting a second condition;

during the second condition, providing the first voltage and the second voltage to the memory system from the first power subsystem;

charging a second power subsystem;

detecting a third condition;

during the third condition, providing the first voltage and the second voltage to the memory system from the second power subsystem.

29. The method of Claim 28, wherein detecting the second condition comprises detecting that a trigger condition is likely to occur.

30. The method of Claim 29, wherein detecting the third condition comprises detecting that the trigger condition has occurred.

31. The method of Claim 28, wherein the trigger condition comprises a power reduction.

32. The method of Claim 28, wherein the trigger condition comprises a power failure.

33. The method of Claim 28, wherein the trigger condition comprises a system hang-up.

34. The method of Claim 28, wherein the first power subsystem comprises a pulse-width modulation power controller and a voltage conversion subsystem.

35. The method of Claim 28, wherein the second power subsystem does not comprise a battery.

36. The method of Claim 35, wherein the second power subsystem comprises one or more capacitors and the voltage conversion subsystem.

37. A method of controlling a memory system operatively coupled to a host system and which includes a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

operating the volatile memory subsystem at a first frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;

operating the non-volatile memory subsystem at a second frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and

operating the volatile memory subsystem at a third frequency when the memory system is in the second mode of operation, the third frequency less than the first frequency.

38. The method of Claim 37, wherein the third frequency is approximately equal to the second frequency.

39. The method of Claim 37, wherein the memory system is not powered by a battery when it is in the second mode of operation.

40. The method of Claim 7, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.

41. The method of Claim 40, wherein the trigger condition comprises a power failure condition.

42. The method of Claim 37, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.

43. A method of controlling a memory system operatively coupled to a host system and which includes a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

communicating data words between the volatile memory subsystem and the host system when the memory system is in a first mode of operation; and

transferring data words from the volatile memory subsystem to the non-volatile memory subsystem when the memory system is in a second mode of operation, wherein transferring each data word comprises:

storing a first portion of the data word in a buffer;

storing a second portion of the data word in the buffer; and

writing the entire data word from the buffer to the non-volatile memory subsystem.

44. The method of Claim 43, wherein the transferring each data word further comprises storing a third portion of each data word in the buffer.

45. A memory system operatively coupled to a host system, comprising:

a volatile memory subsystem;

a non-volatile memory subsystem comprising at least 100 percent more storage capacity than does the volatile memory subsystem; and

a controller operatively coupled to the volatile memory subsystem and operatively coupled to the non-volatile memory subsystem, the controller configured to allow data to be communicated between the volatile memory subsystem and the host system when the memory system is operating in a first state and to allow data to be communicated between the volatile memory subsystem and the non-volatile memory subsystem when the memory system is operating in a second state.

46. The memory system of Claim 45, wherein power is supplied to the volatile memory subsystem from a first power supply when the memory system is in the first state.

47. The memory system of Claim 46, wherein power is supplied to the volatile memory subsystem from a second power supply when the memory system is in the second state.

48. The memory system of Claim 47, wherein the second power supply does not comprise a battery.

49. The memory system of Claim 45, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem, the non-volatile memory subsystem, and the controller are located on the printed circuit board.

50. A method of controlling a memory system operatively coupled to a host system and which includes a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

communicating data between the volatile memory subsystem and the host system when the memory system is in a first mode of operation;

storing a first copy of data from the volatile memory subsystem to the non-volatile memory subsystem at a first time when the memory system is in a second mode of operation;

restoring the first copy of data from the non-volatile memory subsystem to the volatile memory subsystem;

erasing the first copy of data from the non-volatile memory subsystem; and

storing a second copy of data from the volatile memory subsystem to the non-volatile memory subsystem at a second time when the memory system is in the second mode of operation, wherein storing the second copy begins before the first copy is completely erased from the non-volatile memory subsystem.

51. The method of Claim 50, further comprising restoring the second copy of data from the non-volatile memory subsystem to the volatile memory subsystem.

52. The method of Claim 50, wherein the memory system enters the second mode of operation in response to a power failure.

53. The method of Claim 50, wherein the memory system is not powered by a battery when it is in the second mode of operation.

54. The method of Claim 50, wherein the first copy of data and the second copy of data are stored in separate portions of the non-volatile memory subsystem.

NON-VOLATILE MEMORY MODULE

ABSTRACT OF THE DISCLOSURE

Certain embodiments described herein include a memory system which can communicate with a host system such as a disk controller of a computer system. The memory system can include volatile and non-volatile memory and a controller which are configured such that the controller backs up the volatile memory using the non-volatile memory in the event of a trigger condition. In order to power the system in the event of a power failure or reduction, the memory system can include a secondary power source which is not a battery and may include, for example, a capacitor or capacitor array. The memory system can be configured such that the operation of the volatile memory is not adversely affected by the non-volatile memory or the controller when the volatile memory is interacting with the host system.

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Figure 1:

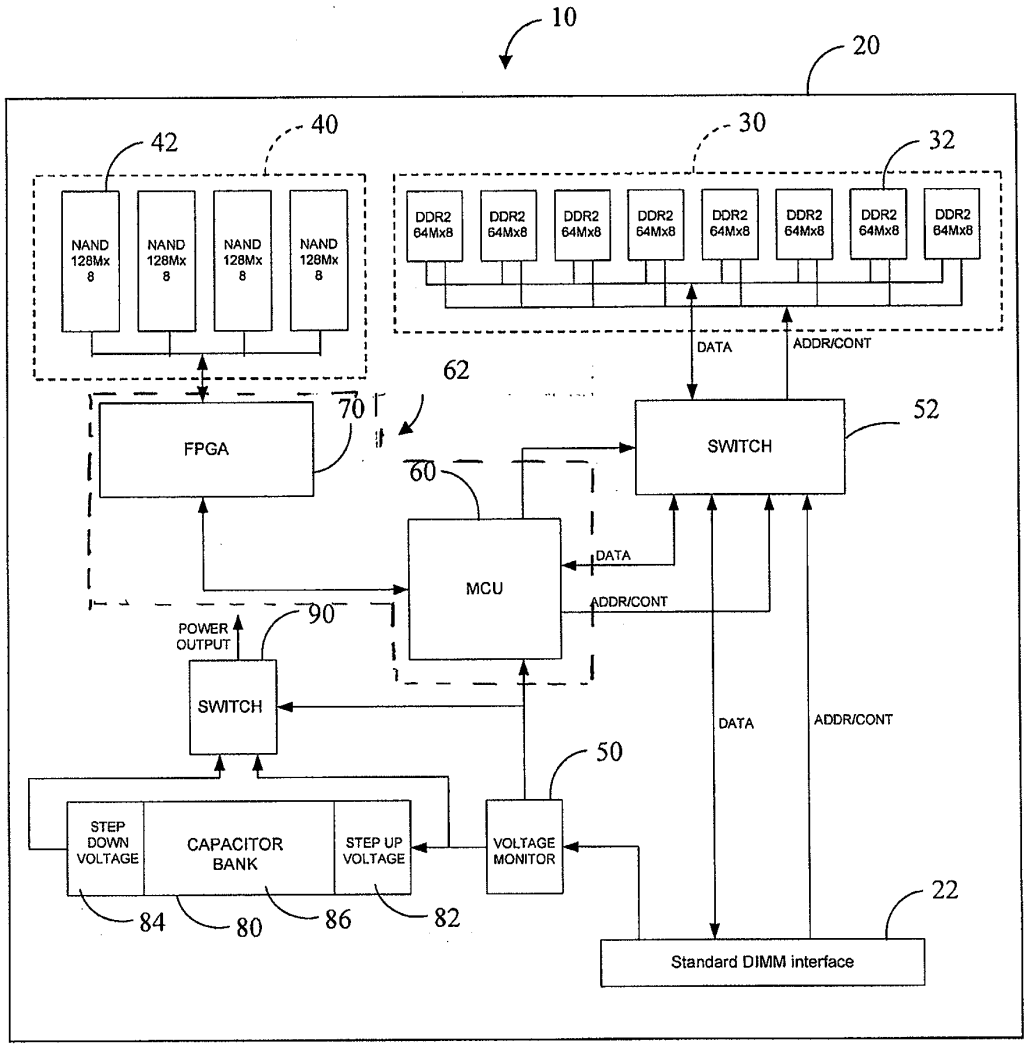

10
20
42
40
30
32
NAND 128Mx 8
NAND 128Mx 8
NAND 128Mx 8
NAND 128Mx 8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DATA
ADDR/CONT
62
70
FPGA
SWITCH
52
60
MCU
DATA
ADDR/CONT
POWER OUTPUT
90
SWITCH
DATA
ADDR/CONT
50
STEP DOWN VOLTAGE
CAPACITOR BANK
STEP UP VOLTAGE
VOLTAGE MONITOR
84
80
86
82
22
Standard DIMM interface

Figure 2:

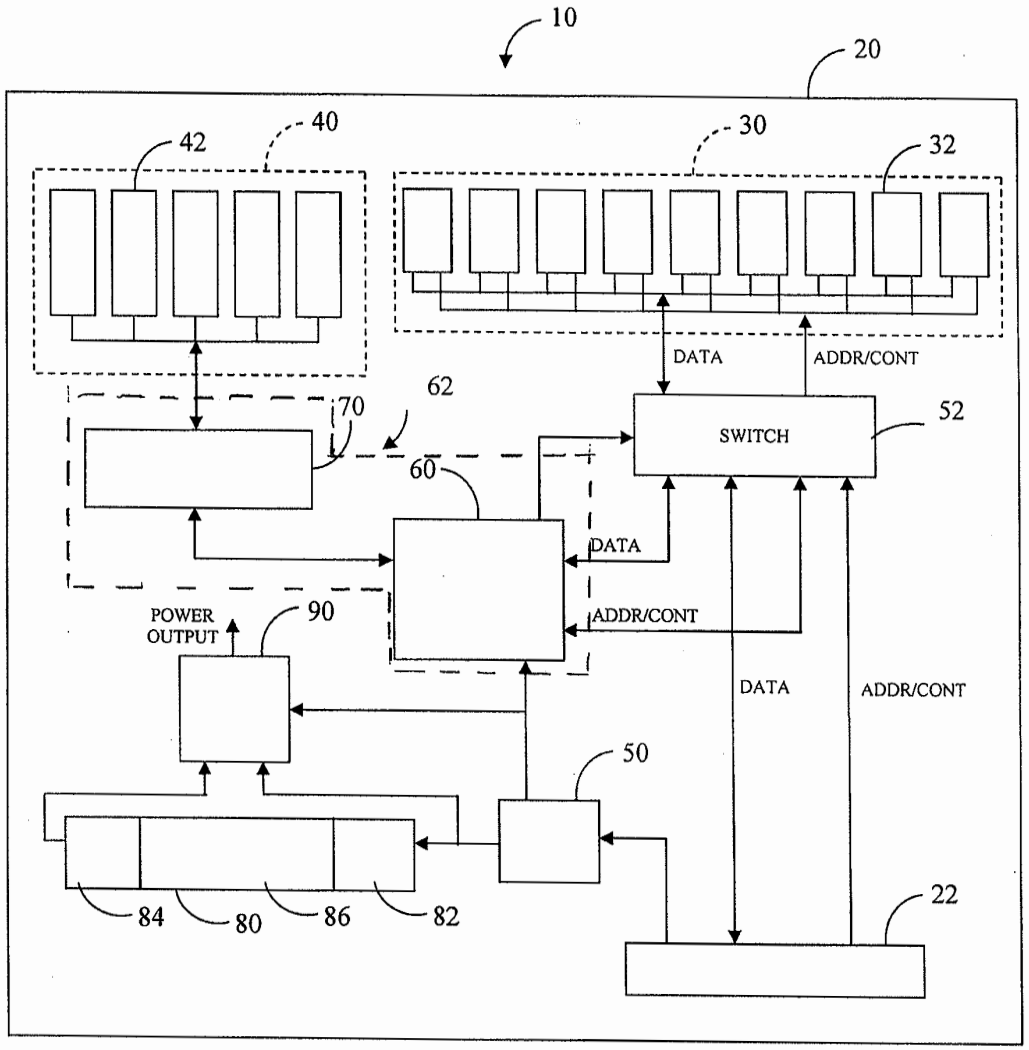

10
20
42
40
30
32
DATA
ADDR/CONT
62
70
SWITCH
52
60
DATA
POWER
OUTPUT
90
ADDR/CONT
DATA
ADDR/CONT
50
84
80
86
82
22

Figure 3:

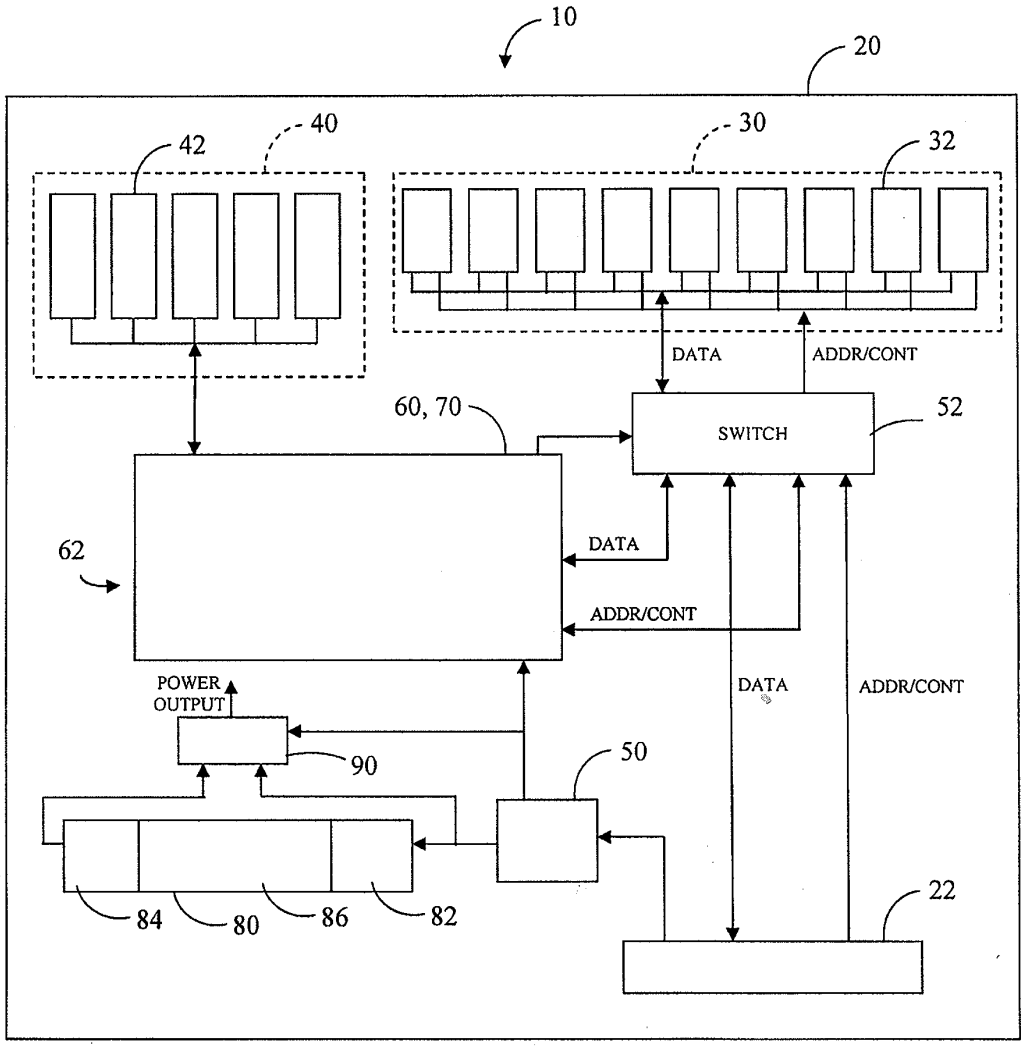

10
20
42
40
30
32
DATA
ADDR/CONT
60, 70
SWITCH
52
62
DATA
ADDR/CONT
POWER OUTPUT
DATA
ADDR/CONT
90
50
84
80
86
82
22

Figure 4A:

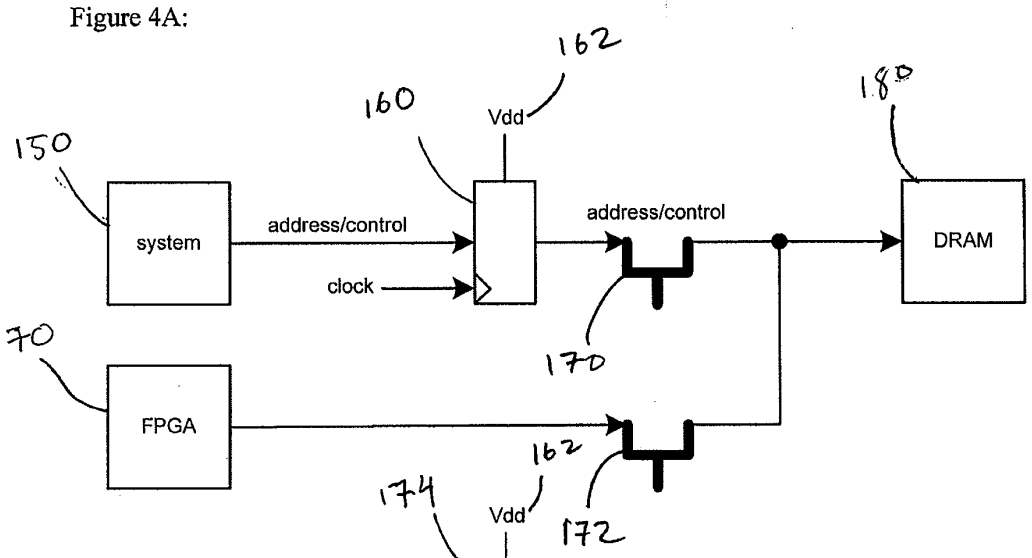


Figure 4B:

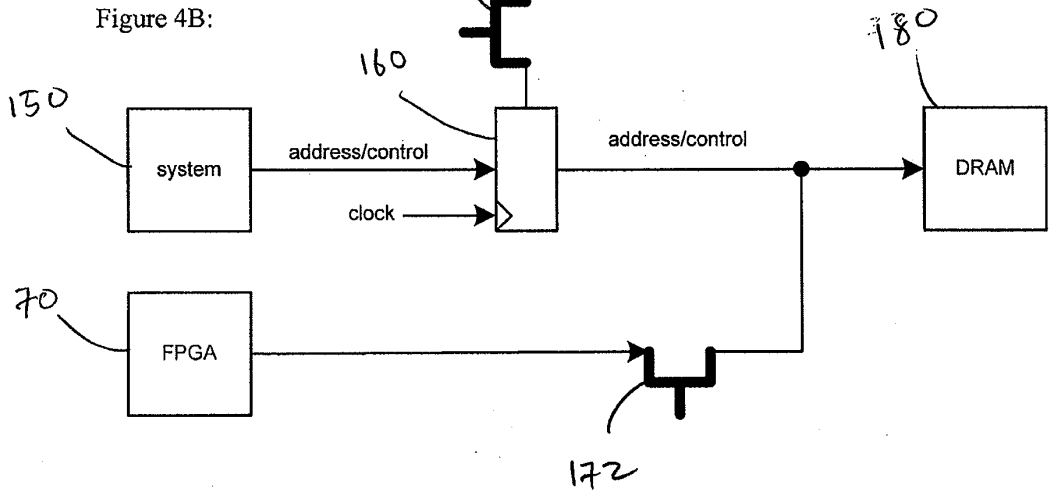


Figure 4C:

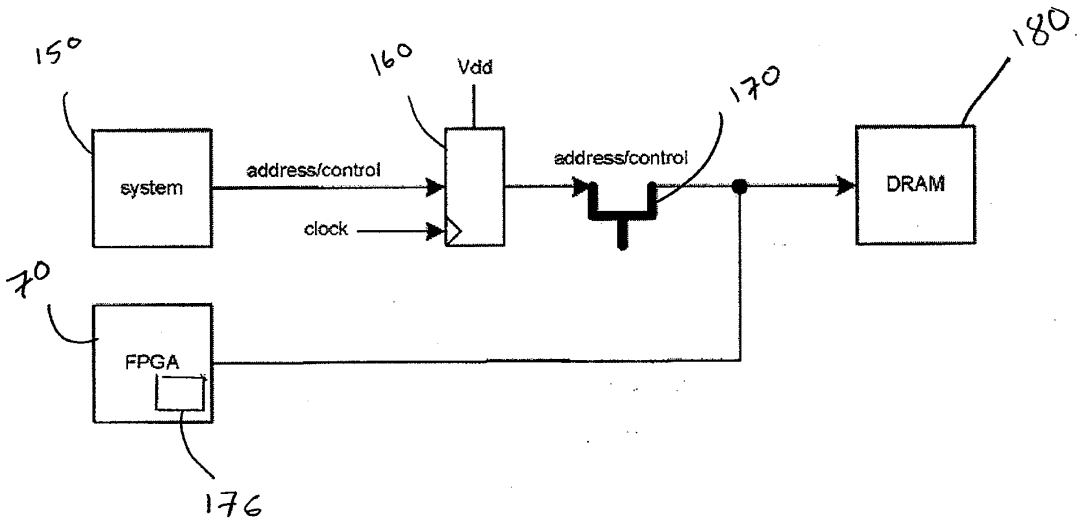

150
160
Vdd
170
180
system
address/control
clock
address/control
DRAM
70
FPGA
176

Figure 5

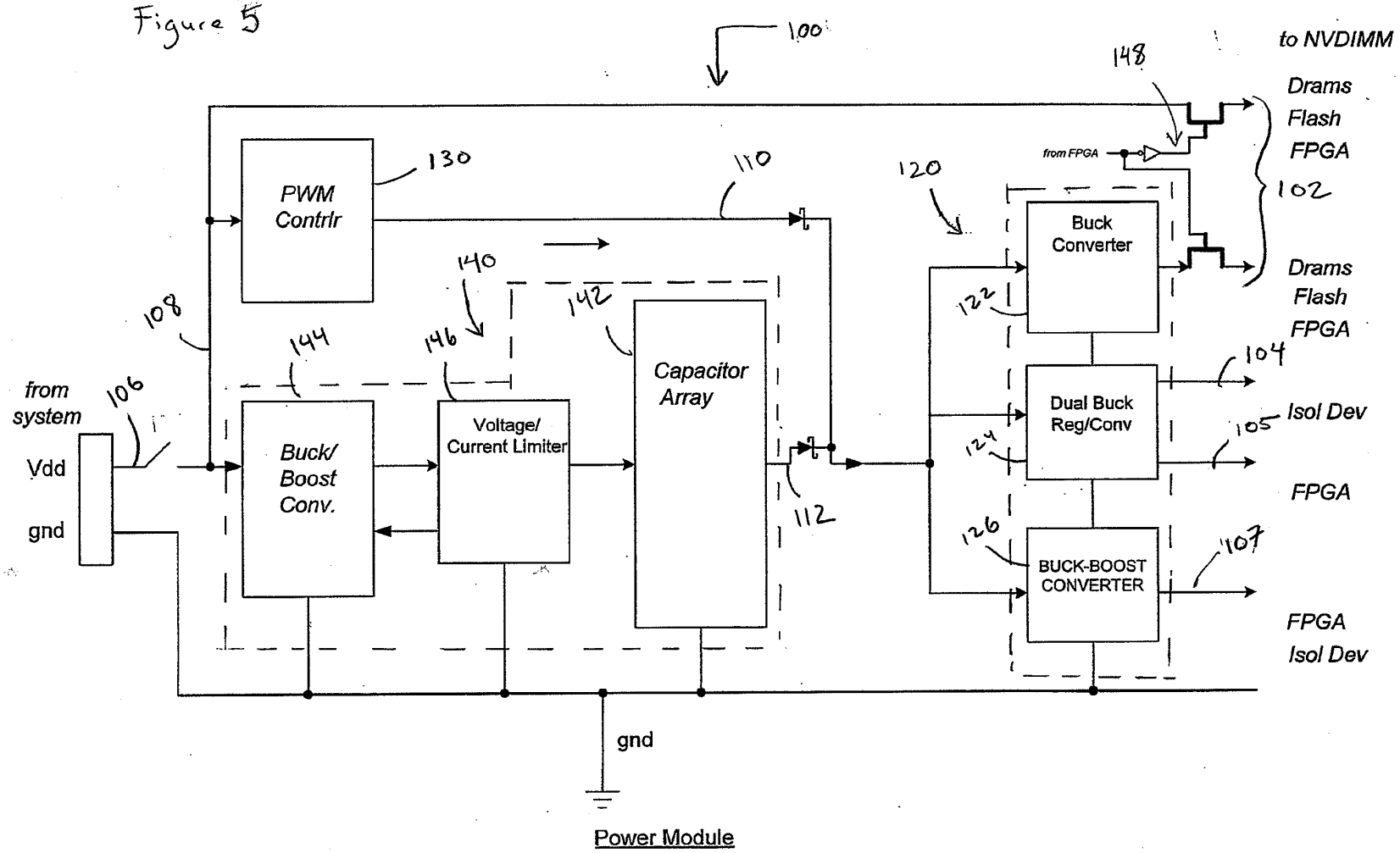

100
to NVDIMM
148
Drams
Flash
FPGA
102
from FPGA
PWM
Contrlr
130
110
120
Buck
Converter
140
142
108
144
146
Capacitor
Array
122
Drams
Flash
FPGA
104
from
system
106
Vdd
gnd
Buck/
Boost
Conv.
Voltage/
Current Limiter
Dual Buck
Reg/Conv
Isol Dev
105
124
112
FPGA
126
BUCK-BOOST
CONVERTER
107
FPGA
Isol Dev
gnd
Power Module

Figure 6

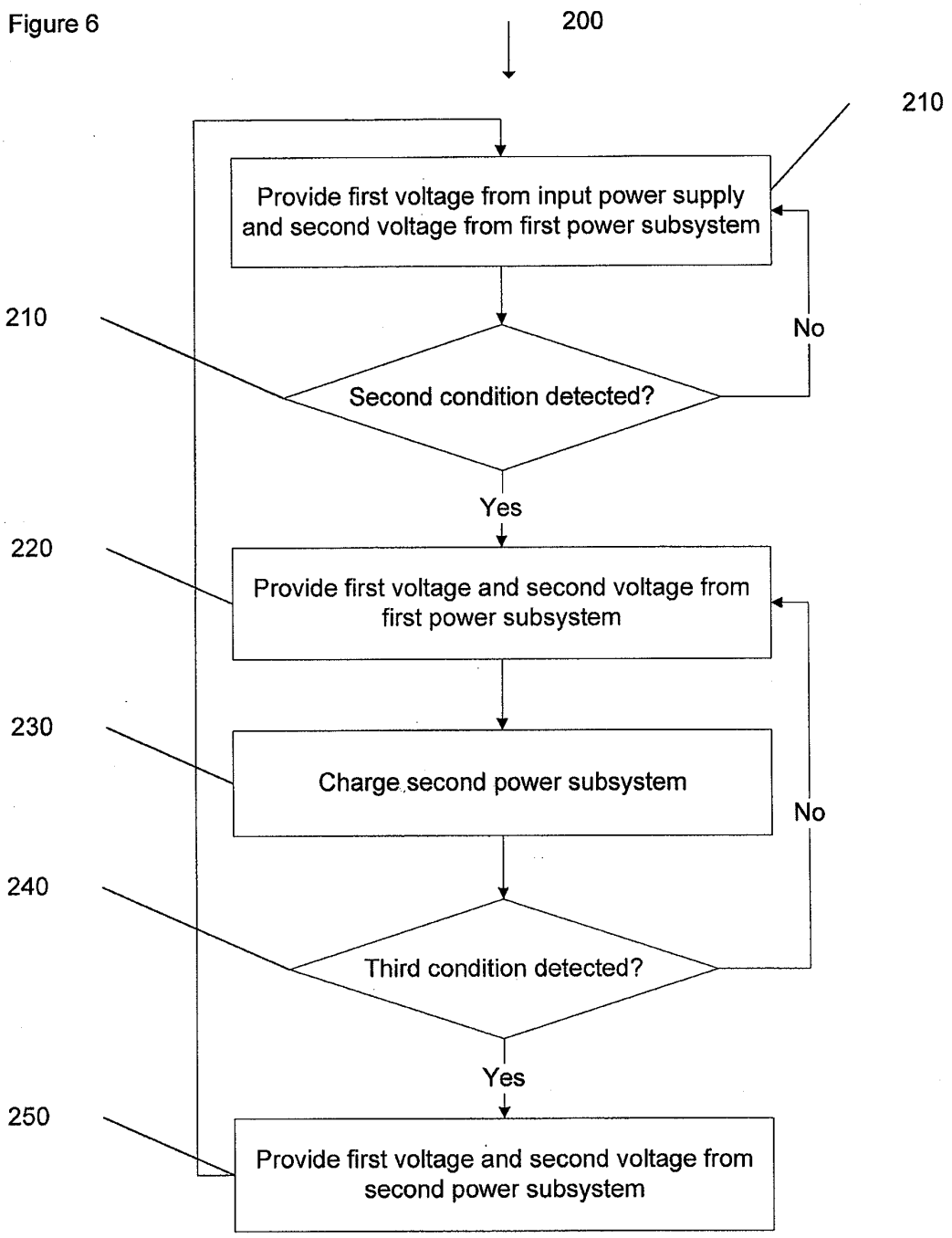

200
210
Provide first voltage from input power supply and second voltage from first power subsystem
210
No
Second condition detected?
Yes
220
Provide first voltage and second voltage from first power subsystem
230
Charge second power subsystem
No
240
Third condition detected?
Yes
250
Provide first voltage and second voltage from second power subsystem

Figure 7

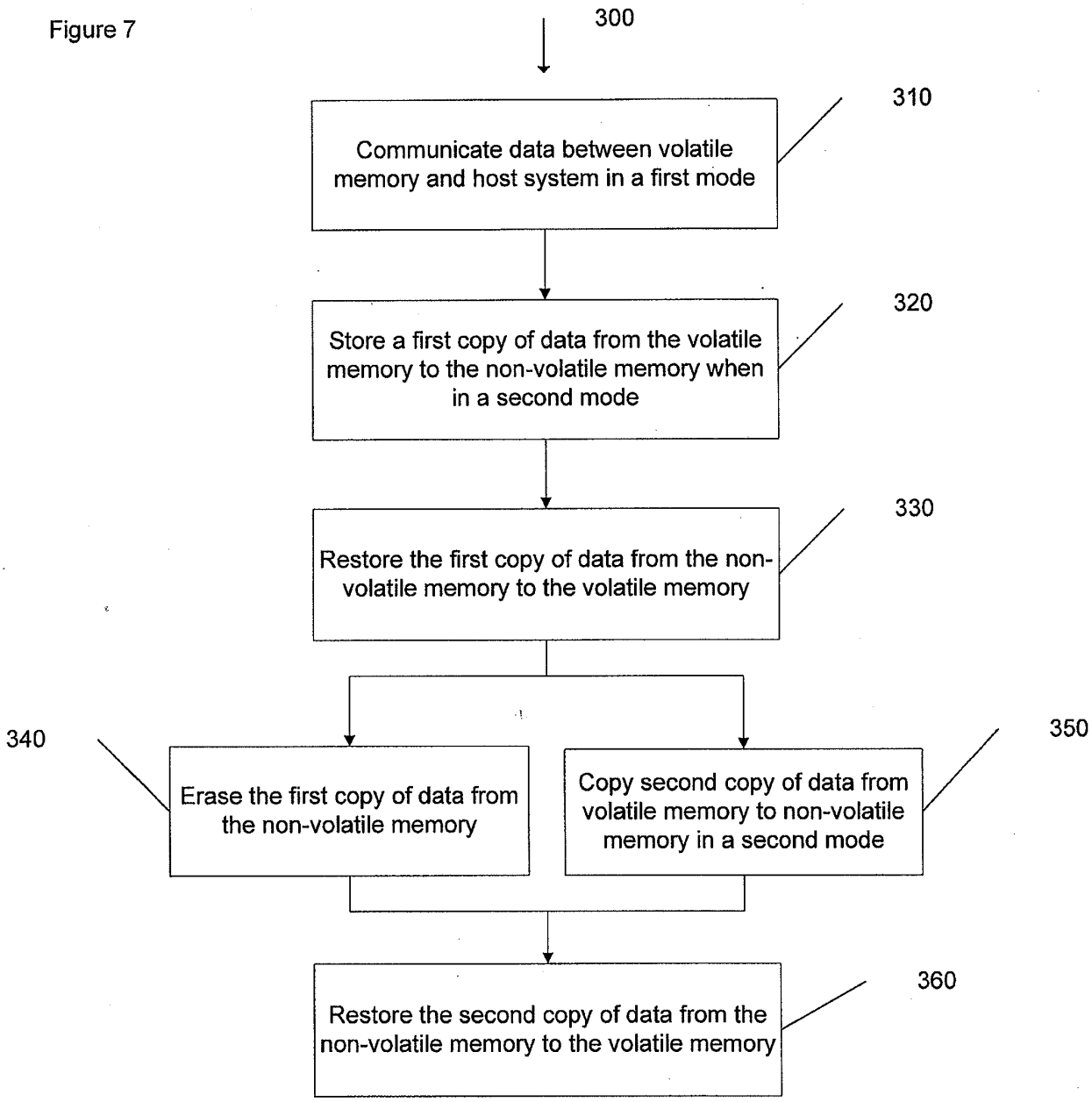

300
310
Communicate data between volatile memory and host system in a first mode
320
Store a first copy of data from the volatile memory to the non-volatile memory when in a second mode
330
Restore the first copy of data from the non-volatile memory to the volatile memory
340
Erase the first copy of data from the non-volatile memory
350
Copy second copy of data from volatile memory to non-volatile memory in a second mode
360
Restore the second copy of data from the non-volatile memory to the volatile memory

Figure 8

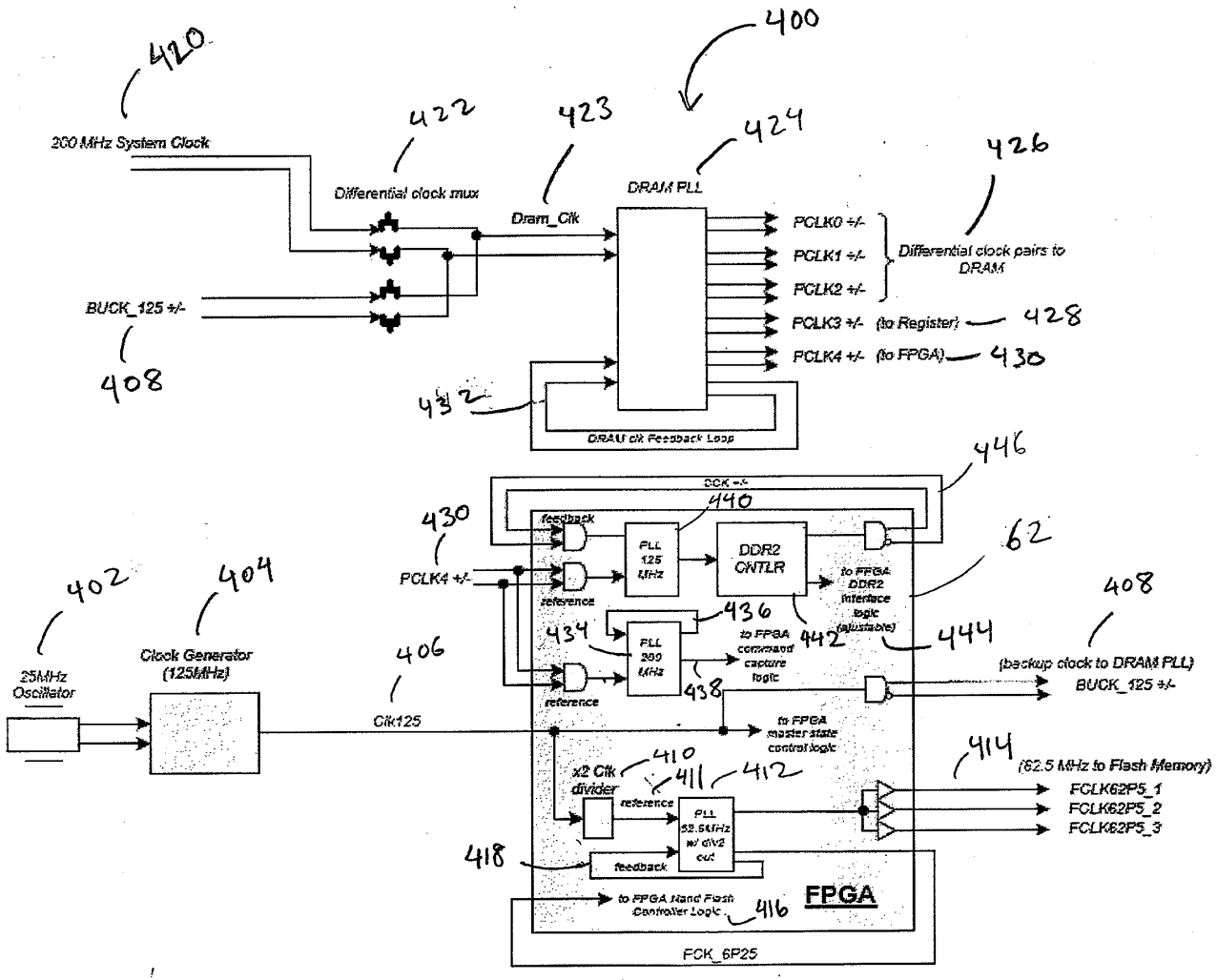

420
400
200 MHz System Clock
422
Differential clock mux
423
Dram_Clk
424
DRAM PLL
426
PCLK0 +/-
PCLK1 +/-
PCLK2 +/-
Differential clock pairs to DRAM
BUCK_125 +/-
PCLK3 +/- (to Register)
428
PCLK4 +/- (to FPGA)
430
408
432
DRAM clk Feedback Loop
446
440
feedback
PLL 125 MHz
DDR2 CNTLR
62
to FPGA DDR2 interface logic (optional)
430
PCLK4 +/-
reference
436
434
PLL 200 MHz
to FPGA command capture logic
442
444
408
(backup clock to DRAM PLL)
BUCK_125 +/-
402
404
406
25MHz Oscillator
Clock Generator (125MHz)
Clk125
438
reference
to FPGA master state control logic
414
(62.5 MHz to Flash Memory)
x2 Clk divider
410
411
412
FCLK62P5_1
FCLK62P5_2
FCLK62P5_3
reference
PLL 62.5MHz w/ div2 out
418
feedback
to FPGA Nand Flash Controller Logic
416
FPGA
FCK_6P25

Figure 9

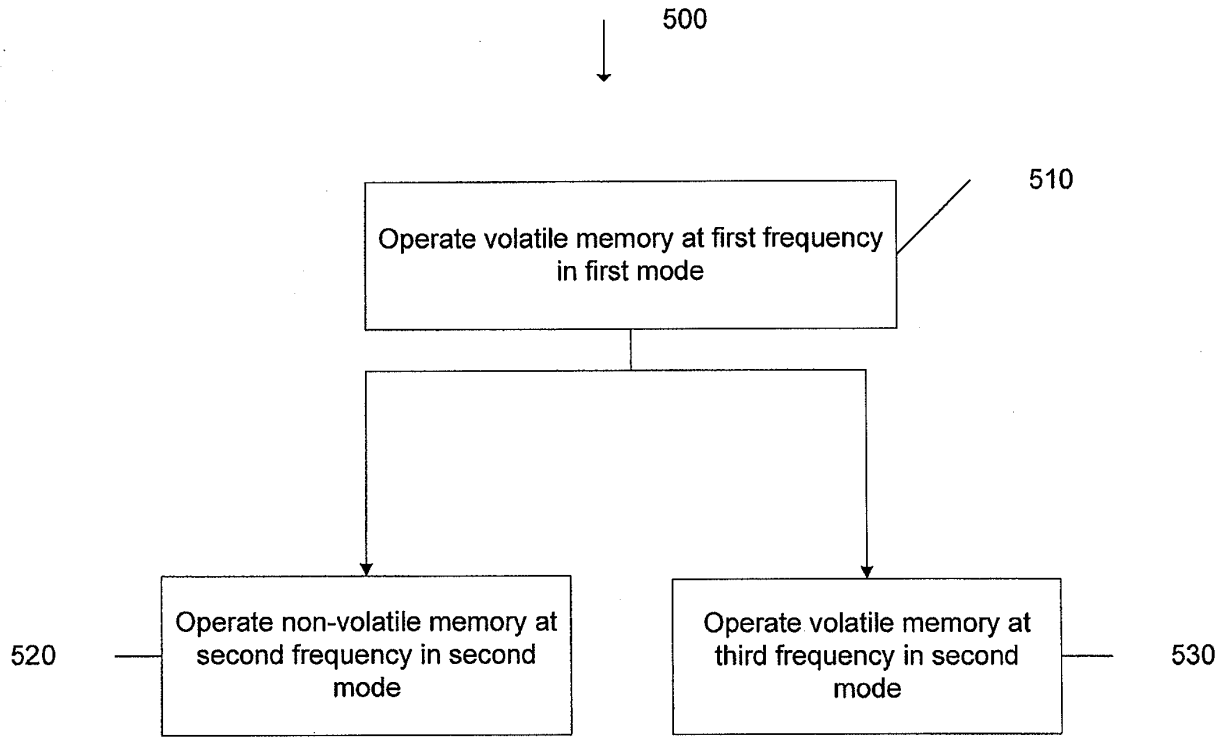

500
510
Operate volatile memory at first frequency in first mode
520
Operate non-volatile memory at second frequency in second mode
Operate volatile memory at third frequency in second mode
530

Figure 10

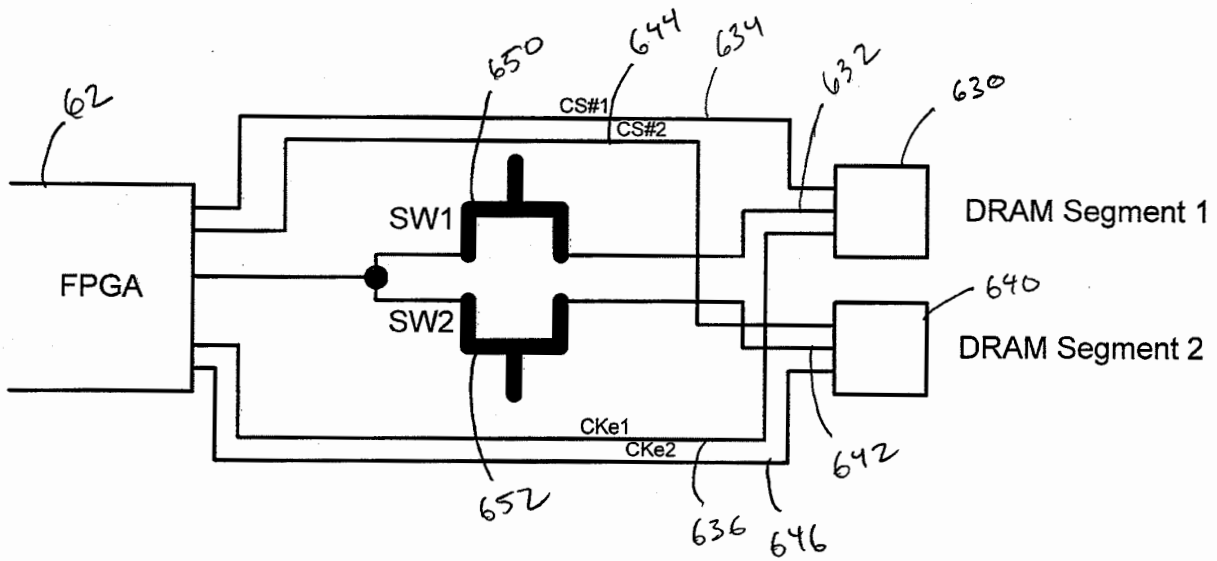
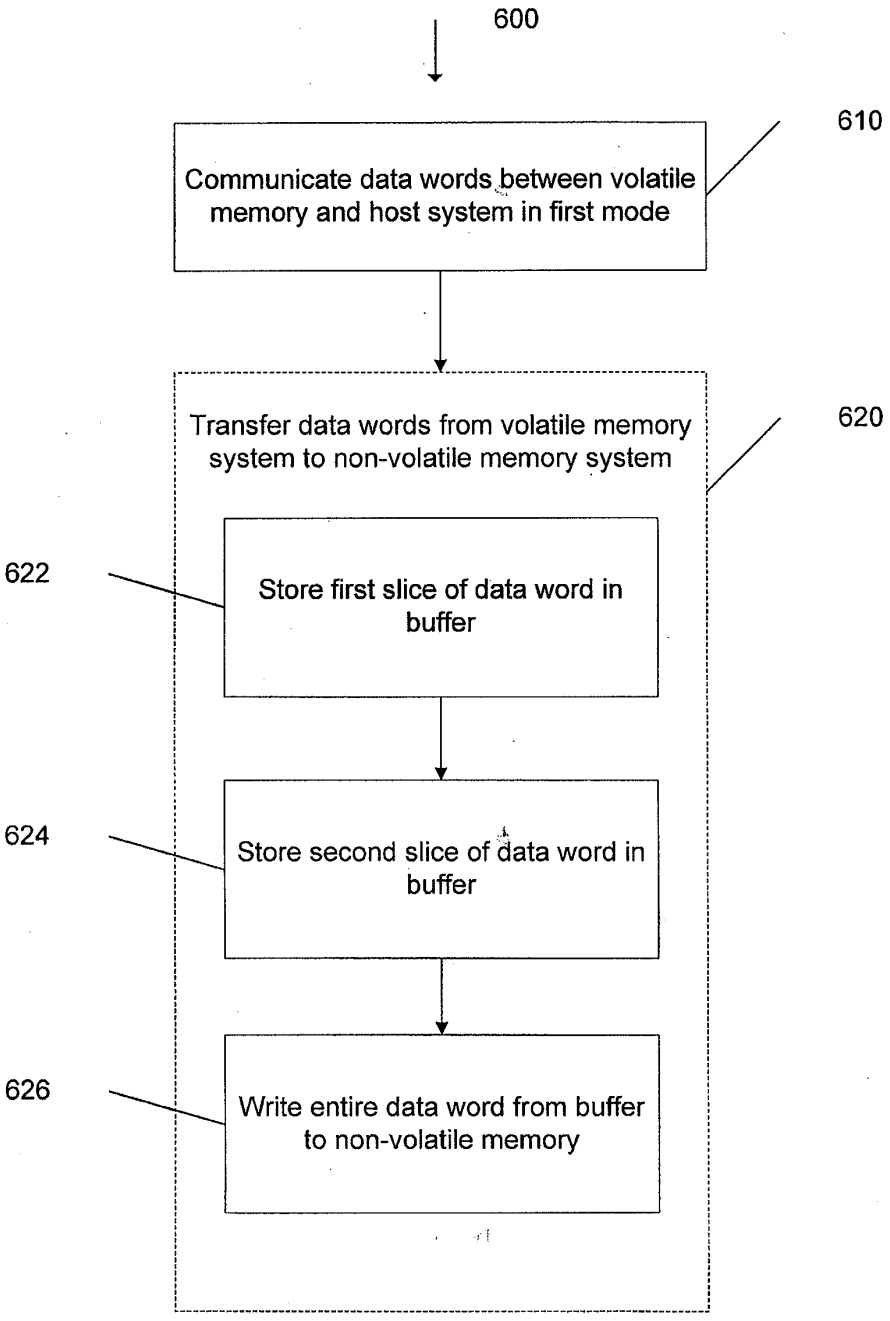

62
650
644
634
632
630
CS#1
CS#2
SW1
SW2
FPGA
DRAM Segment 1
640
DRAM Segment 2
CKe1
CKe2
642
652
636
646

Figure 11


600
610
Communicate data words between volatile memory and host system in first mode
620
Transfer data words from volatile memory system to non-volatile memory system
622
Store first slice of data word in buffer
624
Store second slice of data word in buffer
626
Write entire data word from buffer to non-volatile memory

COPY

DECLARATION FOR UTILITY OR DESIGN APPLICATION UNDER 37 CFR 1.63

Docket No.: NETL.040A

Title: NON-VOLATILE MEMORY MODULE

Inventors: Chi-She Chen, Jeffrey C. Solomon; Scott Milton; Jayesh Bhakta

Please Direct All Correspondence to Customer Number 20995

This Declaration is directed to the invention that:

Was filed as Serial No. 12/131,873 filed on June 2, 2008

As a below named inventor:

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is described and claimed and for which a patent is sought;

I have reviewed and understand the contents of the above-identified application, including the claims, and any amendment filed herewith or identified above;

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56;

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of **first** inventor: Chi-She Chen

Signature: _____ Date: 09-15-08

Citizenship: Taiwan

Mailing Address: 944 Crystal Water Lane, Walnut, CA 91789

Residence Address: Same as above
(if different than above)

DECLARATION FOR UTILITY OR DESIGN APPLICATION UNDER 37 CFR 1.63

Docket No.: NETL.040A

Title: NON-VOLATILE MEMORY MODULE

Inventors: Chi-She Chen, Jeffrey C. Solomon; Scott Milton; Jayesh Bhakta

Please Direct All Correspondence to Customer Number 20995

Full name of **second** inventor: Jeffery C. Solomon

Signature: Jeffrey C Solomon Date: 09-15-08

Citizenship: United States

Mailing Address: 6 Silver Fir, Irvine, CA 92604

Residence Address: Same as above
(if different than above)

Full name of **third** inventor: Scott Milton

Signature: Scott H. Milton Date: 09/15/2008

Citizenship: United States

Mailing Address: 49 Statehouse Place, Irvine, CA 92602

Residence Address: Same as above
(if different than above)

Full name of **fourth** inventor: Jayesh Bhakta

Signature: Jayesh Bhakta Date: 9-15-08

Citizenship: United States

Mailing Address: 12220 Rose Street, Cerritos, CA 90703

Residence Address: Same as above
(if different than above)

Send Correspondence To:
KNOBBE, MARTENS, OLSON & BEAR, LLP
Customer No. 20,995

5618847

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	CHI-SHE CHEN
Filer:	Bruce S. Itchkawitz/Khylo Rhoden
Attorney Docket Number:	NETL.040C1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	310	310
Utility Search Fee	1111	1	510	510
Utility Examination Fee	1311	1	210	210
Pages:				
Claims:				
Claims in excess of 20	1202	34	50	1700
Independent claims in excess of 3	1201	4	210	840
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**3570**

Electronic Acknowledgement Receipt	
EFS ID:	4027882
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	CHI-SHE CHEN
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Chelsea Pearsall
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.040C1
Receipt Date:	29-SEP-2008
Filing Date:	
Time Stamp:	21:11:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$3570
RAM confirmation Number	5851
Deposit Account	111410
Authorized User	KNOBBE MARTENS OLSON AND BEAR
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NETL040C1.pdf	3115757 d6a44207cc2e372ce42cc20b95e514aa36eafe65	yes	58

Multipart Description/PDF files in .zip description

Document Description	Start	End
Application Data Sheet	1	4
Specification	5	35
Claims	36	43
Abstract	44	44
Drawings-only black and white line drawings	45	56
Oath or Declaration filed	57	58

Warnings:

Information:

2	Fee Worksheet (PTO-06)	fee-info.pdf	37878 528a30fcd98f429c7514b64ce48d6f5f365481e6	no	2

Warnings:

Information:

Total Files Size (in bytes):	3153635

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (12-04)

09/29/08

Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

12/240,916

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	310
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	510
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	210
TOTAL CLAIMS (37 CFR 1.16(i))	54 minus 20 =	* 34	X 25=		OR	X 50=	1700
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7 minus 3 =	* 4	X 105=			X 210=	840
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			N/A			N/A	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	3570

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/240,916	09/29/2008	Chi-She Chen	NETL.040C1

CONFIRMATION NO. 6240

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

FORMALITIES LETTER

OC000000032525402

Date Mailed: 10/15/2008

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - The drawings must be reasonably free from erasures and must be free from alterations, overwriting, interlineations, folds, and copy marks. See Figure(s) 8.
  - Numbers, letters, and reference characters on the drawings must measure at least 0.32 cm (1/8 inch) in height. See Figure(s) 8.
  - The drawings submitted to the Office are not electronically reproducible because portions of figures 8 are missing and/or blurry.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/agizaw/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
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www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/240,916	09/29/2008	2189	3570	NETL.040C1	54	7

CONFIRMATION NO. 6240

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

FILING RECEIPT

OC000000032525401

Date Mailed: 10/15/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Chi-She Chen, Walnut, CA;
Jeffery C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 12/131,873 06/02/2008
which claims benefit of 60/941,586 06/01/2007

Foreign Applications

If Required, Foreign Filing License Granted: 10/08/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/240,916**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

NON-VOLATILE MEMORY MODULE

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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Please Direct All Correspondence to Customer Number 20,995

RESPONSE TO FORMALITIES NOTICE

Applicant	:	Chi-She Chen et al.
App. No	:	12/240,916
Filed	:	September 29, 2008
For	:	NON-VOLATILE MEMORY MODULE
Art Unit	:	2189

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence, and any other attachment noted on the automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web server on:

December 15, 2008
(Date)

Bruce S. Itchkawitz, Reg. No. 47,677

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-referenced application are the following:

(X) 12 Sheets of Replacement Drawings.

(X) A Supplemental Declaration in 2 pages.

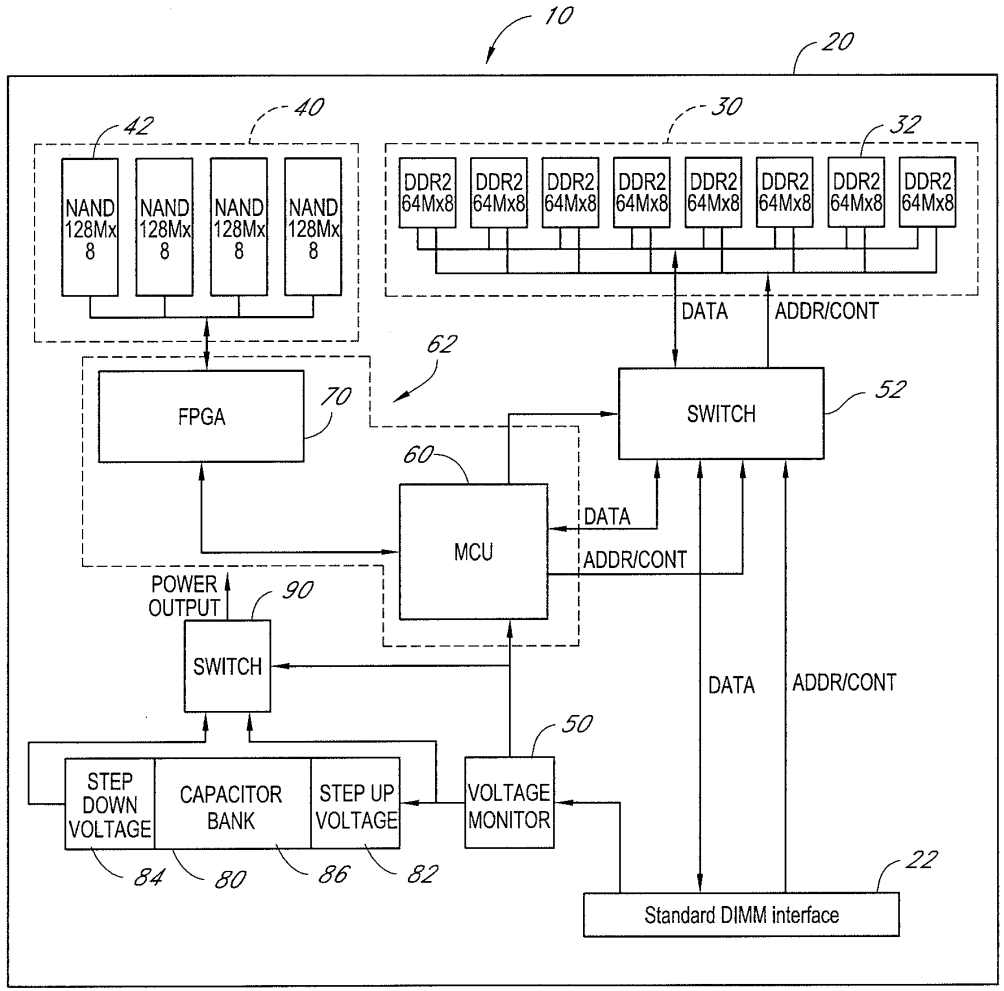
(X) Fees will be paid via EFS Web. Extension of time is requested by payment of any extension fee.

Please note that a copy of the declaration filed in U.S. Application No. 12/131,873, the parent of the above-referenced application, was previously filed in this case in accordance with 37 C.F.R. § 1.63(d)(1). However, the name of inventor Jeffrey C. Solomon was incorrectly spelled "Jeffery C. Solomon" in that previously filed declaration. The enclosed newly executed declaration includes the correct spelling.

The Commissioner is hereby authorized to charge any additional fees which may be required, now or in the future, or credit any overpayment, to Account No. 11-1410.

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404

6367818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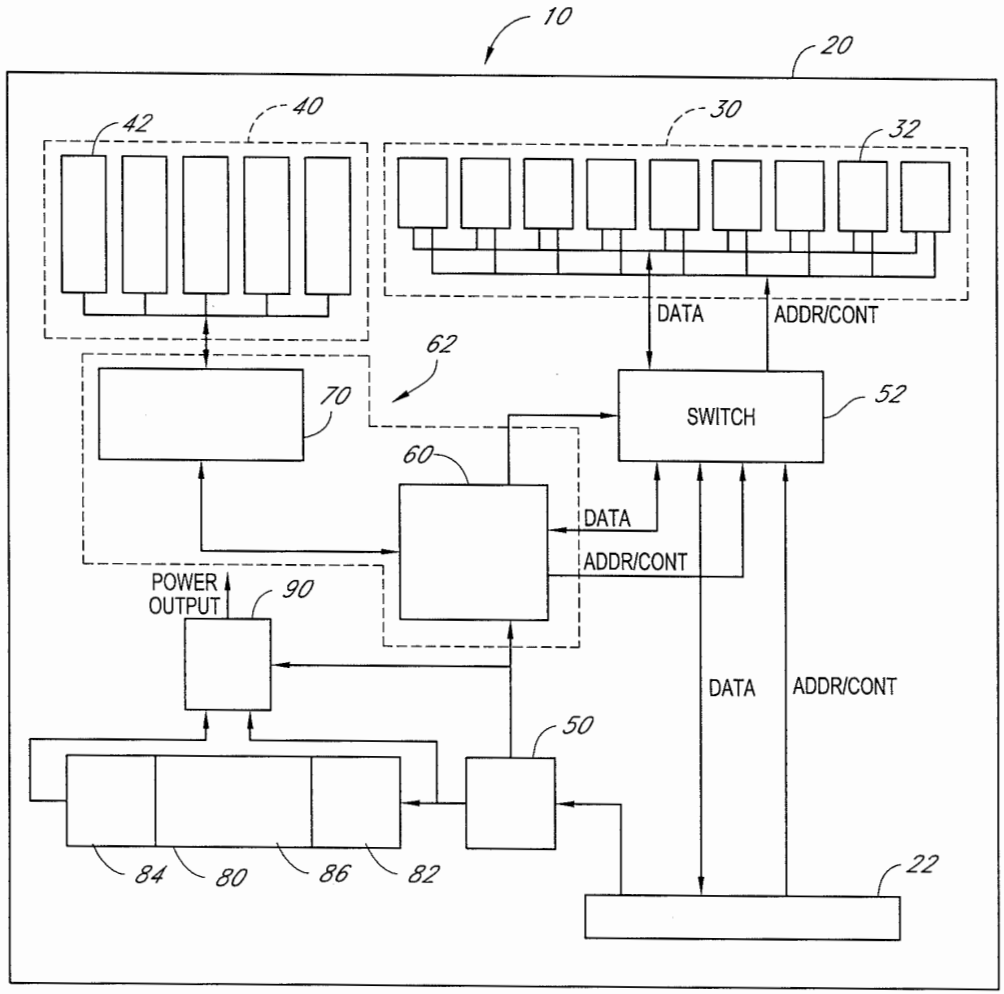
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DATA
ADDR/CONT
62
FPGA
70
SWITCH
52
60
MCU
DATA
ADDR/CONT
POWER OUTPUT
90
SWITCH
DATA
ADDR/CONT
50
STEP DOWN VOLTAGE
CAPACITOR BANK
STEP UP VOLTAGE
VOLTAGE MONITOR
84
80
86
82
22
Standard DIMM interface

FIG. 1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20
42
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ADDR/CONT
62
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SWITCH
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POWER
OUTPUT
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ADDR/CONT
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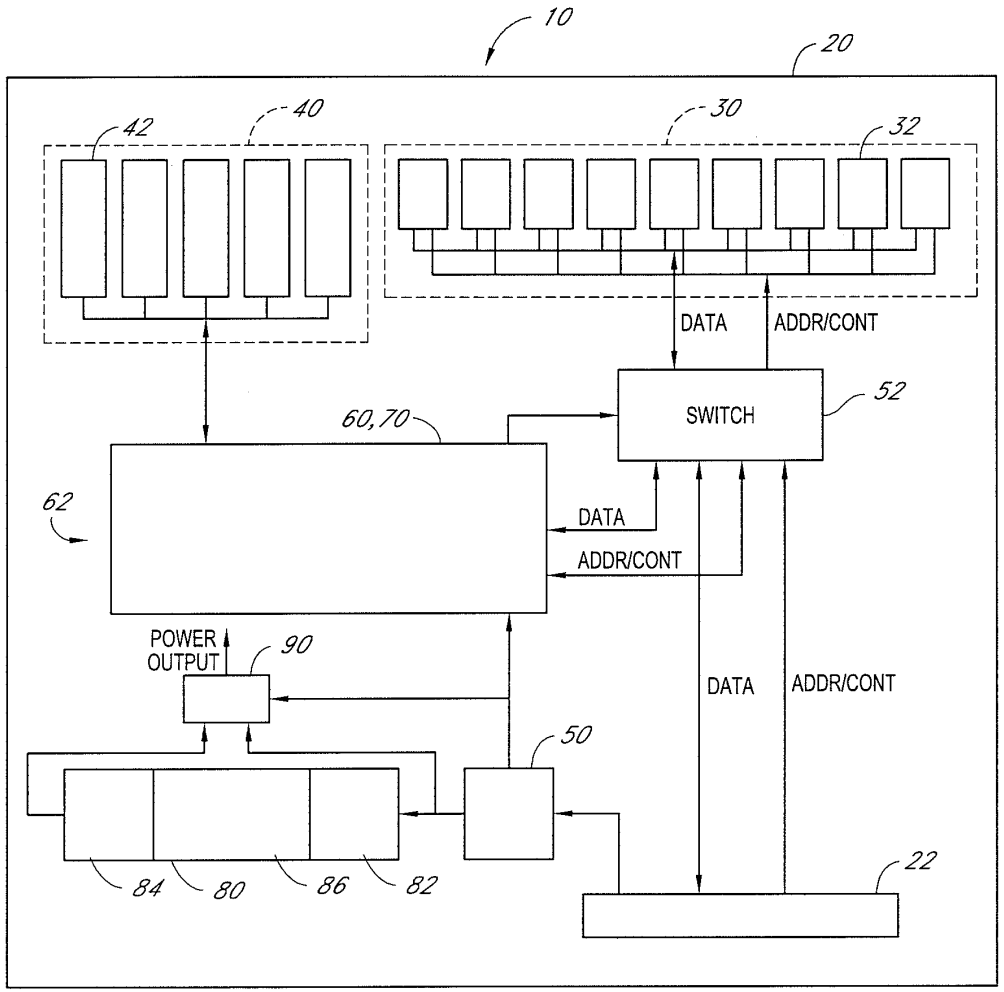
86
82
22

FIG. 2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20
42
40
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32
DATA
ADDR/CONT
SWITCH
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DATA
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POWER
OUTPUT
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ADDR/CONT
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84
80
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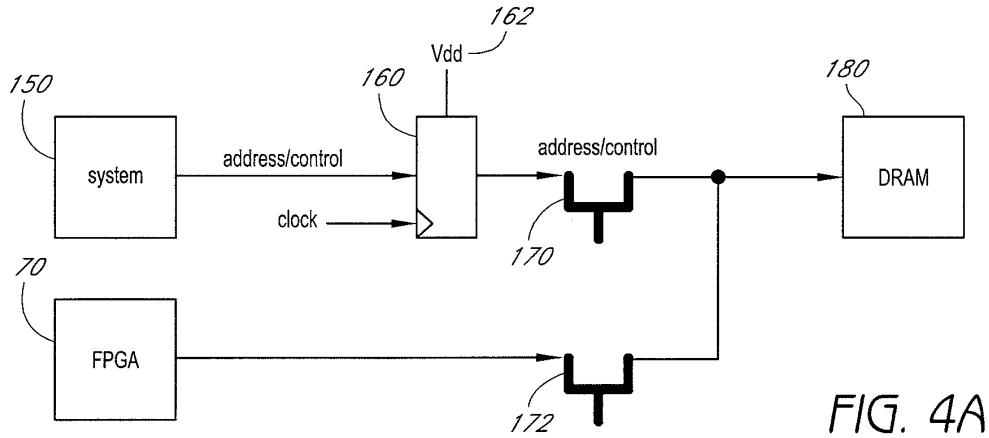
82
22

FIG. 3


162
Vdd
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150
180
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address/control
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DRAM
clock
170
70
FPGA
172

FIG. 4A

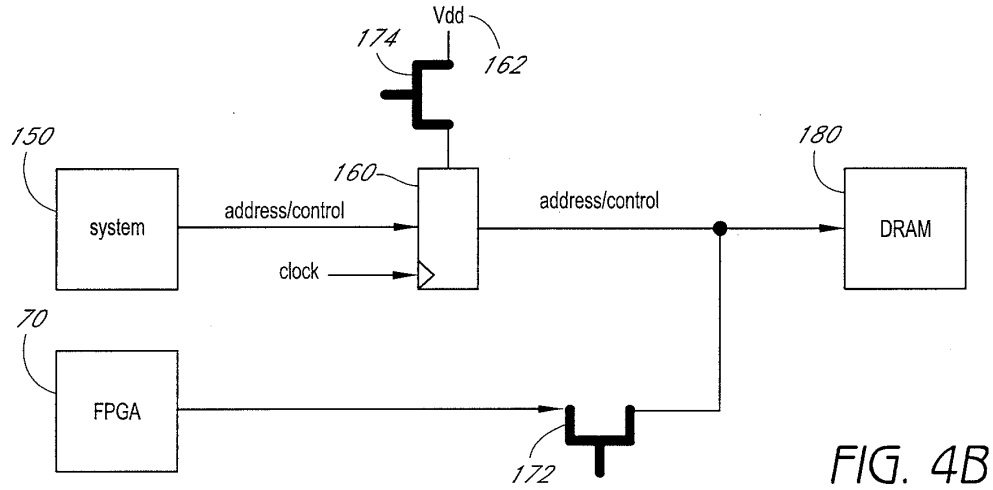
Vdd
174
162
150
180
160
system
address/control
address/control
DRAM
clock
70
FPGA
172

FIG. 4B

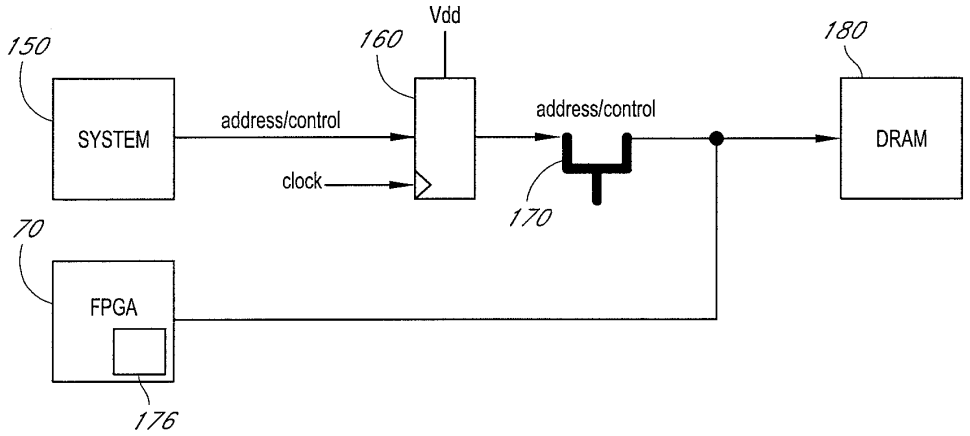
150
SYSTEM
address/control
clock
160
Vdd
address/control
170
180
DRAM
70
FPGA
176

FIG. 4C

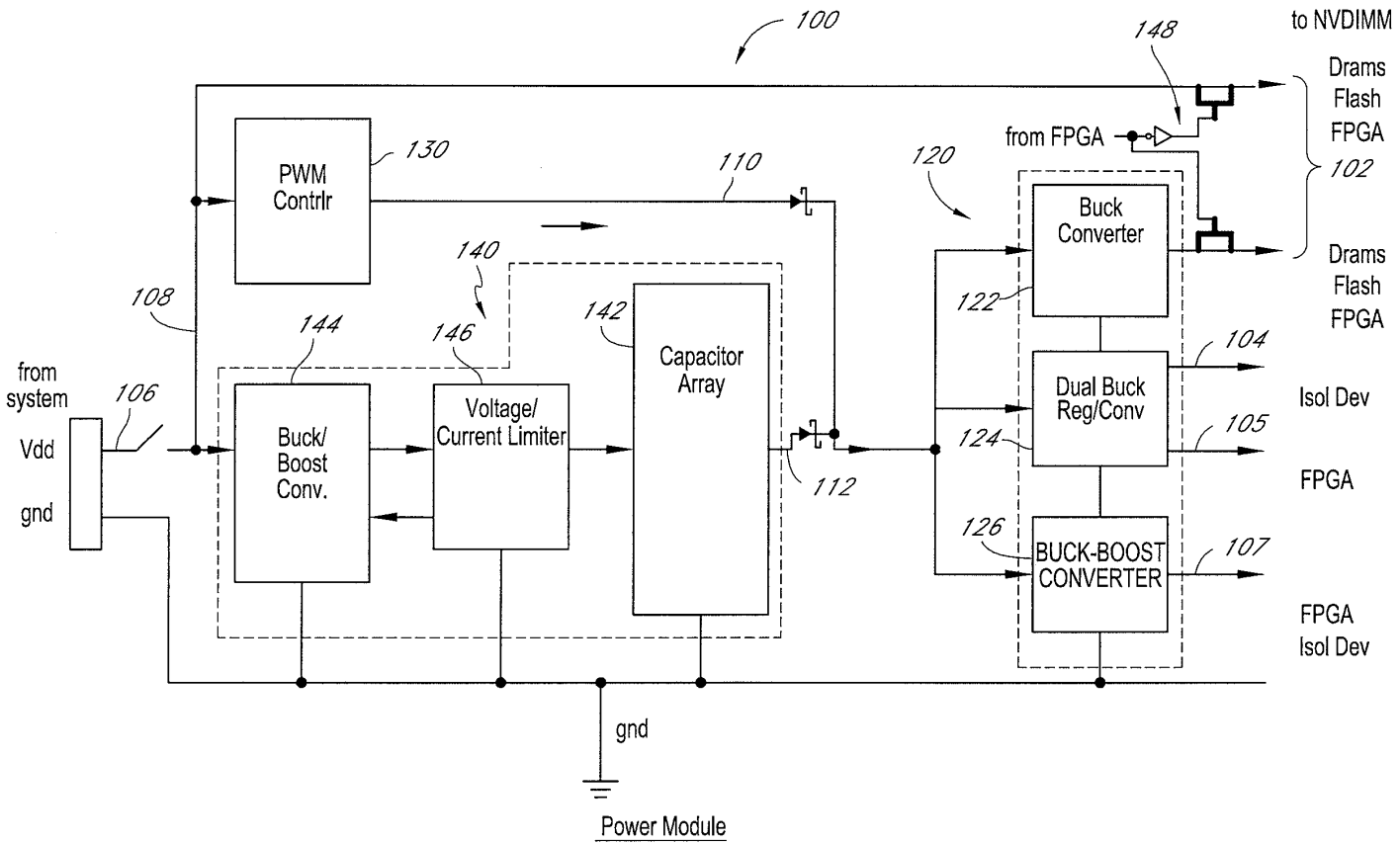
100
148
to NVDIMM
Drams
Flash
FPGA
102
from FPGA
PWM
Contrlr
130
110
120
Buck
Converter
140
108
144
146
142
Capacitor
Array
122
104
from
system
106
Buck/
Boost
Conv.
Voltage/
Current Limiter
Dual Buck
Reg/Conv
Isol Dev
105
Vdd
gnd
124
112
FPGA
126
BUCK-BOOST
CONVERTER
107
FPGA
Isol Dev
gnd
Power Module

FIG. 5

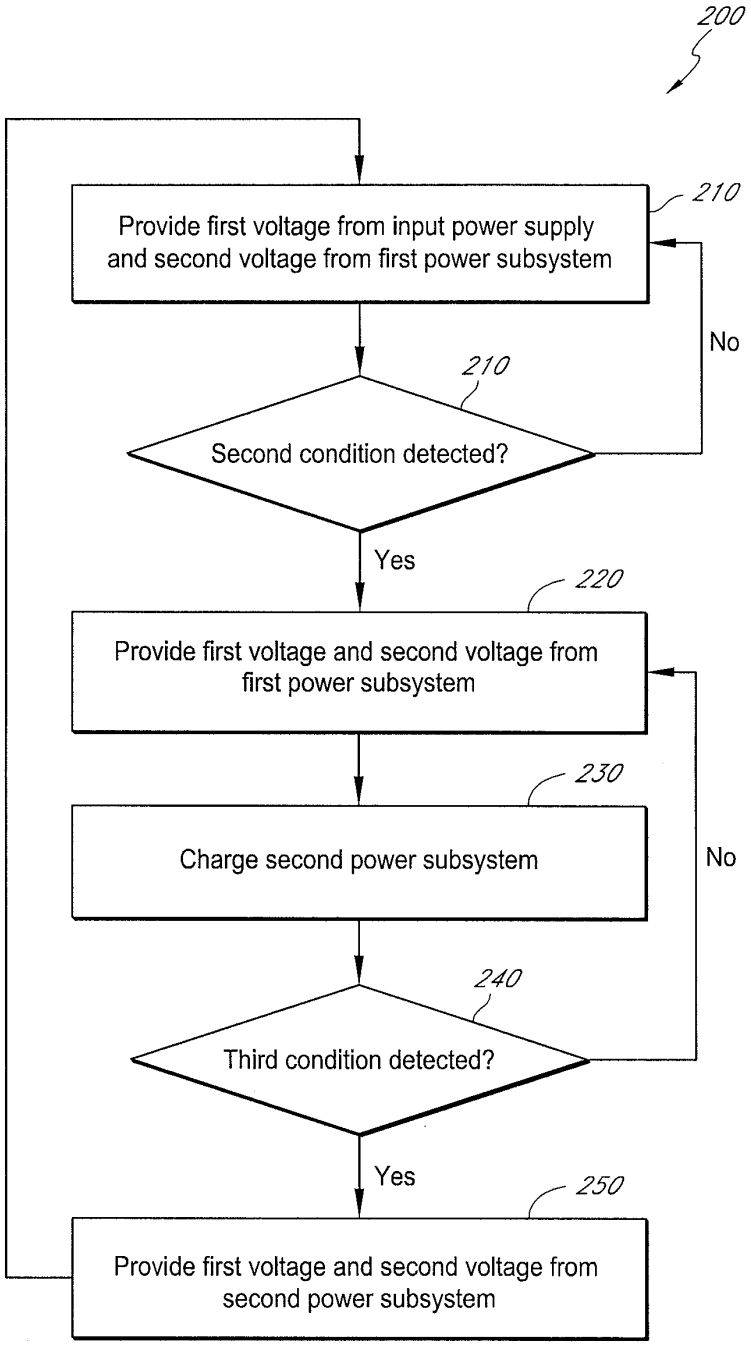
200
210
Provide first voltage from input power supply and second voltage from first power subsystem
210
Second condition detected?
No
Yes
220
Provide first voltage and second voltage from first power subsystem
230
Charge second power subsystem
No
240
Third condition detected?
Yes
250
Provide first voltage and second voltage from second power subsystem

FIG. 6

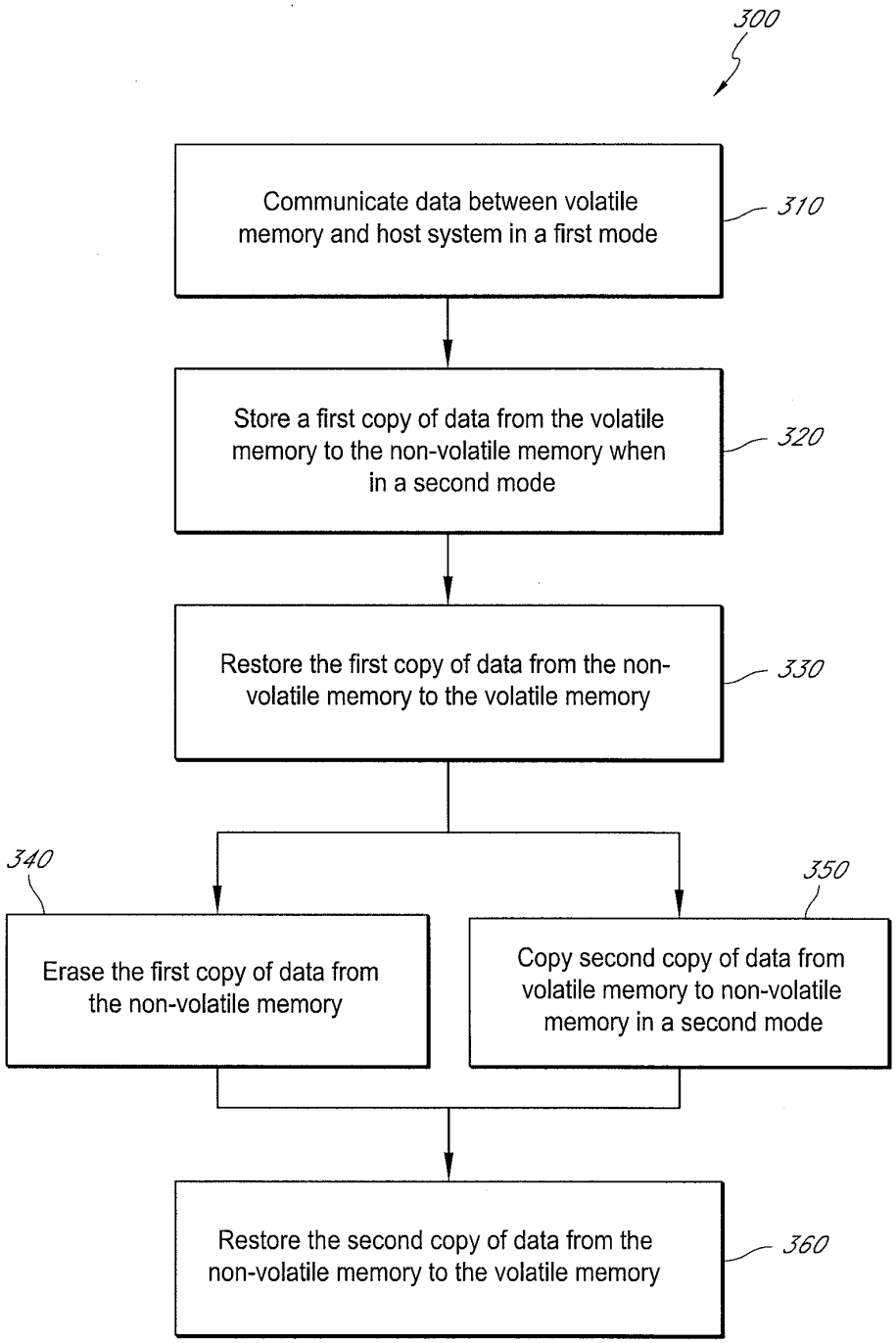
300
Communicate data between volatile memory and host system in a first mode
310
Store a first copy of data from the volatile memory to the non-volatile memory when in a second mode
320
Restore the first copy of data from the non-volatile memory to the volatile memory
330
340
Erase the first copy of data from the non-volatile memory
350
Copy second copy of data from volatile memory to non-volatile memory in a second mode
Restore the second copy of data from the non-volatile memory to the volatile memory
360

FIG. 7

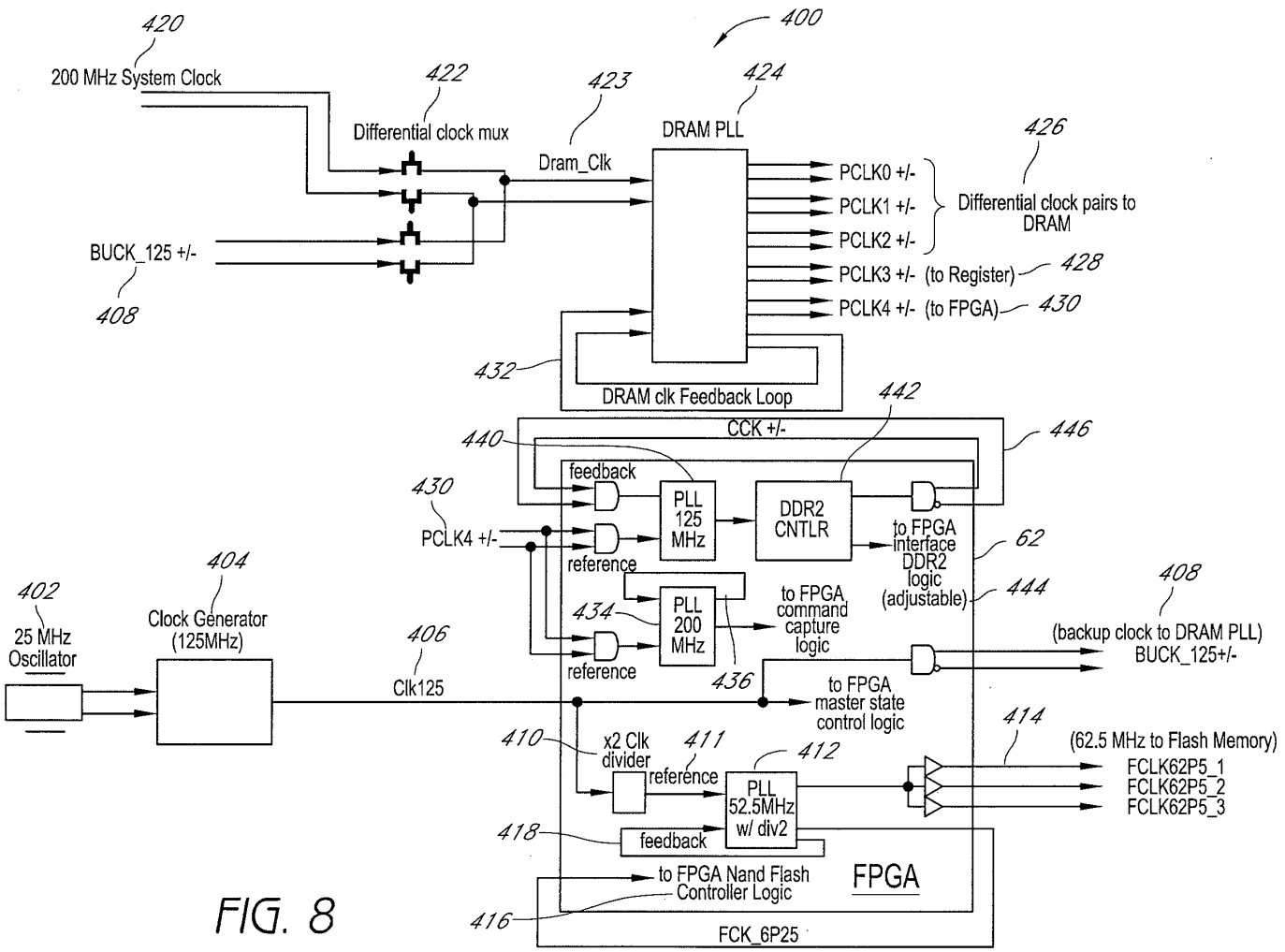
400
420
200 MHz System Clock
422
Differential clock mux
423
Dram_Clk
424
DRAM PLL
426
PCLK0 +/-
PCLK1 +/-
PCLK2 +/-
Differential clock pairs to DRAM
BUCK_125 +/-
408
PCLK3 +/- (to Register)
428
PCLK4 +/- (to FPGA)
430
432
DRAM clk Feedback Loop
442
CCK +/-
446
440
feedback
PLL 125 MHz
DDR2 CNTLR
to FPGA interface DDR2 logic (adjustable)
62
444
430
PCLK4 +/-
reference
402
25 MHz Oscillator
404
Clock Generator (125MHz)
406
Clk125
434
PLL 200 MHz
to FPGA command capture logic
436
reference
408
(backup clock to DRAM PLL)
BUCK_125+/-
to FPGA master state control logic
414
(62.5 MHz to Flash Memory)
410
x2 Clk divider
411
reference
412
PLL 52.5MHz w/ div2
FCLK62P5_1
FCLK62P5_2
FCLK62P5_3
418
feedback
to FPGA Nand Flash Controller Logic
FPGA
416
FCK_6P25

FIG. 8

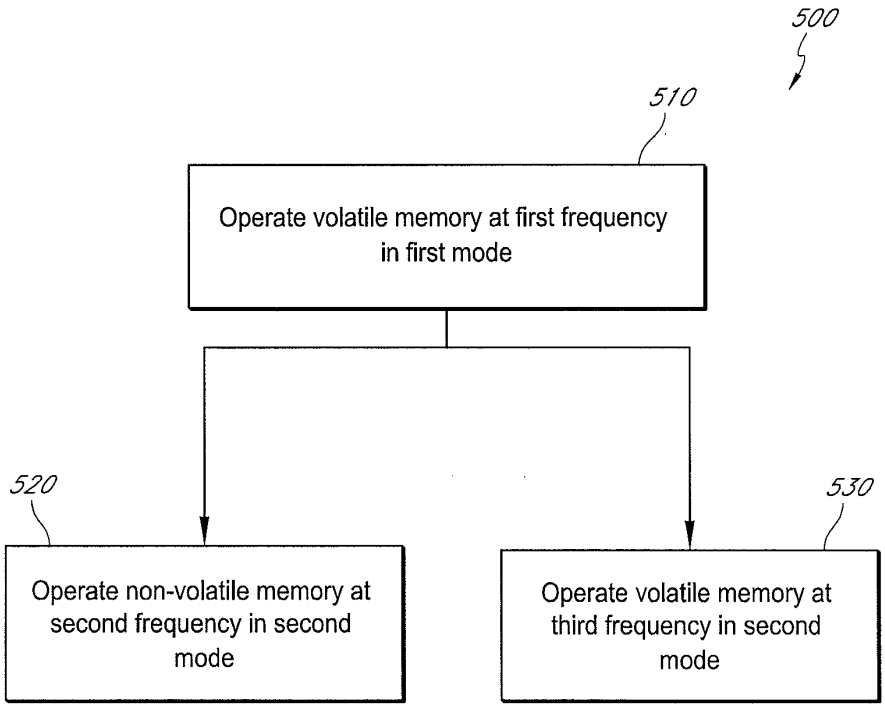
500
510
Operate volatile memory at first frequency in first mode
520
Operate non-volatile memory at second frequency in second mode
530
Operate volatile memory at third frequency in second mode

FIG. 9

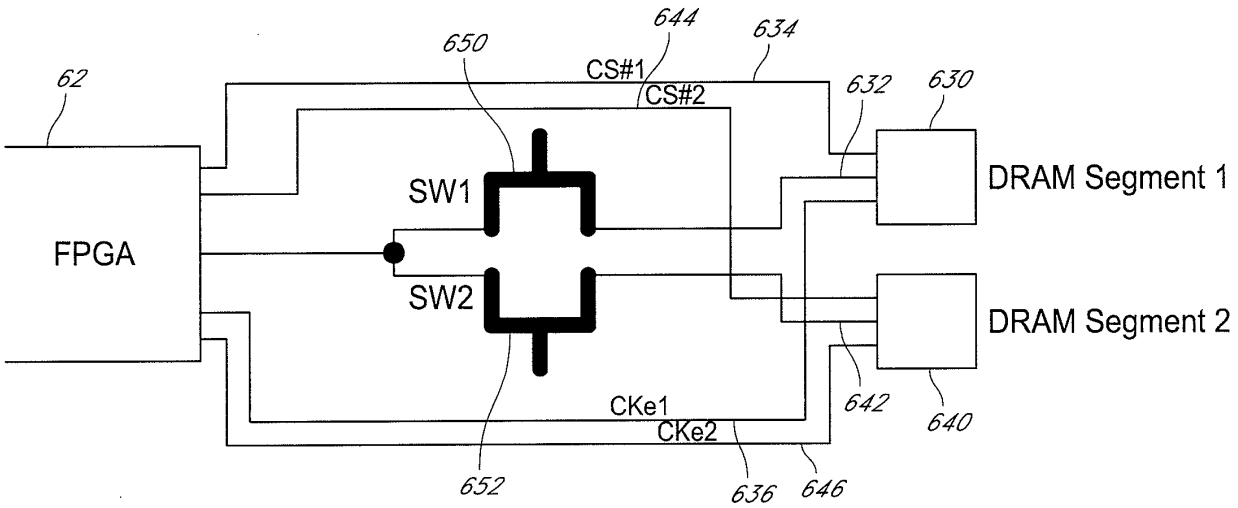
62
650
644
634
CS#1
CS#2
632
630
SW1
FPGA
SW2
DRAM Segment 1
DRAM Segment 2
CKe1
CKe2
642
640
652
636
646

FIG. 10

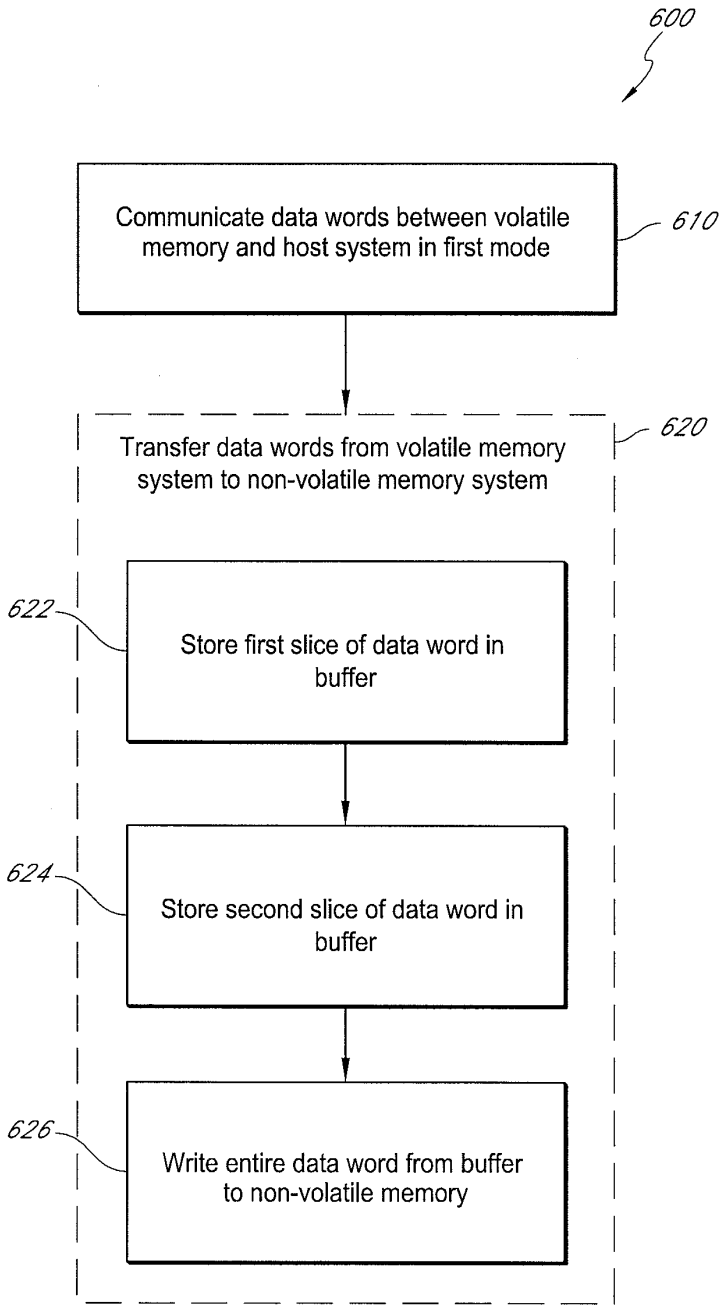
600
Communicate data words between volatile memory and host system in first mode
610
Transfer data words from volatile memory system to non-volatile memory system
620
622
Store first slice of data word in buffer
624
Store second slice of data word in buffer
626
Write entire data word from buffer to non-volatile memory

FIG. 11

DECLARATION FOR UTILITY OR DESIGN APPLICATION UNDER 37 CFR 1.63

Docket No.: NETL.040C1

Title: NON-VOLATILE MEMORY MODULE

Inventors: Chi-She Chen, Jeffrey C. Solomon; Scott Milton; Jayesh Bhakta

Please Direct All Correspondence to Customer Number 20995

This Declaration is directed to the invention that:

Was filed as Serial No. 12/240,916 filed on September 29, 2008

As a below named inventor:

I believe the inventors named below to be the original and first inventors of the subject matter which is described and claimed and for which a patent is sought;

I have reviewed and understand the contents of the above-identified application, including the claims, and any amendment filed herewith or identified above;

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56;

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of **first** inventor: Chi-She Chen

Signature: _____ Date: 12-11-08

Citizenship: Taiwan

Mailing Address: 944 Crystal Water Lane, Walnut, CA 91789

Residence Address: Same as above
(if different than above)

DECLARATION FOR UTILITY OR DESIGN APPLICATION UNDER 37 CFR 1.63

Docket No.: NETL.040C1

Title: NON-VOLATILE MEMORY MODULE

Inventors: Chi-She Chen, Jeffrey C. Solomon; Scott Milton; Jayesh Bhakta

Please Direct All Correspondence to Customer Number 20995

Full name of **second** inventor: Jeffrey C. Solomon

Signature: _____ Date: 12-11-08

Citizenship: United States

Mailing Address: 6 Silver Fir, Irvine, CA 92604

Residence Address: Same as above
(if different than above)

Full name of **third** inventor: Scott Milton

Signature: _____ Date: 12/11/2008

Citizenship: United States

Mailing Address: 49 Statehouse Place, Irvine, CA 92602

Residence Address: Same as above
(if different than above)

Full name of **fourth** inventor: Jayesh Bhakta

Signature: _____ Date: 12-11-08

Citizenship: United States

Mailing Address: 12220 Rose Street, Cerritos, CA 90703

Residence Address: Same as above
(if different than above)

Send Correspondence To:
KNOBBE, MARTENS, OLSON & BEAR, LLP
Customer No. 20,995

6282127
112408

Electronic Acknowledgement Receipt

EFS ID:	4458805
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Chelsea Pearsall
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.040C1
Receipt Date:	15-DEC-2008
Filing Date:	29-SEP-2008
Time Stamp:	19:53:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NETL040C1_MP_RESPONSE.pdf	388696 47b5f229aef5b2992864ba502fa0f296353e cba5	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Response to Pre-Exam Formalities Notice	1	1
	Drawings-only black and white line drawings	2	13
	Oath or Declaration filed	14	15
Warnings:			
Information:			
	Total Files Size (in bytes):	388696	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/240,916	09/29/2008	2189	3570	NETL.040C1	54	7

CONFIRMATION NO. 6240

UPDATED FILING RECEIPT

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

OC000000033714085

Date Mailed: 12/24/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Chi-She Chen, Walnut, CA;
Jeffery C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

Foreign Applications

If Required, Foreign Filing License Granted: 10/08/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/240,916**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

NON-VOLATILE MEMORY MODULE

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

TRANSMITTAL LETTER (General - Patent Pending)	Docket No. 987-04-CON

In Re Application Of: **Chen et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
12/240,916	September 26,2008	Unknown	22145	2189	6240

Title: **NON-VOLATILE MEMORY MODULE**

COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Statement under 37 CFR 3.73(b) (1 page)
Power of Attorney by Assignee (1 page)

in the above identified application.

- ☒ No additional fee is required.
- ☐ A check in the amount of is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account No. **11-1159** as described below.
  - ☐ Charge the amount of
  - ☒ Credit any overpayment.
  - ☒ Charge any additional fee required.
- ☐ Payment by credit card. Form PTO-2038 is attached.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Signature

Dated: **February 19, 2009**

Howard J. Klein (Reg. No. 28,727)
Klein, O'Neill & Singh, LLP (Customer No. 22145)
43 Corporate Park, Suite 204
Irvine, California 92606
Tel: 949-955-1920
Fax: 949-955-1921

cc:

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on

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(Date)

Signature of Person Mailing Correspondence

Typed or Printed Name of Person Mailing Correspondence

P16A/REV04

PTO/SB/96 (12-08)
Approved for use through 01/31/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: **Chi-She Chen et al.**

Application No./Patent No.: **12/240,916** Filed/Issue Date: **September 29, 2008**

Entitled: **NON-VOLATILE MEMORY MODULE**

NETLIST INC. , a **Corporation**

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☑ the assignee of the entire right, title, and interest; or

2. ☐ an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is _____ %)

in the patent application/patent identified above by virtue of either:

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____ , Frame _____ , or for which a copy thereof is attatched.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☑ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Jim V. Kwet	2/19/2009
Signature	Date
James Perrott	949-679-0152
Printed or Typed Name	Telephone number
SVP of Engineering and Marketing	
Title	

ASSIGNMENT

WHEREAS, We, Chi-She Chen, a Taiwanese citizen, residing at 944 Crystal Water Lane, Walnut, CA 91789; Jeffrey C. Solomon, a United States citizen, residing at 16 Silver Fir, Irvine, CA 92604; Scott Milton, a United States citizen, residing at 49 Statehouse Place, Irvine, CA 92602; and Jayesh Bhakta, a United States citizen, residing at 12220 Rose Street, Cerritos, CA 90703, have invented certain new and useful improvements in a NON-VOLATILE MEMORY MODULE for which we have filed an application for Letters Patent in the United States, Application No. 12/131,873, Filed on June 2, 2008;

AND WHEREAS, Netlist, Inc. (hereinafter "ASSIGNEE"), a Delaware Corporation, with its principal place of business at 51 Discovery, Ste #150, Irvine, CA 92618, desires to acquire the entire right, title, and interest in and to said improvements and said Application:

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, we, the inventors, do hereby acknowledge that we have sold, assigned, transferred and set over, and by these presents do hereby sell, assign, transfer and set over, unto said ASSIGNEE, its successors, legal representatives and assigns, the entire right, title, and interest throughout the world in, to and under said improvements, and said application including all provisional applications relating thereto (including but not limited to U.S. Provisional Application No. 60/941,586, filed June 1, 2007), and all divisions, renewals and continuations thereof, and all Letters Patent of the United States which may be granted thereon and all reissues and extensions thereof, and all rights of priority under International Conventions and applications for Letters Patent which may hereafter be filed for said improvements in any country or countries foreign to the United States, and all Letters Patent which may be granted for said improvements in any country or countries foreign to the United States and all extensions, renewals and reissues thereof; and we hereby authorize and request the Commissioner of Patents of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said improvements to said ASSIGNEE, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND WE DO HEREBY sell, assign, transfer, and convey to ASSIGNEE, its successors, legal representatives, and assigns all claims for damages and all remedies arising out of any violation of the rights assigned hereby that may have accrued prior to the date of assignment to ASSIGNEE, or may accrue hereafter, including, but not limited to, the right to sue for, collect, and retain damages for past infringements of said Letters Patent before or after issuance.

AND WE HEREBY covenant and agree that we will communicate to said ASSIGNEE, its successors, legal representatives and assigns, any facts known to us respecting said improvements, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing and reissue applications, make all rightful oaths and generally do everything possible to aid said ASSIGNEE, its successors, legal representatives and assigns, to obtain and enforce proper patent protection for said improvements in all countries.

SEE ATTACHED ACKNOWLEDGMENT

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 24th day of October, 2008.

Chi-She Chen

STATE OF California }
COUNTY OF Orange } ss.

On October 24, 2008, before me, Dennis B. Ginther, notary public, personally appeared Chi-She Chen who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(ies), and that by his signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

[SEAL]

DENNIS B. GINTHER
Commission # 1648822
Notary Public - California
Orange County
My Comm. Expires Mar 30, 2010

Notary Signature

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 22nd day of October, 2008.

Jeffrey C. Solomon

STATE OF California }
COUNTY OF Orange } ss.

On October 22, 2008, before me, Dennis B. Ginther, notary public, personally appeared Jeffrey C. Solomon who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/~~are~~ subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(~~ies~~), and that by his signature(~~s~~) on the instrument the person(~~s~~), or the entity upon behalf of which the person(~~s~~) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

[SEAL]

DENNIS B. GINTHER
Commission # 1648822
Notary Public - California
Orange County
My Comm. Expires Mar 30, 2010

Notary Signature

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 24 day of October, 2008.

Scott H. Milton
Scott Milton

STATE OF California }
} ss.
COUNTY OF Orange }

On October 24, 2008, before me Dennis B. Ginther, notary public, personally appeared Scott Milton who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(ies), and that by his signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

[SEAL]

DENNIS B. GINTHER
Commission # 1648822
Notary Public - California
Orange County
My Comm. Expires Mar 30, 2010

Notary Signature

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 22 day of October, 2008.

Jayesh Bhakta

STATE OF California }
COUNTY OF Orange } ss.

On October 22, 2008, before me, Dennis B. Ginther, notary public, personally appeared Jayesh Bhakta who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(ies), and that by his signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

[SEAL]

Notary Signature

DENNIS B. GINTHER
Commission # 1648822
Notary Public - California
Orange County
My Comm. Expires Mar 30, 2010

5619488

U.S. Patent Application No.: 12/240,916
Attorney Docket No.: 987-04-CON

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:	)	
Chen et al.	)	**Group Art Unit: 2189**
	)	
Serial No.: 12/240,916	)	**Confirmation No.: 6240**
	)	
Filed: September 29, 2008	)	**Examiner: To be assigned**
	)	
For: NON-VOLATILE MEMORY MODULE	)	
	)	

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST (REVOCATION OF PRIOR POWERS)

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

As representative of the assignee of an entire interest in the above-identified application, the undersigned hereby revokes all previous powers of attorney and appoints the practitioners associated with Customer Number **22145** as attorney for the assignee herein, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Please direct all correspondence to:

Howard J. Klein (Reg. No.: 28,727)
Klein, O'Neill & Singh, LLP (Customer No. 22145)
43 Corporate Park, Suite 204
Irvine, California 92606
Telephone: (949) 955-1920
Fax: (949) 955-1921

Respectfully submitted,

Netlist Inc.

Dated: 2/19/2009

By: James P. Perrott

Name: James Perrott
Title: SVP of Engineering and Marketing

NETLIST INC.
51 Discovery, Suite 150
Irvine, California 92618

Electronic Acknowledgement Receipt

EFS ID:	4825579
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	20995
Filer:	Howard J. Klein/Carrie Cheung
Filer Authorized By:	Howard J. Klein
Attorney Docket Number:	NETL.040C1
Receipt Date:	19-FEB-2009
Filing Date:	29-SEP-2008
Time Stamp:	19:11:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		987-04-CON--POAasFiled02192009.pdf	671314 2c6063649702d1d0d3fac6cc01cb3e03a769b4c7	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Assignee showing of ownership per 37 CFR 3.73(b).	2	7
	Power of Attorney	8	8
Warnings:			
Information:			
	Total Files Size (in bytes):	671314	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/81 (01-09)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	12/240,916
Filing Date	September 29, 2008
First Named Inventor	Chi-She Chen et al.
Title	NON-VOLATILE MEMORY MODULE
Art Unit	2189
Examiner Name	Unassigned
Attorney Docket Number	NETL.040C1

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: **22,145**

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐	Firm or Individual Name				
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant/Inventor.

OR

☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on 10-28-2008.

SIGNATURE of Applicant or Assignee of Record

Signature	James P. Perrott	Date	3/31/09
Name	James P. Perrott	Telephone	949-435-0025
Title and Company	Netlist, Inc. SVP, Marketing + Engineering		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	5079583
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Brittany West
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.040C1
Receipt Date:	01-APR-2009
Filing Date:	29-SEP-2008
Time Stamp:	17:50:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	SIGNED_REVOCATION_NETL040C1.PDF	93520 d712cfa6b8e26d87ceac1e6f2bdd475447c9ab8e	no	1

Warnings:

Information:

Total Files Size (in bytes):	93520

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/240,916	09/29/2008	Chi-She Chen	987-04-CON

CONFIRMATION NO. 6240

POA ACCEPTANCE LETTER

22145
KLEIN, O'NEILL & SINGH, LLP
43 CORPORATE PARK
SUITE 204
IRVINE, CA 92606

OC000000035348368

Date Mailed: 04/07/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/19/2009.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/sleutchit/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/08a(07-05)
Approved for use through 7/31/2006. OMB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

	Complete if Known
Application Number	12/240,916
Filing Date	September 29, 2008
First Named Inventor	Chi-She Chen
Art Unit	2189
Examiner Name	Unknown

Sheet	1	of	1

Attorney Docket No: 987-04-CON-H

US PATENT DOCUMENTS

Examiner Initial *	Cite No	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
		4,420,821	12-13-1983	Hoffman	02-19-1982
		4,449,205	05-15-1984	Hoffman	02-19-1982
		5,519,663	05-21-1996	Harper, Jr. et al.	09-28-1994
		6,158,015	12-05-2000	Klein	03-30-1998
		6,336,176	01-01-2002	Li et al.	08-09-1999
		6,487,623	11-26-2002	Emerson et al.	04-30-1999
		6,658,507	12-02-2003	Chan	08-31-1998
		6,799,244	09-28-2004	Tanaka et al.	12-06-2002
		2002/0083368	06-27-2002	Abe et al.	12-20-2001
		2004/0190210	09-30-2004	Leete	03-26-2003

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

EXAMINER **DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt

EFS ID:	5144773
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	22145
Filer:	Howard J. Klein/Monique Le
Filer Authorized By:	Howard J. Klein
Attorney Docket Number:	987-04-CON
Receipt Date:	13-APR-2009
Filing Date:	29-SEP-2008
Time Stamp:	17:32:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	987-04-CON--RequestFilingReceiptCorrections04132009.pdf	377274 c25cd326ff0c67d7ab3a86a6bee89bd853bb9136	no	6

Warnings:	
Information:	

2	Information Disclosure Statement (IDS) Filed (SB/08)	987-04-CON--IDSasFiled04132009.pdf	91382 34b3e6148abfa59d8bf9924c4752a25ca784852f	no	1

Warnings:	
Information:	
This is not an USPTO supplied IDS fillable form	
Total Files Size (in bytes):	468656

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Chen et al.	
Assignee:	Netlist, Inc.	
Title:	**NON-VOLATILE MEMORY MODULE**	
Serial No.:	12/240,916	Filed: September 29, 2008
Examiner:	Unknown	Group Art Unit: 2189
Confirmation No.:	6240	
Attorney Docket No.:	987-04-CON-HK	

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

REQUEST FOR FILING RECEIPT CORRECTIONS

Sir:

Attached hereto is a marked-up copy of the Official Filing Receipt in connection with the above-identified application.

THE FOLLOWING CORRECTION(S) IS/ARE RESPECTFULLY REQUESTED:

The second inventor's name should be **Jeffrey C. Solomon** instead of Jeffery C. Solomon.

It is respectfully requested that the U.S. Patent and Trademark Office forward/issue a new Filing Receipt with the correction indicated above. Support for the correction is readily apparent on the enclosed photocopy of the executed Declaration and Power of Attorney document.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 11-1159 for any additional fee required under 37 C.F.R. §§ 1.16 or 1.17.

Respectfully submitted,

Date: April 13, 2009

Howard J. Klein (Reg. No. 28,727)
Klein, O'Neill & Singh, LLP (CN 22145)
43 Corporate Park, Suite 204
Irvine, California 92606
Tel: (949) 955-1920
Fax: (949) 955 1921

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/240,916	09/29/2008	2189	3570	NETL.040C1	54	7

CONFIRMATION NO. 6240

UPDATED FILING RECEIPT

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

OC000000033714085

Date Mailed: 12/24/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

This should be "Jeffrey"

Chi-She Chen, Walnut, CA;
Jeffery C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Assignment For Published Patent Application
Netlist, Inc., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant
This application is a CON of 12/131,873 06/02/2008 ABN which claims benefit of 60/941,586 06/01/2007

Foreign Applications

If Required, Foreign Filing License Granted: 10/08/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/240,916**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

NON-VOLATILE MEMORY MODULE

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

DECLARATION FOR UTILITY OR DESIGN APPLICATION UNDER 37 CFR 1.63

Docket No.: NETL.040C1

Title: NON-VOLATILE MEMORY MODULE

Inventors: Chi-She Chen, Jeffrey C. Solomon; Scott Milton; Jayesh Bhakta

Please Direct All Correspondence to Customer Number 20995

This Declaration is directed to the invention that:

Was filed as Serial No. 12/240,916 filed on September 29, 2008

As a below named inventor:

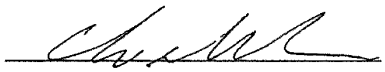
I believe the inventors named below to be the original and first inventors of the subject matter which is described and claimed and for which a patent is sought;

I have reviewed and understand the contents of the above-identified application, including the claims, and any amendment filed herewith or identified above;

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56;

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of **first** inventor: Chi-She Chen

Signature:  Date: 12-11-08

Citizenship: Taiwan

Mailing Address: 944 Crystal Water Lane, Walnut, CA 91789

Residence Address: Same as above
(if different than above)

DECLARATION FOR UTILITY OR DESIGN APPLICATION UNDER 37 CFR 1.63

Docket No.: NETL.040C1

Title: NON-VOLATILE MEMORY MODULE

Inventors: Chi-She Chen, Jeffrey C. Solomon; Scott Milton; Jayesh Bhakta

Please Direct All Correspondence to Customer Number 20995

Full name of **second** inventor: Jeffrey C. Solomon

Signature: _____ Date: 12-11-08

Citizenship: United States

Mailing Address: 6 Silver Fir, Irvine, CA 92604

Residence Address: Same as above
(if different than above)

Full name of **third** inventor: Scott Milton

Signature: Scott H. Milton Date: 12/11/2008

Citizenship: United States

Mailing Address: 49 Statehouse Place, Irvine, CA 92602

Residence Address: Same as above
(if different than above)

Full name of **fourth** inventor: Jayesh Bhakta

Signature: _____ Date: 12-11-08

Citizenship: United States

Mailing Address: 12220 Rose Street, Cerritos, CA 90703

Residence Address: Same as above
(if different than above)

Send Correspondence To:
KNOBBE, MARTENS, OLSON & BEAR, LLP
Customer No. 20,995

6282127
112408

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/240,916	09/29/2008	2189	3570	987-04-CON	54	7

CONFIRMATION NO. 6240

CORRECTED FILING RECEIPT

22145
KLEIN, O'NEILL & SINGH, LLP
43 CORPORATE PARK
SUITE 204
IRVINE, CA 92606

OC000000035930125

Date Mailed: 05/14/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 22145

Domestic Priority data as claimed by applicant

This application is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

Foreign Applications

If Required, Foreign Filing License Granted: 10/08/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/240,916**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

NON-VOLATILE MEMORY MODULE

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

PTO/SB/08a(07-05)
Approved for use through 7/31/2006. OMB 0651-0031
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	1	Attorney Docket No: 987-04-CON-H

Complete if Known	
Application Number	12/240,916
Filing Date	September 29, 2008
First Named Inventor	Chi-She Chen
Art Unit	2189
Examiner Name	Unknown
IDS Filing Date	October 5, 2009

US PATENT DOCUMENTS

Examiner Initial *	Cite No	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
		6,336,174	01-01-2002	Li et al.	08-09-1999
		7,409,590	08-05-2008	Moshayedi et al.	07-28-2006

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

EXAMINER **DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)
` EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt

EFS ID:	6201185
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	22145
Filer:	Howard J. Klein/Carrie Cheung
Filer Authorized By:	Howard J. Klein
Attorney Docket Number:	987-04-CON
Receipt Date:	05-OCT-2009
Filing Date:	29-SEP-2008
Time Stamp:	14:13:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	987-04-CON--IDSasFiled10052009.pdf	26559 8ccf00b1405571457647ea376a00d8a611715bc4	no	1

Warnings:

Information:

This is not an USPTO supplied IDS fillable form	
Total Files Size (in bytes):	26559

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/240,916	09/29/2008	Chi-She Chen	987-04-CON	6240

22145 7590 03/31/2011
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IRVINE, CA 92612

EXAMINER	
ROJAS, MIDYS	
ART UNIT	**PAPER NUMBER**
2185	
MAIL DATE	**DELIVERY MODE**
03/31/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/240,916	CHEN ET AL.	
	Examiner	Art Unit	
	MIDYS ROJAS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2008*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-54* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-20, and 43-49, drawn to a non-volatile and a volatile memory systems, classified in class 711, subclass 100 and 104.

II. Claims 21-36, drawn to a power module for a volatile and non-volatile memory including a voltage conversion element, classified in class 327, subclass 51; class 365, subclass 242; and class 714, subclass 721.

III. Claims 37-42 drawn to non-volatile and a volatile memory systems wherein the memory systems operate at different frequencies depending on the mode of operation classified in class 715, subclass 745, 789, 811.

IV. Claims 50-54, drawn to restoring data, classified in class 707 subclass 679, 680, 681.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination II has separate utility such as use in a system where a voltage conversion element is used for convert operational voltage in order to operation in different modes. See MPEP § 806.05(d).

Inventions I and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination III has separate utility such as use in a system where different modes of operation represent different operational frequencies. See MPEP § 806.05(d).

Inventions I and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination IV has separate utility such as use in a system where data can be restored. See MPEP § 806.05(d).

Inventions II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination III has separate utility such as use in a system where different modes of operation represent different operational frequencies. See MPEP § 806.05(d).

Inventions II and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination IV has separate utility such as use in a system where data can be restored. See MPEP § 806.05(d).

Inventions III and IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination IV has separate utility such as use in a system where data can be restored. See MPEP § 806.05(d).

The examiner has required restriction between subcombinations usable together. Where applicant elects a subcombination and claims thereto are subsequently found allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because at least the following reason(s) apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MIDYS ROJAS whose telephone number is (571)272-4207. The examiner can normally be reached on M-TH 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Midys Rojas/
Examiner, Art Unit 2185

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Chen et al.	
Assignee:	Netlist, Inc.	
Title:	**NON-VOLATILE MEMORY MODULE**	
Serial No.:	12/240,916	Filed: September 29, 2008
Examiner:	Rojas, Midys	Group Art Unit: 2185
Attorney Docket No.:	987-004.201	Confirmation No.: 6240

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

PRELIMINARY AMENDMENT
AND REPLY TO ELECTION/RESTRICTION REQUIREMENT

Sir:

In response to the restriction/election requirement mailed March 31, 2011, please amend the application as shown on the pages below.

Amendments to the Claims are described on page 2 of this paper.

Remarks begin on page 9 of this paper.

A Request for a One-Month Extension of Time under 37 CFR 1.136(a) is submitted herewith, along with the fee prescribed by 37 CFR 1.17(a)(1).

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Withdrawn) A memory system coupled to a computer system, comprising:

a volatile memory subsystem;

a non-volatile memory subsystem;

a controller operatively coupled to the non-volatile memory subsystem;

at least one circuit configured to selectively operatively decouple the controller from the volatile memory subsystem.

2. (Withdrawn) The memory system of Claim 1, wherein the memory system is configured to be operated in at least two states, the at least two states comprising:

a first state in which the controller and the non-volatile memory subsystem are decoupled from the volatile memory subsystem by the at least one circuit; and

a second state in which the volatile memory subsystem is operatively coupled to the controller to allow data to be communicated between the volatile memory subsystem and the non-volatile memory subsystem via the controller.

3. (Withdrawn) The memory system of Claim 2, wherein power is supplied to the volatile memory subsystem from a first power supply when the memory system is in the first state and power is supplied to the volatile memory subsystem from a second power supply when the memory system is in the second state.

4. (Withdrawn) The memory system of Claim 3, wherein the second power supply does not comprise a battery.

5. (Withdrawn) The memory system of Claim 3, wherein the second power supply comprises one or more capacitors.

6. (Withdrawn) The memory system of Claim 5, wherein the second power supply comprises a battery and is configured to power the volatile memory subsystem for less

than thirty minutes.

7. (Withdrawn) The memory system of Claim 5, wherein the one or more capacitors comprises one or more double layered capacitors.

8. (Withdrawn) The memory system of Claim 5, wherein the one or more capacitors are charged by the first power supply while the memory system is in the first state.

9. (Withdrawn) The memory system of Claim 3, further comprising a printed circuit board, wherein the second power supply and the memory system are located on the printed circuit board.

10. (Withdrawn) The memory system of Claim 3, wherein the at least two states further comprise a third state in which power is supplied to the volatile memory subsystem from a third power supply.

11. (Withdrawn) The memory system of Claim 2, wherein the controller and the non-volatile memory subsystem do not add a significant capacitive load to the volatile memory system when the memory system is in the first state.

12. (Withdrawn) The memory system of Claim 1, wherein the volatile memory subsystem comprises one or more DRAM memory elements.

13. (Withdrawn) The memory system of Claim 1, wherein the volatile memory subsystem comprises one or more SRAM memory elements.

14. (Withdrawn) The memory system of Claim 1, wherein the non-volatile memory subsystem comprises one or more flash memory elements.

15. (Withdrawn) The memory system of Claim 1, wherein the memory system is implemented on a memory module.

16. (Withdrawn) The memory system of Claim 1, wherein the at least one circuit comprise one or more switches coupled to the controller, to the volatile memory subsystem, and to the host computer.

17. (Withdrawn) The memory system of Claim 1, wherein the volatile memory subsystem comprises a registered DIMM comprising one or more registers and a plurality of DRAM elements, wherein the one or more registers are coupled to the computer system.

18. (Withdrawn) The memory system of Claim 17, wherein the at least one circuit comprise one or more switches coupled to the one or more registers and to the plurality of DRAM elements and configured to selectively operatively couple the volatile memory subsystem and

to the computer system.

19. (Withdrawn) The memory system of Claim 17, wherein the one or more registers are coupled to the plurality of DRAM elements and the at least one circuit comprises one or more switches coupled to the one or more registers and to a power source for the one or more registers, wherein the one or more switches are configured to selectively operatively couple the one or more registers to the power source for the one or more registers.

20. (Withdrawn) The memory system of Claim 1, wherein the non-volatile memory subsystem comprises at least 100 percent more storage capacity than does the volatile memory subsystem.

21. (Withdrawn) A power module for providing a plurality of voltages to a memory system comprising non-volatile and volatile memory, the plurality of voltages comprising at least a first voltage and a second voltage, the power module comprising:

an input providing a third voltage to the power module;

a voltage conversion element configured to provide the second voltage to the memory system;

a first power element configured to selectively provide a fourth voltage to the conversion element;

a second power element configured to selectively provide a fifth voltage to the conversion element, wherein the power module is configured to selectively provide the first voltage to the memory system either from the conversion element or from the input, wherein the power module is configured to be operated in at least three states comprising:

a first state in which the first voltage is provided to the memory system from the input and the fourth voltage is provided to the conversion element from the first power element;

a second state in which the fourth voltage is provided to the conversion element from the first power element and the first voltage is provided to the memory system from the conversion element;

a third state in which the fifth voltage is provided to the conversion element from the second power element and the first voltage is provided to the memory system from the conversion element.

22. (Withdrawn) The power module of Claim 21, wherein the first power element comprises a pulse-width modulation power controller.

23. (Withdrawn) The power module of Claim 21, wherein the second power element does not comprise a battery.

24. (Withdrawn) The power module of Claim 21, wherein the second power element comprises one or more capacitors.

25. (Withdrawn) The power module of Claim 24, wherein the second power element comprises a battery and is configured to power the volatile memory for less than thirty minutes.

26. (Withdrawn) The power module of Claim 21, wherein the conversion element comprises one or more buck converters.

27. (Withdrawn) The power module of Claim 21, wherein the conversion element comprises one or more buck-boost converters.

28. (Withdrawn) A method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems, the method comprising:

during a first condition, providing the first voltage to the memory system from an input power supply and providing the second voltage to the memory system from a first power subsystem;

detecting a second condition;

during the second condition, providing the first voltage and the second voltage to the memory system from the first power subsystem;

charging a second power subsystem;

detecting a third condition;

during the third condition, providing the first voltage and the second voltage to the memory system from the second power subsystem.

29. (Withdrawn) The method of Claim 28, wherein detecting the second condition comprises detecting that a trigger condition is likely to occur.

30. (Withdrawn) The method of Claim 29, wherein detecting the third condition comprises detecting that the trigger condition has occurred.

31. (Withdrawn) The method of Claim 28, wherein the trigger condition comprises a power reduction.

32. (Withdrawn) The method of Claim 28, wherein the trigger condition comprises a power failure.

33. (Withdrawn) The method of Claim 28, wherein the trigger condition comprises a system hang-up.

34. (Withdrawn) The method of Claim 28, wherein the first power subsystem comprises a pulse-width modulation power controller and a voltage conversion subsystem.

35. (Withdrawn) The method of Claim 28, wherein the second power subsystem does not comprise a battery.

36. (Withdrawn) The method of Claim 35, wherein the second power subsystem comprises one or more capacitors and the voltage conversion subsystem.

37. (Original) A method of controlling a memory system operatively coupled to a host system and which includes a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

operating the volatile memory subsystem at a first frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;

operating the non-volatile memory subsystem at a second frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and

operating the volatile memory subsystem at a third frequency when the memory system is in the second mode of operation, the third frequency less than the first frequency.

38. (Original) The method of Claim 37, wherein the third frequency is approximately equal to the second frequency.

39. (Original) The method of Claim 37, wherein the memory system is not powered by a battery when it is in the second mode of operation.

40. (Currently Amended) The method of Claim [[7]] 37, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.

41. (Original) The method of Claim 40, wherein the trigger condition comprises a power failure condition.

42. (Original) The method of Claim 37, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.

43. (Withdrawn) A method of controlling a memory system operatively coupled to a host system and which includes a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

communicating data words between the volatile memory subsystem and the host system when the memory system is in a first mode of operation; and

transferring data words from the volatile memory subsystem to the nonvolatile memory subsystem when the memory system is in a second mode of operation, wherein transferring each data word comprises:

storing a first portion of the data word in a buffer;

storing a second portion of the data word in the buffer;

and writing the entire data word from the buffer to the non-volatile memory subsystem.

44. (Withdrawn) The method of Claim 43, wherein the transferring each data word further comprises storing a third portion of each data word in the buffer.

45. (Withdrawn) A memory system operatively coupled to a host system, comprising:

a volatile memory subsystem;

a non-volatile memory subsystem comprising at least 100 percent more storage capacity than does the volatile memory subsystem; and

a controller operatively coupled to the volatile memory subsystem and operatively coupled to the non-volatile memory subsystem, the controller configured to allow data to be communicated between the volatile memory subsystem and the host system when the memory system is operating in a first state and to allow data to be communicated between the volatile memory subsystem and the non-volatile memory subsystem when the memory system is opeiating in a second state.

46. (Withdrawn) The memory system of Claim 45, wherein power is supplied to the volatile memory subsystem from a first power supply when the memory system is in the first state.

47. (Withdrawn) The memory system of Claim 46, wherein power is supplied to the volatile memory subsystem from a second power supply when the memory system is in the second state.

48. (Withdrawn) The memory system of Claim 47, wherein the second power supply does not comprise a battery.

49. (Withdrawn) The memory system of Claim 45, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem, the non-volatile memory subsystem, and the controller are located on the printed circuit board.

50. (Withdrawn) A method of controlling a memory system operatively coupled to a host system and which includes a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

communicating data between the volatile memory subsystem and the host system when the memory system is in a first mode of operation;

storing a first copy of data from the volatile memory subsystem to the nonvolatile memory subsystem at a first time when the memory system is in a second mode of operation;

restoring the first copy of data from the non-volatile memory subsystem to the volatile memory subsystem;

erasing the first copy of data from the non-volatile memory subsystem; and

storing a second copy of data from the volatile memory subsystem to the non-volatile memory subsystem at a second time when the memory system is in the second mode of operation, wherein storing the second copy begins before the first copy is completely erased from the non-volatile memory subsystem.

51. (Withdrawn) The method of Claim 50, further comprising restoring the second copy of data from the non-volatile memory subsystem to the volatile memory subsystem.

52. (Withdrawn) The method of Claim 50, wherein the memory system enters the second mode of operation in response to a power failure.

53. (Withdrawn) The method of Claim 50, wherein the memory system is not powered by a battery when it is in the second mode of operation.

54. (Withdrawn) The method of Claim 50, wherein the first copy of data and the second copy of data are stored in separate portions of the non-volatile memory subsystem.

REMARKS

In response to the restriction/election requirement mailed March 31, 2011, applicant elects to prosecute Group III. At least the following claims read on the elected group: Claims 37-42.

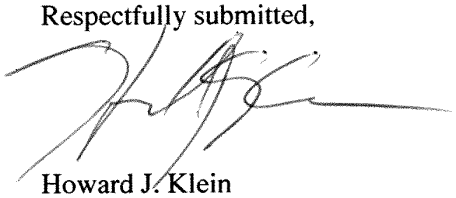
This election is made without traverse.

A Request for a One Month Extension of Time under 37 CFR 1.136(a) is submitted herewith, along with the fee prescribed by 37 CFR 1.17(a)(1).

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 11-1159 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,



Date: May 20, 2011

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Klein, O'Neill & Singh, LLP (Customer No.: 22145)
18200 Von Karman Avenue, Suit 725
Irvine, CA 92612
Tel: (949) 955-1920
Fax: (949) 955 1921

Electronic Patent Application Fee Transmittal

Application Number:	12240916
Filing Date:	29-Sep-2008
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Filer:	Howard J. Klein/Carrie Cheung
Attorney Docket Number:	987-004.201

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	1251	1	130	130

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**130**

Electronic Acknowledgement Receipt	
EFS ID:	10141197
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	22145
Filer:	Howard J. Klein/Carrie Cheung
Filer Authorized By:	Howard J. Klein
Attorney Docket Number:	987-004.201
Receipt Date:	20-MAY-2011
Filing Date:	29-SEP-2008
Time Stamp:	19:46:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$130
RAM confirmation Number	6239
Deposit Account	111159
Authorized User	CHEUNG,CARRIE A.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		987-004-201--RRRof03312011asFiled05202011.pdf	710587 7e2b20deb8661f44c60460364d2bb04cd1115084	yes	11

Multipart Description/PDF files in .zip description

Document Description	Start	End
Extension of Time	1	2
Response to Election / Restriction Filed	3	3
Claims	4	10
Applicant Arguments/Remarks Made in an Amendment	11	11

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	30306 eb01d48a823f3dcff6025d3b6e2400d64fa4a034	no	2

Warnings:

Information:

Total Files Size (in bytes):	740893

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Amendment Transmittal & Petition for Extension of Time under 37 CFR 1.136(a)

Docket Number
987-004.101

Address To
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Title of Invention

NON-VOLATILE MEMORY MODULE

First Named Inventor	Chi-She Chen
Application No.	12/240,916
Filing Date	September 29, 2008
Examiner	Midys Rojas
Art Unit	2185

Transmitted herewith is an amendment in the above-identified application.

This is also a petition under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above identified application.

The requested extension and fee are as shown below (check time period desired).

Fee Calculation

Extension of Time Fee

☒ One month (37 CFR 1.17(a)(1)) ☐ Two months (37 CFR 1.17(a)(2)) ☐ Three months (37 CFR 1.17(a)(3))
☐ Four months (37 CFR 1.17(a)(4)) ☐ Five months (37 CFR 1.17(a)(5))

Claims as Amended

For	#Filed	#Previously Paid For	#Extra	Rate	Fee
Total Claims	6	- 20 =		x 52 =	
Total Indep. Claims	1	- 3 =		x 220 =	
Multiple Dependent Claims (check if applicable) ☐					
				Extension Fee (from above)	$130
☐ Applicant claims small entity status. See 37 CFR 1.27.				**TOTAL**	$130

Method of Payment

☐ Deposit Account ☒ Credit Card ☐ Check ☐ Money Order ☐ Other: _____

Deposit Account Number 11-1159

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge the fee(s) set forth above
☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17
☐ Charge fee(s) indicated above, **except for the filing fee**
☒ Credit any overpayments
☒ If an additional extension of time is required, please consider this a petition therefor and charge any additional fees which may be required to the Deposit Account above.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on form PTO-2038.

Amount Grand Total _____ $130

Amendment Transmittal & Petition for Extension of Time under 37 CFR 1.136(a)	Docket Number
	987-004.101

Correspondence Address			
Customer Number	22145		
-OR-			
Name			
Address			
City		State	
Country		Postal Code	
Phone Number			
E-mail Address			

Certificate of Mailing by Express Mail

I hereby certify that this Amendment and Petition for Extension of Time, accompanying documents, and fee are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on the date indicated below:

(Date of Mailing)

(Typed or Printed Name of Person Mailing Correspondence)

(Signature of Person Mailing Correspondence)

("Express Mail" Mailing Label Number)

Certificate of Mailing by First Class Mail

I hereby certify that this Amendment and Petition for Extension of Time, accompanying documents, and fee are being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on the date indicated below:

(Date of Mailing) *(Name of Person Mailing Correspondence)*

(Signature of Person Mailing Correspondence)

Certificate of Transmission

I hereby certify that this Amendment and Petition for Extension of Time, accompanying documents, and fee authorization are being facsimile transmitted to the United States Patent and Trademark Office on the date indicated below:

(Date of Transmission) *(Name of Person Transmitting Correspondence)*

(Signature of Person Transmitting Correspondence)

Signature Instructions

Select the name of the person who will electronically sign the Amendment and Petition for Extension of Time from the drop-down box below.

If a practitioner is not present in the drop-down list, you must close this form and select 'Add Practitioner...' in the Form Manager's Utility menu.

Verify that the signatory information is correct and press the 'eSign' button to electronically sign the submission. If you prefer to sign the form manually, simply do not click the 'eSign' button; just print and manually sign.

Signatory Drop-Down Box Howard J. Klein

Name	Howard J. Klein		Registration Number	28727
Signatory Capacity	Attorney for Applicant(s)	E-mail Address		
eSign			Date Signed	5/20/2011

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/240,916	09/29/2008	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	05/20/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 54	Minus	** 54	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 7	Minus	***7	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/PATRICIA LEWIS/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/240,916	09/29/2008	Chi-She Chen	987-004.201	6240

22145 7590 07/29/2011
KLEIN, O'NEILL & SINGH, LLP
18200 VON KARMAN AVENUE
SUITE 725
IRVINE, CA 92612

EXAMINER	
ROJAS, MIDYS	
ART UNIT	**PAPER NUMBER**
2185	
MAIL DATE	**DELIVERY MODE**
07/29/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	12/240,916	CHEN ET AL.
	Examiner	Art Unit
	MIDYS ROJAS	2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-42* is/are pending in the application.

4a) Of the above claim(s) *1-36 and 43-54* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)	
1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/13/2009; 10/5/2009*.	6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 37-42 in the reply filed on 5/20/2011 is acknowledged.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 4/13/2009 and 10/5/2009 were considered by the examiner.

Drawings

The drawings received on 9/29/2008 have been accepted by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 37-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. [US 6,336,174], Applicant cited art, in view of Oshikiri [US 2007/0192627].

Claim 37, Li et al. discloses a method of controlling [via controller 206, Fig. 2] a memory system [hardware assisted memory module 104, of Fig. 1 and 2] operatively coupled to a host system [host system 100 including CPU 102, Fig. 1] and which includes a volatile memory subsystem [volatile memory 202, Fig. 2] and a non-volatile memory subsystem [nonvolatile memory 204, Fig. 2], the method comprising:

operating the volatile memory subsystem when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system [volatile memory 202 switches between modes of operation by switching isolation devices on/off in response to trigger events, see col. 6, lines 48-57; during normal operation, when the isolation devices are on, the HAMM behaves like a conventional memory module, see Abstract, and stores digital information received from the data bus of the host, see col. 3, lines 5-9 and col. 5, line 55 – col. 6, line 3, thus representing the first mode of operation claimed];

operating the non-volatile memory subsystem when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem [when a trigger event occurs, such as a system fault or a power failure, the HAMM isolates the volatile memory from the system memory bus by turning off isolation devices and isolating the HAMM from the host system. Then to store operation begins which includes copying data, address by address, from the volatile memory to the nonvolatile memory, see col. 9, lines 49-67].

Li et al. does not teach that in the first mode, the volatile memory operates at a first frequency while in the second mode, the non-volatile memory operates at a second frequency and the volatile memory operates at a third frequency that is less than the first frequency.

Oshikiri discloses a semiconductor memory 2 being used in an information processing apparatus 1 [Fig. 1] which switches between two operation modes [see par. 0029] wherein a first operation mode is detected when a first mode switching command

is received from the information processing apparatus [see par. 0031] and a second operation mode is detected when a second mode switching command is received from the information processing apparatus [see par. 0039]. In either operating mode, the information processing apparatus executes various processes in the semiconductor memory by using the CPU 11 and RAM 12 [par. 0021]. When the semiconductor memory operates in the second mode, it is operating at a lower level of security but at a higher processing speed, thus representing a higher operating frequency [par. 0040]. Therefore, when in the second mode, all elements accessing the memory operate at this higher operating frequency, thus representing the claimed first mode of operation [higher first frequency]. In Oshikiri's first mode, all elements operate at the lower operating speed, thus representing the claimed second mode of operation [lower second and third frequency]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Li et al. with the operating seed of Oshikiri since providing for memory operations in different frequencies depending on the memory mode provided since different operating speeds have different power requirements.

Claim 38, Li et al. in view of Oshikiri discloses the method of Claim 37, wherein the third frequency is approximately equal to the second frequency [In Oshikiri's first mode, all elements operate at the lower operating speed, thus representing the claimed second mode of operation, lower second and third frequency, par. 0031 and 0040]

Claim 39, Li et al. in view of Oshikiri discloses the method of Claim 37, wherein the memory system is not powered by a battery when it is in the second mode of operation [when the trigger condition that causes the switch of operation mode is a O/S hang-up, a backup battery is not required, see col. 7, lines 59-66 of Li et al.].

Claim 40, Li et al. in view of Oshikiri discloses the method of Claim 37, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition [detection of a trigger event, see Abstract of Li et al.].

Claim 41, Li et al. in view of Oshikiri discloses the method of Claim 40, wherein the trigger condition comprises a power failure condition [trigger event may be power failure, see Abstract of Li et al.].

Claim 42, Li et al. in view of Oshikiri discloses the method of Claim 37, wherein the memory system 104 further comprises a printed circuit board [as shown in Fig. 2 all elements are within one board] and the volatile memory subsystem 202 and the non-volatile memory subsystem 204 are located on the printed circuit board [see Fig. 2, and col. 2, line 58-col. 3, line 4].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MIDYS ROJAS whose telephone number is (571)272-4207. The examiner can normally be reached on M-TH 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Midys Rojas/
Primary Examiner, Art Unit 2185

MR

Notice of References Cited	Application/Control No. 12/240,916	Applicant(s)/Patent Under Reexamination CHEN ET AL.	
	Examiner MIDYS ROJAS	Art Unit 2185	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2007/0192627	08-2007	Oshikiri, Takashi	713/191
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12240916	CHEN ET AL.
	Examiner	Art Unit
	MIDYS ROJAS	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/28/2011								
	1	N								
	2	N								
	3	N								
	4	N								
	5	N								
	6	N								
	7	N								
	8	N								
	9	N								
	10	N								
	11	N								
	12	N								
	13	N								
	14	N								
	15	N								
	16	N								
	17	N								
	18	N								
	19	N								
	20	N								
	21	N								
	22	N								
	23	N								
	24	N								
	25	N								
	26	N								
	27	N								
	28	N								
	29	N								
	30	N								
	31	N								
	32	N								
	33	N								
	34	N								
	35	N								
	36	N								

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12240916	CHEN ET AL.
	Examiner	Art Unit
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✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
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☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/28/2011								
	37	✓								
	38	✓								
	39	✓								
	40	✓								
	41	✓								
	42	✓								
	43	N								
	44	N								
	45	N								
	46	N								
	47	N								
	48	N								
	49	N								
	50	N								
	51	N								
	52	N								
	53	N								
	54	N								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12240916	CHEN ET AL.
	Examiner	Art Unit
	MIDYS ROJAS	2185

SEARCHED			
Class	Subclass	Date	Examiner
711	160, 161, 162	7/28/2011	Mr
710	10	7/28/2011	Mr

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search: limited search of 711/160, 161, 162; 710/10; and text searches	7/28/2011	Mr
PALM inventor name search		Mr

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

	/MIDYS ROJAS/ Primary Examiner.Art Unit 2185

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4347	((711/162) or (711/160) or (711/161) or (710/10)).CCLS.	USPAT; USOCR	OR	OFF	2011/07/28 19:20
L2	0	L1 and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/28 19:21
L3	1	L1 and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 19:21
S1	0	("("20020083368" | "20040190210" | "4420821" | "4449205" | "5519663" | "6158015" | "6336174" | "6336176" | "6487623" | "6658507" | "6799244" | "7409590").PN.").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/27 15:21
S2	12	("20020083368" | "20040190210" | "4420821" | "4449205" | "5519663" | "6158015" | "6336174" | "6336176" | "6487623" | "6658507" | "6799244" | "7409590").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:21
S3	0	host same (volatile with non-volatile with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:34
S4	1	(volatile with non-volatile with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:34
S5	87	(memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:35
S6	56	"711"/$.ccls. and (memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:35
S7	1013	memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:44
S8	128	"711"/$.ccls. and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2011/07/27 15:44

			JPO			
S9	46	("4072852" | "4815074" | "4959774" | "5283792" | "5379431" | "5799200").PN. OR ("6336174").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/27 15:44
S10	8	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) with (frequency or speed or clock)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:08
S11	2	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:09
S12	0	memory same (host near3 frequency) same (non-volatile near3 frequency) same mode	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:11
S13	1	(memory with mode) same (host with frequency) same (non-volatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:12
S14	6	(memory with mode) same (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:12
S15	13	"711"/$.ccls. and (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:14
S16	40	"711"/$.ccls. and (host with speed) same (nonvolatile with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:22
S17	16	"711"/$.ccls. and (host with speed) same (backup with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:23
S18	50	(backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:29
S19	48	power and (backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:29
S20	14	(power near3 (loss or fail$3)) and (backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:30
S21	8	(power near3 (loss or fail$3)) and (copy$3 or tranfer$3) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:38
S22	8	"711"/$.ccls. and (copy$3 or tranfer$3 or back-up or (back adj up)) with (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:41
S23	88	"711"/$.ccls. and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:44

EAST Search History (Interference)

< This search history is empty>

7/28/2011 7:22:23 PM
C:\Users\mrojas\Documents\EAST\Workspaces\12240916.wsp

PTO/SB/08a(07-05)
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	1

Complete if Known

Application Number	12/240,916
Filing Date	September 29, 2008
First Named Inventor	Chi-She Chen
Art Unit	2189
Examiner Name	Unknown

Attorney Docket No: 987-04-CON-H

US PATENT DOCUMENTS

Examiner Initial *	Cite No	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
/M.R./		4,420,821	12-13-1983	Hoffman	02-19-1982
		4,449,205	05-15-1984	Hoffman	02-19-1982
		5,519,663	05-21-1996	Harper, Jr. et al.	09-28-1994
		6,158,015	12-05-2000	Klein	03-30-1998
		6,336,176	01-01-2002	Li et al.	08-09-1999
		6,487,623	11-26-2002	Emerson et al.	04-30-1999
		6,658,507	12-02-2003	Chan	08-31-1998
		6,799,244	09-28-2004	Tanaka et al.	12-06-2002
		2002/0083368	06-27-2002	Abe et al.	12-20-2001
		2004/0190210	09-30-2004	Leete	03-26-2003

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

EXAMINER	/Midys Rojas/	DATE CONSIDERED	07/27/2011

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.R./

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

	Complete if Known
Application Number	12/240,916
Filing Date	September 29, 2008
First Named Inventor	Chi-She Chen
Art Unit	2189
Examiner Name	Unknown
IDS Filing Date	October 5, 2009

Sheet	1	of	1	Attorney Docket No: 987-04-CON-H

US PATENT DOCUMENTS

Examiner Initial *	Cite No	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
/M.R./		6,336,174	01-01-2002	Li et al.	08-09-1999
/M.R./		7,409,590	08-05-2008	Moshayedi et al.	07-28-2006

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

EXAMINER /Midys Rojas/ **DATE CONSIDERED** 07/27/2011

Substitute Disclosure Statement Form (PTO-1449)
[1] EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.R./

PTO/SB/81 (01-09)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Application Number	12/240,916
Filing Date	2008-09-29
First Named Inventor	Chi-She Chen
Title	Non-volatile Memory Module
Art Unit	2185
Examiner Name	Midys Rojas
Attorney Docket Number	062453-002

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

46,188

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant/inventor.

OR

☒ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____

SIGNATURE of Applicant or Assignee of Record

Signature		Date	9/1/11
Name	Gail Sasaki	Telephone	
Title and Company	Vice-president and Chief Financial Officer, Netlist, Inc.		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Netlist, Inc.

Application No./Patent No.: 12/240,916 Filed/Issue Date: September 29, 2008

Titled:
NON-VOLATILE MEMORY MODULE

Netlist, Inc. , a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. [x] the assignee of the entire right, title, and interest in;

2. [ ] an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or

3. [ ] the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. [x] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy therefore is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet(s).

[ ] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Khaled Shami/	September 7, 2011
Signature	Date
Khaled Shami	Attorney of Record
Printed or Typed Name	Title

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Application No.: 12/131,873
Filing Date: June 2, 2008

ASSIGNMENT

WHEREAS, We, Chi-She Chen, a Taiwanese citizen, residing at 944 Crystal Water Lane, Walnut, CA 91789; Jeffrey C. Solomon, a United States citizen, residing at 16 Silver Fir, Irvine, CA 92604; Scott Milton, a United States citizen, residing at 49 Statehouse Place, Irvine, CA 92602; and Jayesh Bhakta, a United States citizen, residing at 12220 Rose Street, Cerritos, CA 90703, have invented certain new and useful improvements in a NON-VOLATILE MEMORY MODULE for which we have filed an application for Letters Patent in the United States, Application No. 12/131,873, Filed on June 2, 2008;

AND WHEREAS, Netlist, Inc. (hereinafter "ASSIGNEE"), a Delaware Corporation, with its principal place of business at 51 Discovery, Ste #150, Irvine, CA 92618, desires to acquire the entire right, title, and interest in and to said improvements and said Application:

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, we, the inventors, do hereby acknowledge that we have sold, assigned, transferred and set over, and by these presents do hereby sell, assign, transfer and set over, unto said ASSIGNEE, its successors, legal representatives and assigns, the entire right, title, and interest throughout the world in, to and under said improvements, and said application including all provisional applications relating thereto (including but not limited to U.S. Provisional Application No. 60/941,586, filed June 1, 2007), and all divisions, renewals and continuations thereof, and all Letters Patent of the United States which may be granted thereon and all reissues and extensions thereof, and all rights of priority under International Conventions and applications for Letters Patent which may hereafter be filed for said improvements in any country or countries foreign to the United States, and all Letters Patent which may be granted for said improvements in any country or countries foreign to the United States and all extensions, renewals and reissues thereof; and we hereby authorize and request the Commissioner of Patents of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said improvements to said ASSIGNEE, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND WE DO HEREBY sell, assign, transfer, and convey to ASSIGNEE, its successors, legal representatives, and assigns all claims for damages and all remedies arising out of any violation of the rights assigned hereby that may have accrued prior to the date of assignment to ASSIGNEE, or may accrue hereafter, including, but not limited to, the right to sue for, collect, and retain damages for past infringements of said Letters Patent before or after issuance.

AND WE HEREBY covenant and agree that we will communicate to said ASSIGNEE, its successors, legal representatives and assigns, any facts known to us respecting said improvements, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing and reissue applications, make all rightful oaths and generally do everything possible to aid said ASSIGNEE, its successors, legal representatives and assigns, to obtain and enforce proper patent protection for said improvements in all countries.

SEE ATTACHED ACKNOWLEDGMENT

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 24th day of October, 2008.

Chi-She Chen

STATE OF California
COUNTY OF Orange } ss.

On October 24, 2008, before me, Dennis B. Ginther, notary public, personally appeared Chi-She Chen who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(ies), and that by his signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

[SEAL]

DENNIS B. GINTHER
Commission # 1648822
Notary Public - California
Orange County
My Comm. Expires Mar 30, 2010

Notary Signature

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 22nd day of October, 2008.

Jeffrey C. Solomon

STATE OF California }
COUNTY OF Orange } ss.

On October 22, 2008, before me, Dennis B. Ginther, notary public, personally appeared Jeffrey C. Solomon who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/~~are~~ subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(~~ies~~), and that by his signature(~~s~~) on the instrument the person(~~s~~), or the entity upon behalf of which the person(~~s~~) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

[SEAL]

DENNIS B. GINTHER
Commission # 1648822
Notary Public - California
Orange County
My Comm. Expires Mar 30, 2010

Notary Signature

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 24 day of October, 2008.

Scott H. Milton
Scott Milton

STATE OF California }
COUNTY OF Orange } ss.

On October 24, 2008, before me Dennis B. Ginther, notary public, personally appeared Scott Milton who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/~~are~~ subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(~~ies~~), and that by his signature(~~s~~) on the instrument the person(~~s~~), or the entity upon behalf of which the person(~~s~~) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

[SEAL]

DENNIS B. GINTHER
Commission # 1648822
Notary Public - California
Orange County
My Comm. Expires Mar 30, 2010

Notary Signature

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 22 day of October, 2008.

Jayesh Bhakta

Jayesh Bhakta

STATE OF California }
COUNTY OF Orange } ss.

On October 22, 2008 before me Dennis B. Ginther, notary public, personally appeared Jayesh Bhakta who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/~~are~~ subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(~~ies~~), and that by his signature(~~s~~) on the instrument the person(~~s~~), or the entity upon behalf of which the person(~~s~~) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

[SEAL]

Notary Signature

DENNIS B. GINTHER
Commission # 1648822
Notary Public - California
Orange County
My Comm. Expires Mar 30, 2010

5619488

Electronic Acknowledgement Receipt

EFS ID:	10892151
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	22145
Filer:	Khaled Shami
Filer Authorized By:	
Attorney Docket Number:	987-004.201
Receipt Date:	07-SEP-2011
Filing Date:	29-SEP-2008
Time Stamp:	13:08:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	executed_POA.pdf	786534 f3fdb296722a812ecc166ffd91530418e76f028f	no	2

Warnings:	
Information:	

2	Assignee showing of ownership per 37 CFR 3.73(b).	3_73_wa_statement.pdf	1057450 b67aa7077f37cc10a89659f8dd85732f60a22746	no	7

Warnings:	
Information:	
Total Files Size (in bytes):	1843984

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/240,916	09/29/2008	Chi-She Chen	062453-002

CONFIRMATION NO. 6240

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POA ACCEPTANCE LETTER

OC000000049807666

Date Mailed: 09/15/2011

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/07/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/ddinh/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/240,916	09/29/2008	Chi-She Chen	987-004.201

CONFIRMATION NO. 6240

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POWER OF ATTORNEY NOTICE

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Date Mailed: 09/15/2011

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/07/2011.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/ddinh/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Chen et al. CONFIRMATION NO.: 6240

SERIAL NO.: 12/240,916

FILING DATE: September 29, 2008

TITLE: NON-VOLATILE MEMORY MODULE

EXAMINER: ROJAS, Midys

ART UNIT: 2185

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND/OR REPLY TO OFFICE ACTION

Sir:

In response to the Office Action mailed July 29, 2011, please amend the subject application as indicated.

Amendments to the Specification begin on page **2**.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page **8**.

Remarks begin on page **14**.

In the Specification

Please amend paragraph [0039] as follows:

[0039] Certain embodiments described herein utilize the non-volatile memory subsystem 40 as a flash "mirror" to provide backup of the volatile memory subsystem 30 in the event of certain system conditions. For example, the non-volatile memory subsystem 40 may backup the volatile memory subsystem 30 in the event of a trigger condition, such as, for example, a power failure or power reduction or a request from the host system. In one embodiment, the non-volatile memory subsystem 30 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition. In certain embodiments, the trigger condition occurs when the memory system 10 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. In various embodiments, a backup and/or restore operation may occur in reboot and/or non-reboot trigger conditions.

Please amend paragraph [0047] as follows:

[0047] When operating in the first state, in certain embodiments, the step-up transformer 82 keeps the capacitor bank 86 charged at a peak value. In certain embodiments, the step-down transformer 84 acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 32 and 3.0V to the non-volatile flash memory elements 42) when operating in the second state (e.g., during power down). In certain embodiments, as schematically illustrated by Figures 1-3, the memory module 10 further comprises a switch 90 (e.g., FET switch) that

switches power provided to the controller 62, the volatile memory subsystem 30, and the non-volatile memory subsystem 40, between the power from the second power supply 80 and the power from the first power supply (e.g., system power) received via the interface 22. For example, the switch 90 may switch from the first power supply to the second power supply 80 when the voltage monitor 50 detects a low voltage condition. The switch 90 of certain embodiments advantageously ensures that the volatile memory elements 32 and non-volatile memory elements 42 are powered long enough for the data to be transferred from the volatile memory elements 32 and stored in the non-volatile memory elements 42. In certain embodiments, after the data transfer is complete, the switch 90 then switches back to the first power supply and the controller 62 transmits a signal to ~~a the~~ at least one circuit 50 to operatively decouple the controller 62 from the volatile memory subsystem 30, such that the memory system 10 re-enters the first state.

Please amend paragraph [0050] as follows:

[0050] The memory system 10 generally operates as a write-back cache in certain embodiments. For example, in one embodiment, the host system (e.g., a disk controller) writes data to the volatile memory subsystem 30 which then writes the data to non-volatile storage which is not part of the memory system 10, such as, for example, a hard disk. The disk controller may wait for an acknowledgment signal from the memory system 10 indicating that the data has been written to the hard disk or is otherwise secure. The memory system 10 of certain embodiments can decrease delays in the system operation by indicating that the data has been written to the hard disk before it has actually done so. In certain embodiments, the memory system 10 will still be able to recover the data efficiently in the event of a power outage because of the backup and restore capabilities described herein. In certain other embodiments, the memory system 10 may be operated as a write-through cache or as some other type of cache.

Please amend paragraph [0053] as follows:

[0053] The power module 100 further comprises a second power element 140 can be configured to selectively provide a fifth voltage 112 to the conversion element 120. The power module 100 can be configured to selectively provide the first voltage 102 to the memory system ~~110~~10 either from the conversion element 120 or from the input 106.

Please amend paragraph [0059] as follows:

[0059] Figure 6 is a flowchart of an example method 200 of providing a first voltage 102 and a second voltage 104 to a memory system 10 including volatile and nonvolatile memory subsystems 30, 40. While the method 200 is described herein by reference to the memory system 10 schematically illustrated by Figures 1-4, other memory systems are also compatible with embodiments of the method 200. During a first condition, the method 200 ~~at~~ comprises providing the first voltage 102 to the memory system 10 from an input power supply 106 and providing the second voltage 104 to the memory system 10 from a first power subsystem in operational block 210. For example, in one embodiment, the first power subsystem comprises the first power element 130 and the voltage conversion element 120 described above with respect to Figure 4. In other embodiments, other first power subsystems are used.

Please amend paragraph [0069] as follows:

[0069] In some embodiments, the memory system 10 enters the second mode of operation in response to a trigger condition, such as a power failure. In certain embodiments, the first copy of data and the second copy of data are stored in separate portions of the nonvolatile memory subsystem 40. The method 300 can also include restoring the second copy of data from the non-volatile memory subsystem 40 to the volatile memory subsystem 30 in an operational block 360. The operational blocks of method 300 referred to herein may be performed in different orders in various embodiments. For example, in some embodiments, ~~the restoring~~ the second copy of data is restored to the volatile memory subsystem

30 at operational block 360 before the first copy of data is completely erased in the operational block 340.

Please amend paragraph [0073] as follows:

[0073] In one embodiment, the backup clock 408 and the volatile memory system clock signal 420 are received by a multiplexer 422, as schematically illustrated by Figure ~~7~~8. The multiplexer 422 can output either the volatile memory system clock signal 420 or the backup clock signal 408 depending on the backup state of the memory system 10. For example, when the memory system 10 is not performing a backup or restore operation and is communicating with the host system (e.g., normal operation), the volatile memory system clock signal 420 may be provided by the multiplexer 422 to the volatile memory PLL block 424. When the memory system 10 is performing a backup (or restore) operation, the backup clock signal 408 may be provided.

Please amend paragraph [0075] as follows:

[0075] The clock signal 430 may be used by the controller 62 to generate and distribute clock signals which will be used by controller logic which is configured to control the volatile memory subsystem 30. For example, control logic in the controller 62 may be used to control the volatile memory subsystem 30 during a backup or restore operation. The clock signal 430 may be used as a reference clock signal for the PLL block 434 which can generate one or more clocks 438 used by logic in the controller 62. For example, the PLL block ~~424~~434 may generate one or more clock signals 438 used to drive logic circuitry associated with controlling the volatile memory subsystem 30. In certain embodiments, the PLL block 434 includes a feedback clock signal 436 and operates in a similar manner to other PLL blocks described herein.

Please amend paragraph [0077] as follows:

[0077] While described with respect to the example embodiment of Figure ~~7~~8, various alternative clock distribution topologies are possible. For example, one or more of the clock signals have a different frequency in various other embodiments. In some embodiments, one or more of the clocks shown as differential signals are single ended signals. In one embodiment, the volatile memory subsystem 30 operates on the volatile memory clock signal 420 and there is no backup clock signal 408. In some embodiments, the volatile memory subsystem 30 is operated at a reduced frequency during a backup operation and not during a restore operation. In other embodiments, the volatile memory subsystem 30 is operated at a reduced frequency during a restore operation and not during a backup operation.

Please amend paragraph [0078] as follows:

[0078] **Figure 9** is a flowchart of an example method 500 of controlling a memory system 10 operatively coupled to a host system. Although described with respect to the memory system 10 described herein, ~~with respect to Figures 1-3 and 7,~~ the method 500 is compatible with other memory systems. The memory system 10 may include a clock distribution topology 400 similar to the one described above with respect to Figure ~~7~~8 or another clock distribution topology. The memory system 10 can include a volatile memory subsystem 30 and a non-volatile memory subsystem 40.

Please amend paragraph [0079] as follows:

[0079] In an operational block 510, the method 500 comprises operating the volatile memory subsystem ~~40~~30 at a first frequency when the memory system 10 is in a first mode of operation in which data is communicated between the volatile memory subsystem 30 and the host system. In an operational block 520, the method 500 comprises operating the non-volatile memory subsystem 40 at a second

frequency when the memory system 10 is in a second mode of operation in which data is communicated between the volatile memory subsystem 30 and the non-volatile memory subsystem 40. The method 500 further comprises operating the volatile memory subsystem 30 at a third frequency in an operational block 530 when the memory system 10 is in the second mode of operation. In certain embodiments, the memory system 10 is not powered by a battery when it is in the second mode of operation. The memory system 10 may switch from the first mode of operation to the second mode of operation in response to a trigger condition. The trigger condition may be any trigger condition described herein such as, for example, a power failure condition. In certain embodiments, the second mode of operation includes both backup and restore operations as described herein. In other embodiments, the second mode of operation includes backup operations but not restore operations. In yet other embodiments, the second mode of operation includes restore operations but not backup operations.

In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1-36. (Canceled)

37. (Currently amended) A method ~~of~~ for controlling a memory system operatively coupled to a host system ~~and which includes~~, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

operating the volatile memory subsystem at a first frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;

operating the non-volatile memory subsystem at a second frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and

operating the volatile memory subsystem at a third frequency when the memory system is in the second mode of operation, the third frequency being less than the first frequency.

38. (Original) The method of Claim 37, wherein the third frequency is approximately equal to the second frequency.

39. (Original) The method of Claim 37, wherein the memory system is not powered by a battery when it is in the second mode of operation.

40. (Currently amended) The method of Claim ~~7~~37, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.

41. (Original) The method of Claim 40, wherein the trigger condition comprises a power failure condition.

42. (Original) The method of Claim 37, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.

43-54. (Canceled)

55. (New) The method of claim 40, wherein the trigger condition is a request by the host system.

56. (New) The method of claim 40, wherein the trigger condition is a system hang-up.

57. (New) The method of claim 40, wherein the trigger condition is a power reduction.

58. (New) The method of claim 40, wherein the trigger condition is a drop below a voltage threshold.

59. (New) The method of claim 40, wherein the trigger condition is a rise above a voltage threshold.

60. (New) The method of claim 40, wherein the trigger condition is a drop below a first voltage threshold or a rise above a second voltage threshold.

61. (New) The method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation.

62. (New) The method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation.

63. (New) The method of claim 62, wherein the backup operation is conducted on a regular basis.

64. (New) The method of claim 63, wherein the backup operation is initiated in response to a trigger event.

65. (New) The method of claim 37, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem.

66. (New) The method of claim 37, wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem.

67. (New) The method of claim 37, wherein one or more of the first, second or third frequencies is configurable by the memory system.

68. (New) The method of claim 37, wherein one or more of the first, second or third frequencies is configurable by a user.

69. (New) A memory system operatively coupled to a host system, the memory system comprising:

a volatile memory subsystem operable at a first frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system; and

a non-volatile memory subsystem operable at a second frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem,

the volatile memory subsystem further being operable at a third frequency when the memory system is in the second mode of operation, the third frequency being less than the first frequency.

70. (New) The memory system of claim 69, further comprising:

a controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation.

71. (New) The memory system of claim 69, further comprising a plurality of power supplies and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation.

72. (New) The memory system of claim 69, wherein the third frequency is approximately equal to the second frequency.

73. (New) The memory system of claim 69, wherein the memory system is not powered by a battery when it is in the second mode of operation.

74. (New) The memory system of claim 69, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.

75. (New) The memory system of claim 74, wherein the trigger condition comprises a power failure condition.

76. (New) The memory system of claim 69, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.

77. (New) The memory system of claim 74, wherein the trigger condition is a request by the host system.

78. (New) The memory system of claim 74, wherein the trigger condition is a system hang-up.

79. (New) The memory system of claim 74, wherein the trigger condition is a power reduction.

80. (New) The memory system of claim 74, wherein the trigger condition is drop below a voltage threshold.

81. (New) The memory system of claim 74, wherein the trigger condition is rise above a voltage threshold.

82. (New) The memory system of claim 74, wherein the trigger condition is a drop below a first voltage threshold or a rise above a second voltage threshold.

83. (New) The memory system of claim 69, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation.

84. (New) The memory system of claim 69, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation.

85. (New) The memory system of claim 84, wherein the backup operation is conducted on a regular basis.

86. (New) The memory system of claim 85, wherein the backup operation is initiated in response to a trigger event.

87. (New) The memory system of claim 69, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem.

88. (New) The memory system of claim 69, wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem.

89. (New) The memory system of claim 69, wherein one or more of the first, second or third frequencies is configurable by the memory system.

90. (New) The memory system of claim 69, wherein one or more of the first, second or third frequencies is configurable by a user.

REMARKS

The Office Action mailed July 29, 2011, has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Canceled Claims

Claims 1-36 and 43-54 have been canceled without prejudice or disclaimer of the subject matter contained therein.

Rejection(s) Under 35 U.S.C. § 103(a)

Claims 37-42 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. pat. no. 6,336,174 to Li *et al.* (hereinafter, "Li") in view of U.S. pat. pub. no. 2007/0192627 to Oshikiri (hereinafter, "Oshikiri").

The Office action acknowledges Li's failure to "teach that in the first mode, the volatile memory operates at a first frequency while in the second mode, the non-volatile memory operates at a second frequency and the volatile memory operates at a third frequency that is less than the first frequency." The Office action asserts that this feature can be found in Oshikiri, and the combination of these two references to achieve the claimed invention would have been obvious to one of ordinary skill in the art at the time the invention was made.

The Office action correctly points out that Oshikiri operates in two different modes—a high security mode and a low security mode. These modes impose different computational burdens, and therefore result in different processing speeds. (See for example Oshikiri at col.1 lines 33-37, stating "When a command is encrypted, however, the processing speed disadvantageously decreases. That is because the encrypted command needs to be decrypted by using a predetermined algorithm and the load of this processing is heavy.") Operation in the low security mode, being less resource-intensive,

naturally results in a higher processing speed (faster) than operation in the high security mode, which is more resource-intensive and therefore slower. Importantly, however, the different processing speeds do not equate to different memory subsystem operation frequency. In claim 37, memory subsystem operation frequencies, which can be thought of as their data or bit rates, can vary depending on the mode of operation. There is no indication in Oshikiri that the memory subsystem operation frequency is different in the two modes, and it is precisely because the memory subsystem operation frequencies are the same in Oshikiri that processing occurs more slowly for the computationally-intensive mode. If the memory subsystem operation frequencies were different, or were controllable or adjustable, then an increased memory subsystem operation frequency could be used to compensate for the greater computational burden, and a constant processing speed could be maintained. Therefore Oshikiri fails to remedy Li's admitted failure to disclose "that in the first mode, the volatile memory operates at a first frequency while in the second mode, the non-volatile memory operates at a second frequency and the volatile memory operates at a third frequency that is less than the first frequency." Accordingly, even if Li and Oshikiri were properly combinable, which is not conceded, the presently claimed invention would not result. The rejection of claim 37-42 under 35 U.S.C. § 103(a) based on the combination of Li and Oshikiri is therefore improper and its withdrawal is respectfully requested.

Newly-Added Claims

Claims 55-91 have been added to further particularly point out and distinctly claim the subject matter regarded as the invention. With respect to claim 69 *et seq*, these are apparatus counterparts to method claim 39 *et seq* and are patentable for at least the same reasons.

Conclusion

In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 50-3557.

Respectfully submitted,
NIXON PEABODY LLP

Dated: October 18, 2011

/Khaled Shami/
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Reg. No. 38,745

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Electronic Acknowledgement Receipt

EFS ID:	11212191
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-002
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		062453_002_Resp_to_OA.pdf	149948 76fe5026b04352c91a2788735572a99546eae43c	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Specification	2	7
	Claims	8	13
	Applicant Arguments/Remarks Made in an Amendment	14	16
Warnings:			
Information:			
	Total Files Size (in bytes):	149948	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/240,916	09/29/2008	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	10/18/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 42	Minus	** 54	= 0	X $ =		OR	X $60=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***7	= 0	X $ =		OR	X $250=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/ANDREA FREEMAN/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/240,916	09/29/2008	Chi-She Chen	062453-002	6240

46188 7590 02/01/2012

Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER	
ROJAS, MIDYS	
ART UNIT	**PAPER NUMBER**
2185	

NOTIFICATION DATE	DELIVERY MODE
02/01/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentsv@nixonpeabody.com
ocastanon@nixonpeabody.com

Office Action Summary	Application No.	Applicant(s)
	12/240,916	CHEN ET AL.
	Examiner	Art Unit
	MIDYS ROJAS	2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2011*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-54, 61-76, 83-90* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *55-60 and 77-82* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)	
1) ☐ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 10/18/2011 have been fully considered but they are not persuasive.

Applicant argues that Oshikiri does not teach the claimed different operating frequencies because although it does disclose different processing speeds when operating in different modes, the memories still operate at the same frequency during both modes. The examiner disagrees. The claimed subject matter requires the operation frequency of the memory subsystem to be different in different operation modes. The memory subsystem includes more elements than just a memory. Since Oshikiri discloses that the memory system operates at a high processing speed in one mode and at a low processing speed in another mode, this teaching correlates to the changes in speeds and operating frequencies of the entire memory subsystem (as claimed) when operating in different modes. It does not represent the operating speed of just the memory. The claim is not directed to the operating speed of a memory, but instead it is drawn to the operating speed of a memory subsystem.

Election/Restrictions

Newly submitted claims 55-60 and 77-82 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

These claims are drawn to different embodiments for the claimed trigger condition. However, the originally presented invention states that the trigger condition is a power failure [Claim 41].

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 55-60 and 77-82 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 63 and 85 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what time interval of operation is defined by "the backup operation is conducted on a regular basis". The term "regular basis" does not clearly define when the backup operations occur.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 37-42, 61-62, 64-76, 83-84, and 86-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. [US 6,336,174], Applicant cited art, in view of Oshikiri [US 2007/0192627].

Claim 37, Li et al. discloses a method of controlling [via controller 206, Fig. 2] a memory system [hardware assisted memory module 104, of Fig. 1 and 2] operatively coupled to a host system [host system 100 including CPU 102, Fig. 1] and which includes a volatile memory subsystem [volatile memory 202, Fig. 2] and a non-volatile memory subsystem [nonvolatile memory 204, Fig. 2], the method comprising:

operating the volatile memory subsystem when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system [volatile memory 202 switches between modes of operation by switching isolation devices on/off in response to trigger

events, see col. 6, lines 48-57; during normal operation, when the isolation devices are on, the HAMM behaves like a conventional memory module, see Abstract, and stores digital information received from the data bus of the host, see col. 3, lines 5-9 and col. 5, line 55 – col. 6, line 3, thus representing the first mode of operation claimed];

operating the non-volatile memory subsystem when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem [when a trigger event occurs, such as a system fault or a power failure, the HAMM isolates the volatile memory from the system memory bus by turning off isolation devices and isolating the HAMM from the host system. Then to store operation begins which includes copying data, address by address, from the volatile memory to the nonvolatile memory, see col. 9, lines 49-67].

Li et al. does not teach that in the first mode, the volatile memory operates at a first frequency while in the second mode, the non-volatile memory operates at a second frequency and the volatile memory operates at a third frequency that is less than the first frequency.

Oshikiri discloses a semiconductor memory 2 being used in an information processing apparatus 1 [Fig. 1] which switches between two operation modes [see par. 0029] wherein a first operation mode is detected when a first mode switching command is received from the information processing apparatus [see par. 0031] and a second operation mode is detected when a second mode switching command is received from the information processing apparatus [see

par. 0039]. In either operating mode, the information processing apparatus executes various processes in the semiconductor memory by using the CPU 11 and RAM 12 [par. 0021]. When the semiconductor memory operates in the second mode, it is operating at a lower level of security but at a higher processing speed, thus representing a higher operating frequency [par. 0040]. Therefore, when in the second mode, all elements accessing the memory operate at this higher operating frequency, thus representing the claimed first mode of operation [higher first frequency]. In Oshikiri's first mode, all elements operate at the lower operating speed, thus representing the claimed second mode of operation [lower second and third frequency]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Li et al. with the operating seed of Oshikiri since providing for memory operations in different frequencies depending on the memory mode provided since different operating speeds have different power requirements.

Claim 38, Li et al. in view of Oshikiri discloses the method of Claim 37, wherein the third frequency is approximately equal to the second frequency [In Oshikiri's first mode, all elements operate at the lower operating speed, thus representing the claimed second mode of operation, lower second and third frequency, par. 0031 and 0040]

Claim 39, Li et al. in view of Oshikiri discloses the method of Claim 37, wherein the memory system is not powered by a battery when it is in the second mode of operation [when the trigger condition that causes the switch of operation

mode is a O/S hang-up, a backup battery is not required, see col. 7, lines 59-66 of Li et al.].

Claim 40, Li et al. in view of Oshikiri discloses the method of Claim 37, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition [detection of a trigger event, see Abstract of Li et al.].

Claim 41, Li et al. in view of Oshikiri discloses the method of Claim 40, wherein the trigger condition comprises a power failure condition [trigger event may be power failure, see Abstract of Li et al.].

Claim 42, Li et al. in view of Oshikiri discloses the method of Claim 37, wherein the memory system 104 further comprises a printed circuit board [as shown in Fig. 2 all elements are within one board] and the volatile memory subsystem 202 and the non-volatile memory subsystem 204 are located on the printed circuit board [see Fig. 2, and col. 2, line 58-col. 3, line 4].

Claim 61, Li et al. in view of Oshikiri discloses the method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation [volatile memory 202 switches between modes of operation by switching isolation devices on/off in response to trigger events, see col. 6, lines 48-57; during normal operation, when the isolation devices are on, the HAMM behaves like a conventional memory module, see Abstract, and stores digital information received from the data bus of the host, see col. 3, lines 5-9

and col. 5, line 55 – col. 6, line 3, thus representing the first mode of operation claimed, Li et al.].

Claim 62, Li et al. in view of Oshikiri discloses the method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation [when a trigger event occurs, such as a system fault or a power failure, the HAMM isolates the volatile memory from the system memory bus by turning off isolation devices and isolating the HAMM from the host system. Then to store operation begins which includes copying data, address by address, from the volatile memory to the nonvolatile memory, see col. 9, lines 49-67, Li et al.].

Claim 64, Li et al. in view of Oshikiri discloses the method of claim 63, wherein the backup operation is initiated in response to a trigger event [when a trigger event occurs, such as a system fault or a power failure, the HAMM isolates the volatile memory from the system memory bus by turning off isolation devices and isolating the HAMM from the host system. Then to store operation begins which includes copying data, address by address, from the volatile memory to the nonvolatile memory, see col. 9, lines 49-67, Li et al.].

Claim 65, Li et al. in view of Oshikiri discloses the method of claim 37, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem [when a trigger event occurs, such as a system fault or a power failure, the HAMM isolates the volatile memory from the system memory bus by turning off isolation devices and isolating the HAMM from the host

system. Then to store operation begins which includes copying data, address by address, from the volatile memory to the nonvolatile memory, see col. 9, lines 49-67, Li et al.].

Claim 66, Li et al. in view of Oshikiri discloses the method of claim 37, wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem [Restoring from the HAMM, see Abstract of Li et al.].

Claim 67, Li et al. in view of Oshikiri discloses the method of claim 37, wherein one or more of the first, second or third frequencies is configurable by the memory system [frequency changing commands are received from the information processing apparatus, Oshikiri par. 0029, 0031, 0039; therefore, they are being configured by the information processing apparatus. In this case, the information processing apparatus is part of a memory system].

Claim 68, Li et al. in view of Oshikiri discloses the method of claim 37, wherein one or more of the first, second or third frequencies is configurable by a user [frequency changing commands are received from the information processing apparatus, Oshikiri par. 0029, 0031, 0039; therefore, they are being configured by the information processing apparatus. In this case, the information processing apparatus is a user of an operation mode switching command generated by the CPU in order to perform this mode switch].

Claim 69 is rejected using the same rationale as that of Claim 37.

Claim 70, Li et al. in view of Oshikiri discloses the memory system of claim 69, further comprising: a controller configured to decouple the non-volatile

memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation [trigger event causes the HAMM to isolate is self, therefore, decoupling itself. When no trigger has occurred, the HAMM is coupled, see Abstract of Li et al].

Claim 71, Li et al. in view of Oshikiri discloses the memory system of claim 69, further comprising a plurality of power supplies and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation [trigger even may be a power failure, Li et al. Abstract].

Claim 72 is rejected using the same rationale as that of Claim 38.

Claim 73 is rejected using the same rationale as that of Claim 39.

Claim 74 is rejected using the same rationale as that of Claim 40.

Claim 75 is rejected using the same rationale as that of Claim 41.

Claim 76 is rejected using the same rationale as that of Claim 42.

Claim 83 is rejected using the same rationale as that of Claim 61.

Claim 84 is rejected using the same rationale as that of Claim 62.

Claim 86 is rejected using the same rationale as that of Claim 64.

Claim 87 is rejected using the same rationale as that of Claim 65.

Claim 88 is rejected using the same rationale as that of Claim 66.

Claim 89 is rejected using the same rationale as that of Claim 62.

Claim 90 is rejected using the same rationale as that of Claim 68.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MIDYS ROJAS whose telephone number is (571)272-4207. The examiner can normally be reached on M-TH 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information

for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Midys Rojas/

Primary Examiner, Art Unit 2185

MR

1/3/2012

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Chen et al. CONFIRMATION NO.: 6240

SERIAL NO.: 12/240,916

FILING DATE: September 29, 2008

TITLE: NON-VOLATILE MEMORY MODULE

EXAMINER: ROJAS, Midys

ART UNIT: 2185

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND/OR REPLY TO OFFICE ACTION

Sir:

In response to the final Office Action mailed February 1, 2012, please amend the subject application as indicated.

Amendments to the Specification begin on page **2**.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page **4**.

Remarks begin on page **9**.

In the Specification

*Please amend paragraph **[0039]** as follows:*

[0039] Certain embodiments described herein utilize the non-volatile memory subsystem 40 as a flash "mirror" to provide backup of the volatile memory subsystem 30 in the event of certain system conditions. For example, the non-volatile memory subsystem 40 may backup the volatile memory subsystem 30 in the event of a trigger condition, such as, for example, a power failure or power reduction or a request from the host system. In one embodiment, the non-volatile memory subsystem ~~30~~ 40 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition. In certain embodiments, the trigger condition occurs when the memory system 10 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. In various embodiments, a backup and/or restore operation may occur in reboot and/or non-reboot trigger conditions.

*Please amend paragraph **[0047]** as follows:*

[0047] When operating in the first state, in certain embodiments, the step-up transformer 82 keeps the capacitor bank 86 charged at a peak value. In certain embodiments, the step-down transformer 84 acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 32 and 3.0V to the non-volatile flash memory elements 42) when operating in the second state (e.g., during power down). In certain embodiments, as schematically illustrated by Figures 1-3, the memory module 10 further comprises a switch 90 (e.g., FET switch) that

switches power provided to the controller 62, the volatile memory subsystem 30, and the non-volatile memory subsystem 40, between the power from the second power supply 80 and the power from the first power supply (e.g., system power) received via the interface 22. For example, the switch 90 may switch from the first power supply to the second power supply 80 when the voltage monitor 50 detects a low voltage condition. The switch 90 of certain embodiments advantageously ensures that the volatile memory elements 32 and non-volatile memory elements 42 are powered long enough for the data to be transferred from the volatile memory elements 32 and stored in the non-volatile memory elements 42. In certain embodiments, after the data transfer is complete, the switch 90 then switches back to the first power supply and the controller 62 transmits a signal to the at least one circuit ~~50~~ 52 to operatively decouple the controller 62 from the volatile memory subsystem 30, such that the memory system 10 re-enters the first state.

In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1-36. (Canceled)

37. (Currently amended) A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;

operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and

operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

38. (Currently amended) The method of Claim 37, wherein the third clock frequency is approximately equal to the second clock frequency.

39. (Original) The method of Claim 37, wherein the memory system is not powered by a battery when it is in the second mode of operation.

40. (Previously presented) The method of Claim 37, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.

41. (Original) The method of Claim 40, wherein the trigger condition comprises a power failure condition.

42. (Original) The method of Claim 37, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.

43-60. (Canceled)

61. (Previously presented) The method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation.

62. (Previously presented) The method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation.

63. (Currently amended) The method of claim 62, wherein the backup operation is conducted ~~on a regular basis~~at repeating time intervals.

64. (Previously presented) The method of claim 63, wherein the backup operation is initiated in response to a trigger event.

65. (Previously presented) The method of claim 37, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem.

66. (Previously presented) The method of claim 37, wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem.

67. (Currently amended) The method of claim 37, wherein one or more of the first, second or third clock frequencies is configurable by the memory system.

68. (Currently amended) The method of claim 37, wherein one or more of the first, second or third clock frequencies is configurable by a user.

69. (Currently amended) A memory system operatively coupled to a host system, the memory system comprising:

a volatile memory subsystem operable at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system; and

a non-volatile memory subsystem operable at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem,

the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency.

70. (Previously presented) The memory system of claim 69, further comprising:
a controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation.

71. (Previously presented) The memory system of claim 69, further comprising a plurality of power supplies and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation.

72. (Currently amended) The memory system of claim 69, wherein the third clock frequency is approximately equal to the second clock frequency.

73. (Previously presented) The memory system of claim 69, wherein the memory system is not powered by a battery when it is in the second mode of operation.

74. (Previously presented) The memory system of claim 69, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.

75. (Previously presented) The memory system of claim 74, wherein the trigger condition comprises a power failure condition.

76. (Previously presented) The memory system of claim 69, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.

77-82. (Canceled)

83. (Previously presented) The memory system of claim 69, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation.

84. (Previously presented) The memory system of claim 69, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation.

85. (Currently amended) The memory system of claim 84, wherein the backup operation is conducted ~~on a regular basis~~at repeating time intervals.

86. (Previously presented) The memory system of claim 85, wherein the backup operation is initiated in response to a trigger event.

87. (Previously presented) The memory system of claim 69, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem.

88. (Previously presented) The memory system of claim 69, wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem.

89. (Currently amended) The memory system of claim 69, wherein one or more of the first, second or third clock frequencies is configurable by the memory system.

90. (Currently amended) The memory system of claim 69, wherein one or more of the first, second or third clock frequencies is configurable by a user.

REMARKS

The final Office Action mailed February 1, 2012, has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Interview Record

Applicants gratefully acknowledge the courtesy and consideration extended to Applicants' undersigned representative, Khaled Shami, during the telephone interview with Examiner Mydis Rohas on March 1, 2012.

During the interview, Mr. Shami explained the distinction between the present invention and U.S. Pat. Pub. no. 2007/0192627 to Oshikiri (hereinafter, "Oshikiri"), and proposed modifying "frequency" with "clock," as reflected in the presently amended claims. Examiner Rohas agreed that such amendment would overcome the prior art rejections of the claims, and should therefore be submitted in the present after-final response.

Specification

The specification has been amended to correct minor typographical errors, changing the numerals "30" to "40" and "50" to "52" where appropriate. No new matter has been introduced.

Election/Restriction

Claims 55-60 and 77-82 were alleged to be drawn to different (non-elected) embodiments and are canceled without prejudice or disclaimer of their subject matter.

Rejection Under 35 U.S.C. § 112, Second Paragraph

Claims 63 and 65 have been amended to clarify that the backups may be performed at repeating time intervals. This language is used instead of "regular basis" even though the term "regular basis" is expressly used in paragraph [0039], line 8, and is in fact intended to mean repeating time intervals.

Rejection(s) Under 35 U.S.C. § 103(a)

Claims 37-42, 61-62, 64-76, 83-84, and 89-90 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. pat. no. 6,336,174 to Li *et al.* (hereinafter, "Li") in view of Oshikiri (hereinafter, "Oshikiri").

All of the independent claims—namely, claims 1 and 69—have been amended to modify "frequency" with "clock" and now expressly recite operation or operability "at a first *clock* frequency," "a second *clock* frequency," "a third *clock* frequency" (emphasis added), and so on. Such modification, it was agreed in the Examiner interview, overcomes the prior art rejection, and these claims and their dependency should now be passed to allowance.

Conclusion

In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 50-3557.

Respectfully submitted,
NIXON PEABODY LLP

Dated: March 2, 2012

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

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P.O. BOX 60610
PALO ALTO, CA 94306
TEL. (650) 320-7700
FAX. (650) 320-7701

Electronic Acknowledgement Receipt

EFS ID:	12216001
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-002
Receipt Date:	02-MAR-2012
Filing Date:	29-SEP-2008
Time Stamp:	17:11:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		062453_002_Resp_to_FOA.pdf	158906 ff811dc4dc919a96424b86e629968ac86b34ffd5	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment After Final	1	1
	Specification	2	2
	Claims	3	8
	Claims	9	11
Warnings:			
Information:			
	Total Files Size (in bytes):	158906	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/240,916	09/29/2008	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	310
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	310

APPLICATION AS AMENDED – PART II

AMENDMENT 03/02/2012

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 30	Minus	** 54	= 0	X $ =		OR	X $60=	0
Independent (37 CFR 1.16(h))	* 2	Minus	***7	= 0	X $ =		OR	X $250=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/TAMMY MCBETH BROWN/

UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/240,916	09/29/2008	Chi-She Chen	062453-002	6240

46188 7590 03/13/2012

Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER	
ROJAS, MIDYS	
ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
03/13/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentsv@nixonpeabody.com
ocastanon@nixonpeabody.com

Advisory Action **Before the Filing of an Appeal Brief**	**Application No.** *12/240,916*	**Applicant(s)** CHEN ET AL.
	Examiner MIDYS ROJAS	**Art Unit** 2185

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 02 March 2012 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: Applicants remarks are based on the claims as amended. The claim amendments are not being entered because they change the scope of the claims and raise new issues that require further search and consideration. Furthermore, the claim amendments do not place the claims in condition for allowance. The examiner is aware of Prior Art that teaches nonvolatile memory which operatates by changing the clock frequency being used to read and write data. .
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Midys Rojas/
Primary Examiner, Art Unit 2185

U.S. Patent and Trademark Office

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/240,916	09/29/2008	Chi-She Chen	062453-002	6240

46188 7590 03/13/2012

Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER	
ROJAS, MIDYS	
ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
03/13/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentsv@nixonpeabody.com
ocastanon@nixonpeabody.com

Applicant-Initiated Interview Summary	**Application No.** 12/240,916	**Applicant(s)** CHEN ET AL.	
	Examiner MIDYS ROJAS	**Art Unit** 2185	

All participants (applicant, applicant's representative, PTO personnel):

(1) *MIDYS ROJAS*. (3)_____.

(2) *Khaled Shami [38,745]*. (4)_____.

Date of Interview: *01 March 2012*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☒103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1 and 69*.

Identification of prior art discussed: *Li et al. [6,336,174] and Oshikiri [2007/0192627]*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applicant presented amendments to overcome the previously presented rejection. The examiner agreed that the amendments should overcome the previously presented rejection. Further search and considaration will be required..

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/Midys Rojas/ Primary Examiner, Art Unit 2185	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

———

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	12240916	Filing Date	2008-09-29	Docket Number (if applicable)	062453-002	Art Unit	2185
First Named Inventor	Chi-She Chen			Examiner Name	Midys Rojas		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☒ Other Response to Final Office Action filed March 2, 2012

☐ Enclosed

☐ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503557

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Signature of Registered U.S. Patent Practitioner			
Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2012-03-20
Name	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	12240916
Filing Date:	29-Sep-2008
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Filer:	Khaled Shami/Pamela Wilson
Attorney Docket Number:	062453-002
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	930	930
		Total in USD ($)		**930**

Electronic Acknowledgement Receipt	
EFS ID:	12351500
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-002
Receipt Date:	20-MAR-2012
Filing Date:	29-SEP-2008
Time Stamp:	18:34:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$930
RAM confirmation Number	5753
Deposit Account	503557
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	062453_002_RCE.pdf	114286 df181dfab020ad0f393025e018222e8e17c094ef	no	3
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30466 a288ac34c852c555b2ca41b8c460828dd3b06377	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	144752		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/240,916	09/29/2008	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 03/20/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 30	Minus	** 54	= 0	X $ =		OR	X $60=	0
Independent (37 CFR 1.16(h))	* 2	Minus	***7	= 0	X $ =		OR	X $250=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DEBRA R. WYATT/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/240,916	09/29/2008	Chi-She Chen	062453-002	6240

46188 7590 04/03/2012

Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER	
ROJAS, MIDYS	
ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
04/03/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentsv@nixonpeabody.com
ocastanon@nixonpeabody.com

Office Action Summary	Application No.	Applicant(s)
	12/240,916	CHEN ET AL.
	Examiner	Art Unit
	MIDYS ROJAS	2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2012*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-54,61-76 and 83-90* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-54,61-76 and 83-90* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)	
1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection, on 3/20/2012. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/02/2012 has been entered.

Response to Arguments

Applicant's arguments with respect to claims 37-42, 61-62, 64-76, 83-84, and 86-90 have been considered but are moot because the arguments do not apply to the references being used in the current rejection.

Claim Rejections - 35 USC § 112

The rejection of claims 63 and 85 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claiming the subject matter which applicant regards as the invention is being withdrawn in view of Applicant's amendment to these claims.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 38 and 72 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear how the third clock frequency can be **approximately** equal to the second clock frequency. It is not clear what makes these two values approximately equal or how two values can be approximately equal. Following mathematical logic, it is held that two values can only be equal or not equal. Clarification is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 37-42, 61-62, 64-76, 83-84, and 86-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. [US 6,336,174], Applicant cited art, in view of Cope [US 2008/0195806].

Claim 37, Li et al. discloses a method of controlling [via controller 206, Fig. 2] a memory system [hardware assisted memory module 104, of Fig. 1 and 2] operatively coupled to a host system [host system 100 including CPU 102, Fig. 1] and which includes a volatile memory subsystem [volatile memory 202, Fig. 2] and a non-volatile memory subsystem [nonvolatile memory 204, Fig. 2], the method comprising:

operating the volatile memory subsystem when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system [volatile memory 202 switches between modes of operation by switching isolation devices on/off in response to trigger events, see col. 6, lines 48-57; during normal operation, when the isolation devices are on, the HAMM behaves like a conventional memory module, see Abstract, and stores digital information received from the data bus of the host, see col. 3, lines 5-9 and col. 5, line 55 – col. 6, line 3, thus representing the first mode of operation claimed];

operating the non-volatile memory subsystem when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem [when a trigger event occurs, such as a system fault or a power failure, the HAMM isolates the volatile memory from the system memory bus by turning off isolation devices and isolating the HAMM from the host system. Then to store operation begins which includes copying data, address by address, from the volatile memory to the nonvolatile memory, see col. 9, lines 49-67].

Li et al. does not teach that in the first mode, the volatile memory operates at a first clock frequency while in the second mode, the non-volatile memory operates at a second clock frequency and the volatile memory operates at a third clock frequency that is less than the first clock frequency.

Cope discloses a memory [volatile memory device such a DRAM device, par. 0039] that is part of a memory system wherein after a pin grant transition 410, an adjust clock signal 412 transitions from a clock stable signal [which represents the claimed first

mode of operation] to a clock adjustment signal 414 [representing the second mode of operation] which is generated by the first memory controller to signal the volatile memory to discontinue operation at a normal clock frequency [first clock frequency] and to begin operation at a new clock frequency [second or third clock frequencies, see par. 0039]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Li et al. with the changing clock frequencies of Cope since providing for memory operations at different clock frequencies depending on the memory being executed enables the memory system to operate at optimal power consumption depending on the operation [see par. 0046 of Cope].

Claim 38, Li et al. in view of Cope discloses the method of Claim 37, wherein the third frequency is approximately equal to the second frequency [In Cope's first mode, all elements operate at the first clock frequency; the second mode represents a change of frequency clock for operation, therefore, the operations of the memories must be synchronized to this clock, par. 0039]

Claim 39, Li et al. in view of Cope discloses the method of Claim 37, wherein the memory system is not powered by a battery when it is in the second mode of operation [when the trigger condition that causes the switch of operation mode is a O/S hang-up, a backup battery is not required, see col. 7, lines 59-66 of Li et al.].

Claim 40, Li et al. in view of Cope discloses the method of Claim 37, wherein the memory system switches from the first mode of operation to the second mode of

operation in response to a trigger condition [detection of a trigger event, see Abstract of Li et al.].

Claim 41, Li et al. in view of Cope discloses the method of Claim 40, wherein the trigger condition comprises a power failure condition [trigger event may be power failure, see Abstract of Li et al.].

Claim 42, Li et al. in view of Cope discloses the method of Claim 37, wherein the memory system 104 further comprises a printed circuit board [as shown in Fig. 2 all elements are within one board] and the volatile memory subsystem 202 and the non-volatile memory subsystem 204 are located on the printed circuit board [see Fig. 2, and col. 2, line 58-col. 3, line 4].

Claim 61, Li et al. in view of Cope discloses the method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation [volatile memory 202 switches between modes of operation by switching isolation devices on/off in response to trigger events, see col. 6, lines 48-57; during normal operation, when the isolation devices are on, the HAMM behaves like a conventional memory module, see Abstract, and stores digital information received from the data bus of the host, see col. 3, lines 5-9 and col. 5, line 55 – col. 6, line 3, thus representing the first mode of operation claimed, Li et al.].

Claim 62, Li et al. in view of Cope discloses the method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation [when a trigger event occurs, such

as a system fault or a power failure, the HAMM isolates the volatile memory from the system memory bus by turning off isolation devices and isolating the HAMM from the host system. Then to store operation begins which includes copying data, address by address, from the volatile memory to the nonvolatile memory, see col. 9, lines 49-67, Li et al.].

Claim 64, Li et al. in view of Cope discloses the method of claim 63, wherein the backup operation is initiated in response to a trigger event [when a trigger event occurs, such as a system fault or a power failure, the HAMM isolates the volatile memory from the system memory bus by turning off isolation devices and isolating the HAMM from the host system. Then to store operation begins which includes copying data, address by address, from the volatile memory to the nonvolatile memory, see col. 9, lines 49-67, Li et al.].

Claim 65, Li et al. in view of Cope discloses the method of claim 37, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem [when a trigger event occurs, such as a system fault or a power failure, the HAMM isolates the volatile memory from the system memory bus by turning off isolation devices and isolating the HAMM from the host system. Then to store operation begins which includes copying data, address by address, from the volatile memory to the nonvolatile memory, see col. 9, lines 49-67, Li et al.].

Claim 66, Li et al. in view of Cope discloses the method of claim 37, wherein the second mode of operation comprises a restore operation in which data is communicated

from the non-volatile memory subsystem to the volatile memory subsystem [Restoring from the HAMM, see Abstract of Li et al.].

Claim 67, Li et al. in view of Cope discloses the method of claim 37, wherein one or more of the first, second or third frequencies is configurable by the memory system [clock adjustment signal 414 are generated by the memory controller; therefore, they are being configured by the information processing apparatus. In this case, the information processing apparatus is part of a memory system].

Claim 68, Li et al. in view of Cope discloses the method of claim 37, wherein one or more of the first, second or third frequencies is configurable by a user [clock adjustment signal 414 are generated by the memory controller; therefore, they are being configured by the information processing apparatus. In this case, the information processing apparatus is a user of an operation mode switching command generated by the CPU in order to perform this mode switch].

Claim 69 is rejected using the same rationale as that of Claim 37.

Claim 70, Li et al. in view of Cope discloses the memory system of claim 69, further comprising: a controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation [trigger event causes the HAMM to isolate is self, therefore, decoupling itself. When no trigger has occurred, the HAMM is coupled, see Abstract of Li et al].

Claim 71, Li et al. in view of Cope discloses the memory system of claim 69, further comprising a plurality of power supplies and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation [trigger even may be a power failure, Li et al. Abstract].

Claim 72 is rejected using the same rationale as that of Claim 38.

Claim 73 is rejected using the same rationale as that of Claim 39.

Claim 74 is rejected using the same rationale as that of Claim 40.

Claim 75 is rejected using the same rationale as that of Claim 41.

Claim 76 is rejected using the same rationale as that of Claim 42.

Claim 83 is rejected using the same rationale as that of Claim 61.

Claim 84 is rejected using the same rationale as that of Claim 62.

Claim 86 is rejected using the same rationale as that of Claim 64.

Claim 87 is rejected using the same rationale as that of Claim 65.

Claim 88 is rejected using the same rationale as that of Claim 66.

Claim 89 is rejected using the same rationale as that of Claim 62.

Claim 90 is rejected using the same rationale as that of Claim 68.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MIDYS ROJAS whose telephone number is (571)272-4207. The examiner can normally be reached on M-TH 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Midys Rojas/

Primary Examiner, Art Unit 2185

MR

3/25/2012

Notice of References Cited	Application/Control No. 12/240,916	Applicant(s)/Patent Under Reexamination CHEN ET AL.	
	Examiner MIDYS ROJAS	Art Unit 2185	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0195806	08-2008	Cope, Bryan	711/111
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	("("20020083368" | "20040190210" | "4420821" | "4449205" | "5519663" | "6158015" | "6336174" | "6336176" | "6487623" | "6658507" | "6799244" | "7409590").PN.").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/27 15:21
S2	12	("20020083368" | "20040190210" | "4420821" | "4449205" | "5519663" | "6158015" | "6336174" | "6336176" | "6487623" | "6658507" | "6799244" | "7409590").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:21
S3	0	host same (volatile with non-volatile with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:34
S4	1	(volatile with non-volatile with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:34
S5	87	(memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:35
S6	56	"711"/$.ccls. and (memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:35
S7	1013	memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:44
S8	128	"711"/$.ccls. and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:44
S9	46	("4072852" | "4815074" | "4959774" | "5283792" | "5379431" | "5799200").PN. OR ("6336174").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/27 15:44
S10	8	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) with (frequency or speed or clock)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:08
S11	2	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:09

S12	0	memory same (host near3 frequency) same (non-volatile near3 frequency) same mode	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:11
S13	1	(memory with mode) same (host with frequency) same (non-volatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:12
S14	6	(memory with mode) same (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:12
S15	13	"711"/$.ccls. and (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:14
S16	40	"711"/$.ccls. and (host with speed) same (nonvolatile with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:22
S17	16	"711"/$.ccls. and (host with speed) same (backup with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:23
S18	50	(backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:29
S19	48	power and (backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:29
S20	14	(power near3 (loss or fail$3)) and (backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:30
S21	8	(power near3 (loss or fail$3)) and (copy$3 or tranfer$3) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:38
S22	8	"711"/$.ccls. and (copy$3 or tranfer$3 or back-up or (back adj up)) with (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:41
S23	88	"711"/$.ccls. and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:44
S24	4347	((711/162) or (711/160) or (711/161) or (710/10)).CCLS.	USPAT; USOCR	OR	OFF	2011/07/28 19:20
S25	0	S24 and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/28 19:21
S26	1	S24 and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 19:21
S27	8	"711"/$.ccls. and ((non-volatile or nonvolatile) near3 memory) with ((vary$3 or alternat$3 or alter$3 or fluctuat$3 or chang$3) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/03/08 13:52
S28	1	"711"/$.ccls. and ((non-volatile or nonvolatile) near3 memory) with (dynamic near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2012/03/08 13:56

			JPO				

EAST Search History (Interference)

<This search history is empty>

3/26/2012 12:43:27 AM
C:\Users\mrojas\Documents\EAST\Workspaces\12240916.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12240916	CHEN ET AL.
	Examiner	Art Unit
	MIDYS ROJAS	2185

SEARCHED			
Class	Subclass	Date	Examiner
711	160, 161, 162	3/25/2012	MR
710	10	3/25/2012	MR

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Updated search: limited search of 711/160, 161, 162; 710/10; and text searches	3/25/2012	MR
PALM inventor name search	3/25/2012	MR

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

	/MIDYS ROJAS/ Primary Examiner.Art Unit 2185

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Chen et al. CONFIRMATION NO.: 6240

SERIAL NO.: 12/240,916

FILING DATE: September 29, 2008

TITLE: NON-VOLATILE MEMORY MODULE

EXAMINER: ROJAS, Midys

ART UNIT: 2185

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND/OR REPLY TO OFFICE ACTION

Sir:

In response to the Office Action mailed April 3, 2012, please amend the subject application as indicated.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page 2.

Remarks begin on page 7.

In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1-36. (Canceled)

37. (Previously presented) A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;

operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and

operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

38. (Currently amended) The method of Claim 37, wherein the third clock frequency is ~~approximately~~ substantially equal to the second clock frequency.

39. (Original) The method of Claim 37, wherein the memory system is not powered by a battery when it is in the second mode of operation.

40. (Previously presented) The method of Claim 37, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.

41. (Original) The method of Claim 40, wherein the trigger condition comprises a power failure condition.

42. (Original) The method of Claim 37, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.

43-60. (Canceled)

61. (Previously presented) The method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation.

62. (Previously presented) The method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation.

63. (Previously presented) The method of claim 62, wherein the backup operation is conducted at repeating time intervals.

64. (Previously presented) The method of claim 63, wherein the backup operation is initiated in response to a trigger event.

65. (Previously presented) The method of claim 37, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem.

66. (Previously presented) The method of claim 37, wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem.

67. (Previously presented) The method of claim 37, wherein one or more of the first, second or third clock frequencies is configurable by the memory system.

68. (Previously presented) The method of claim 37, wherein one or more of the first, second or third clock frequencies is configurable by a user.

69. (Previously presented) A memory system operatively coupled to a host system, the memory system comprising:

a volatile memory subsystem operable at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system; and

a non-volatile memory subsystem operable at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem,

the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency.

70. (Previously presented) The memory system of claim 69, further comprising:
a controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation.

71. (Previously presented) The memory system of claim 69, further comprising a plurality of power supplies and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation.

72. (Currently amended) The memory system of claim 69, wherein the third clock frequency is ~~approximately~~ substantially equal to the second clock frequency.

73. (Previously presented) The memory system of claim 69, wherein the memory system is not powered by a battery when it is in the second mode of operation.

74. (Previously presented) The memory system of claim 69, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.

75. (Previously presented) The memory system of claim 74, wherein the trigger condition comprises a power failure condition.

76. (Previously presented) The memory system of claim 69, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.

77-82. (Canceled)

83. (Previously presented) The memory system of claim 69, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation.

84. (Previously presented) The memory system of claim 69, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation.

85. (Previously presented) The memory system of claim 84, wherein the backup operation is conducted at repeating time intervals.

86. (Previously presented) The memory system of claim 85, wherein the backup operation is initiated in response to a trigger event.

87. (Previously presented) The memory system of claim 69, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem.

88. (Previously presented) The memory system of claim 69, wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem.

89. (Previously presented) The memory system of claim 69, wherein one or more of the first, second or third clock frequencies is configurable by the memory system.

90. (Previously presented) The memory system of claim 69, wherein one or more of the first, second or third clock frequencies is configurable by a user.

REMARKS

The Office Action mailed April 3, 2012, has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Rejection Under 35 U.S.C. § 112, Second Paragraph

Claims 63 and 85 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. The term "approximately" was objected to and has been replaced with the term "substantially." This term is used to account for the fact that while in theory two clock frequencies can be identical, in practice there will always be a difference, even if it is infinitesimal. This is a common approach in patent practice and has been deemed acceptable in the case law. See for instance Andrew Corp. v. Gabriel Electronics, 847 F.2d 819, 6 USPQ2d 2010 (Fed. Cir. 1988), discussed in MPEP 2173.05(b), ("The court held that the limitation 'which produces substantially equal E and H plane illumination patterns' was definite because one of ordinary skill in the art would know what was meant by 'substantially equal.'")

Rejection(s) Under 35 U.S.C. § 103(a)

Claims 37-42, 61-62, 64-76, 83-84, and 89-90 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. pat. no. 6,336,174 to *Li et al.* (hereinafter, "*Li*") in view of U.S. pat. pub. no. 2008/0195806 to *Cope* (hereinafter, "*Cope*").

The independent claims—namely, claims 37 and 69—recite:

- operation of the volatile memory subsystem at *a first clock frequency in a first mode* (in which data is communicated between the volatile memory subsystem and the host system),

- operation of the non-volatile memory subsystem at *a second clock frequency in a second mode* (in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem), and
- operation of the volatile memory subsystem at *a third clock frequency in the second mode* (the third clock frequency is less than the first clock frequency).

According to the above, the volatile memory subsystem operates at a lower clock frequency in the second mode (data communicated between volatile and non-volatile memory subsystems) than in the first mode (data communicated between volatile memory subsystem and host).

The Office action acknowledges that *Li* "does not teach that in the first mode, the volatile memory operates at a first clock frequency while in the second mode, the non-volatile memory operates at a second clock frequency and the volatile memory operates at a third clock frequency that is less than the first clock frequency." The Office action cites *Cope* to cure this defect, stating:

> *Cope* discloses a memory [volatile memory device such a DRAM device, par. 0039] that is part of a memory system wherein after a pin grant transition 410, an adjust clock signal 412 transitions from a clock stable signal [which represents the claimed first mode of operation] to a clock adjustment signal 414 [representing the second mode of operation] which is generated by the first memory controller to signal the volatile memory to discontinue operation at a normal clock frequency [first clock frequency] and to begin operation at a new clock frequency [second or third clock frequencies, see par. 0039]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Li et al. with the changing clock frequencies of *Cope* since providing for memory operations at different clock frequencies depending on the memory being executed enables the memory system to operate at optimal power consumption depending on the operation [see par. 0046 of *Cope*].

A close examination of *Cope* reveals that during memory operation, **the two memories are synchronized with one another**. Depending on which of the two memories has access to the shared contact 262, the memories operate together at either a first clock frequency or a second clock frequency. **Importantly, they never operate at different clock frequencies**.

This is evident from paragraph [0021], which states:

> In a particular embodiment, the external clock circuit can generate a common clock signal at a first clock frequency **for both** of the first memory controller 204 and the second memory controller 238 when the first memory controller 204 performs memory operations and can generate a common clock signal at a second clock frequency **for both** of the first memory controller 204 and the second memory controller 238 when the second memory controller 238 performs memory operations. In a specific embodiment, by adjusting the common clock signal frequency **for both** the first memory controller 204 and the second memory controller 238, lower power consumption can be achieved than by operating both memory controllers 204 and 238 at a constant clock frequency. In a specific embodiment, the second clock frequency can be predetermined to reduce number of cycles performed by the second memory controller 238 over a time period to reduce power consumption.
>
> (Emphasis added)

It is also evident from paragraph [0026], which describes what happens after the hand off of control of the shared contact 262 from the default second memory (volatile memory 258) to the first memory (non-volatile memory 230). Paragraph [0026] details synchronization of the clock-frequencies so that they are both the same after the hand-off occurs, and states:

> In addition, the logic 206 can send a clock adjust signal to the second memory controller 238 indicating that the external clock circuit has changed the clock frequency. The second memory controller 238 can **synchronize** to the new clock frequency and return a clock adjust complete signal to the logic 206 **when the synchronization is complete**.
>
> (Emphasis added)

In some instances, the shared frequency is lowered in order to reduce power consumption, but as in all cases, both memories are then run at the reduced frequency. This is evident from paragraph [0021], which further states:

> In a specific embodiment, by adjusting the common clock signal frequency for both the first memory controller 204 and the second memory controller 238, lower power consumption can be achieved than by operating both memory controllers 204 and 238 at a constant clock frequency. In a specific embodiment, the second clock frequency can be predetermined to reduce number of cycles performed by the second memory controller 238 over a time period to reduce power consumption.
>
> (Emphasis added)

The above clearly indicates that the frequencies of the *Li* memories are tied together such that the two memories both operate at a first frequency **or** a second frequency. Therefore *Cope* cannot be combined with *Li* to achieve the different clock frequencies of operation for two modes.

FIG. 4 of *Cope* is reproduced below, with labels added for time segments A – F for ease of discussion. The clock frequencies for the first (non-volatile) and second (volatile) memories during these time segments are clearly described in paragraphs [0037] – [0042] in *Cope*. These clock frequencies are listed below, with "transition" indicating an indeterminate clock frequency as clearly described by *Cope* in paragraph [0041]: "[T]he adjust clock signal transition 420 can be generated by the first memory controller to signal to the second memory controller that a clock signal has stabilized after transitioning to a different or new clock frequency."

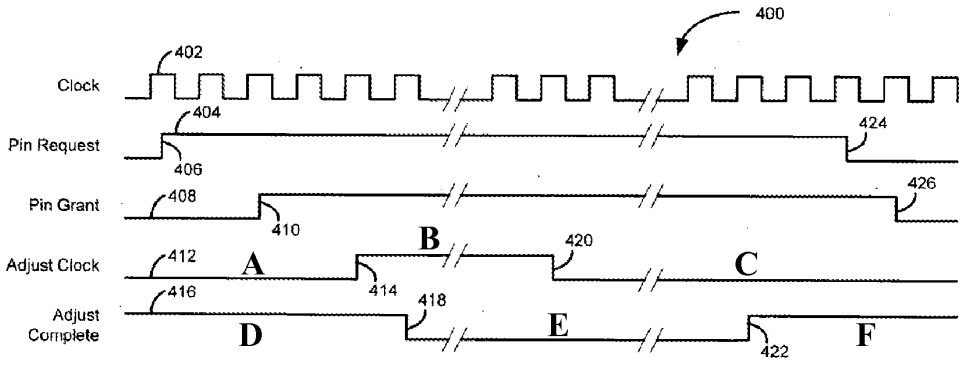

FIG. 4

Time Segment A: First memory (FLASH) at 1st frequency
Time Segment B: Transition
Time Segment C: First memory (FLASH) at 2nd frequency
Time Segment D: Second memory (DRAM) at 1st frequency
Time Segment E: Transition
Time Segment F: Second memory (DRAM) at 2nd frequency

Cope describes a 1st memory controller (FLASH controller) and a 2nd memory controller (DRAM controller) sharing a contact or data pin 262 (see [0012]-[0015] and that shared data pin (bus 106, 108, and 110 of Fig. 1 or bus 208, 210, and 212). *Cope* further describes that only ONE of the FLASH controller and DRAM controllers can use the shared data pin at a time, and that the DRAM controller is the default memory controller for controlling the shared contact (see paragraphs [0022], [0030], and [0045]).

In order for the FLASH controller to utilize the shared data bus in *Cope*, the FLASH controller must request the use of the shared data bus from the DRAM controller via a PIN REQUEST signal 404 at transition 406. The DRAM controller can release the shared data bus to the FLASH controller by asserting the PIN GRANT signal 408 at transition 410 (see [0037]-[0038]).

Cope describes changing the clock frequency for **both** the DRAM controller and FLASH controller (see [0021]). Once the DRAM controller releases the shared data bus to the FLASH controller, as indicated by the "pin grant transition 410" see [0038], the FLASH controller can assert the ADJUST CLOCK signal 412 at transition 414 to "to signal [the] DRAM device, to discontinue operation at a normal clock frequency and to begin operation at a different or new clock frequency" (see [0039]). It should be noted that, according to *Cope*:

a. when the ADJUST SIGNAL 412 is LOW (not asserted or logic 0, see Fig. 4, Time Segment A and Time Segment C) then it is indicative of a clock signal that is stable, regardless of what the frequency of the clock signal is.

b. when the ADJUST SIGNAL 412 is HIGH (asserted or logic 1, see Fig. 4, Time Segment B) then it is indicative of:

i. a clock signal that is NOT stable and with indeterminate frequency, see [0041] and as noted above,

ii. at transition 414, the DRAM device has already released the shared bus and therefore cannot possibly be operable to communicate data and note that *Cope* further describes additional steps that must be performed before

the DRAM device actually may starts operating using the new clock frequency, as clearly described in paragraph [0042] the ADJUST COMPLETE signal at "transition 422 is generated by the second memory controller to signal to the first memory controller that synchronization to the new clock frequency is complete", and

iii *Cope* further describes in paragraph [0040] that "In response to the adjust clock transition 414, an adjust complete signal 416 transitions to a low state at transition 418, indicating that synchronization to a clock signal is being performed." Or "…synchronization to a different or new clock frequency has not been completed."

c. It is very clear that *Cope* describes that:

i. during Time Segment A (see reproduced FIG. 4 above), the clock is stable at a first frequency,

ii. during Time Segment B, the clock is NOT stable, at an indeterminate frequency, and

iii. during Time Segment C, the clock is stable at a second frequency.

Therefore, it is not possible to have the ADJUST SIGNAL 412 while LOW to represent the claimed first mode of operation, because *Cope* uses the LOW level of ADJUST SIGNAL 412 to simply indicate that a "clock signal has stabilized after transitioning to a different or new clock frequency" **regardless of what that frequency is**. In fact, at ADJUST SIGNAL 412 LOW at Time Segment A, the clock is at a first frequency, while at ADJUST SIGNAL 412 LOW at Time Segment C, the clock is at a second frequency. In contrast, the claimed first mode of operation requires "operating the volatile memory subsystem at a first frequency." The DRAM device cannot be operating at two different frequencies, as alleged in the Office action, when the memory system is in a first mode.

Similarly, in the claimed second mode of operation, the "non-volatile memory subsystem operates at a second frequency" and "the volatile memory subsystem [operates] at a third frequency…" The Office action alleges that ADJUST CLOCK 412 transitioning at 414 to HIGH represents the claimed second mode of operation. It is very clear that *Cope* describes that:

a. during Time Segment B, when ADJUST CLOCK 412 transitions at 414 to HIGH, it is indicative of a clock that is NOT stable and thus the clock's frequency cannot be determined, see above, and

b. during Time Segment B, *Cope's* DRAM devices:

i. are inoperative to communicate data on the shared data bus since "after a pin grant transition 410" the DRAM controller has released the shared data bus to be used exclusively by the FLASH controller,

ii. cannot be operative since the clock frequency is unknown or indeterminate , and thus a catastrophic failure would occur if data access to the DRAM were to be gained somehow while the frequency "is not stable", and

iii. inoperable to communicate data since *Cope* clearly describes that the "adjust clock signal transition 414 can cause the volatile memory device to enter a self-refresh mode" and it is well known that if a DRAM device enters a self-refresh mode, which is akin to a power down mode, the DRAM uses an on-chip timer to generate internal refresh cycles as necessary, and the system clock may even be stopped during this time. Thus, no data read or write operation can be performed during DRAM self-refresh mode.

Cope cannot be used to describe two modes of operation, where a DRAM in a first mode operates at a first clock frequency and in a second mode operates at another frequency. This is because *Cope's* DRAM devices are operable only in a first Mode at a first frequency, and are inoperable to communicate data in a second mode where the clock is beginning to change or has changed to another frequency.

In *Cope*, after the FLASH controller asserts ADJUST SIGNAL 412 to a HIGH level, the DRAM controller asserts ADJUST COMPLETE signal 416 to LOW at transition 418 "to signal to the first (FLASH) memory controller that synchronization to a different or new clock frequency has not been completed" (see [0040]). Once the clock has stabilized, the FLASH controller returns ADJUST SIGNAL 412 to a LOW level, at 420, and after an unknown time period (indicated by the breaks in signals and clock in Fig. 4) the DRAM controller asserts ADJUST COMPLETE signal 416 to HIGH at

transition 422 "to signal to the FLASH memory controller that synchronization to the new clock frequency is complete" (see [0042]).

Further, as noted above, when the ADJUST CLOCK pin is asserted at 414 (to begin the alleged second mode of operation), the volatile memory is in fact being taken offline, as indicated by the pin grant transition 410, because *Cope* describes that only one of the first and second memories is allowed access to the shared data pin 262 at a time. In this mode, therefore, the DRAM is non-operational. At best, it is directed to enter a self-refresh mode, but it is effectively disconnected from the system. The combination of *Cope* with *Li* therefore would not teach or suggest operating the volatile memory at a first clock frequency in a first mode and at a lower clock frequency in a second mode, wherein in the first mode the volatile memory is communicating with the host, and in the second mode it is communicating with the non-volatile memory.

It should also be noted that the transition 414 and the asserted ADJUST CLOCK during Time Segment B thereafter do not demarcate a stable second clock frequency—the new clock frequency is not stable for possible usage by the DRAM until transition 422, when the ADJUST COMPLETE pin is returned to high by the DRAM at transition 422 and during Time Segment F thereafter.

Conclusion

In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 50-3557.

Respectfully submitted,
NIXON PEABODY LLP

Dated: May 24, 2012

/Khaled Shami/
Khaled Shami
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Electronic Acknowledgement Receipt

EFS ID:	12855993
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-002
Receipt Date:	24-MAY-2012
Filing Date:	29-SEP-2008
Time Stamp:	13:14:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		062453_002_Resp_to_OA.pdf	236279 298f4c5d348d21e5683e1f782bcb796e34f4e5df	yes	15

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	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	15
Warnings:			
Information:			
	Total Files Size (in bytes):	236279	

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/240,916	09/29/2008	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	**310**
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	**310**

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	05/24/2012	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 30	Minus	** 54	= 0	X $ =		OR	X $60=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***7	= 0	X $ =		OR	X $250=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**0**

		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/TER JACKSON WOODRUFF/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Chen et al. CONFIRMATION NO.: 6240

SERIAL NO.: 12/240,916

FILING DATE: September 29, 2008

TITLE: NON-VOLATILE MEMORY MODULE

EXAMINER: ROJAS, Midys

ART UNIT: 2185

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT AND/OR REPLY TO OFFICE ACTION

Sir:

In the Amendment and/or Reply to Office Action mailed May 24, 2012, two minor errors in the Remarks section were noted and are corrected hereby. On page 7, line 3 of the Amendment, "Claims 63 and 85," should read "Claims 38 and 72," and on page 10, lines 9-10, "*Li*" should be changed to "*Cope*," such that lines 9-10 of page 10 should read: "The above clearly indicates that the frequencies of the *Cope* memories are tied together such that the two memories both operate at a first frequency **or** a second frequency." In all other respects the following remarks and changes continue to apply.

In response to the Office Action mailed April 3, 2012, please amend the subject application as indicated.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page 2.

Remarks begin on page 7.

In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1-36. (Canceled)

37. (Previously presented) A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;

operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and

operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

38. (Currently amended) The method of Claim 37, wherein the third clock frequency is ~~approximately~~ substantially equal to the second clock frequency.

39. (Original) The method of Claim 37, wherein the memory system is not powered by a battery when it is in the second mode of operation.

40. (Previously presented) The method of Claim 37, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.

41. (Original) The method of Claim 40, wherein the trigger condition comprises a power failure condition.

42. (Original) The method of Claim 37, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.

43-60. (Canceled)

61. (Previously presented) The method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation.

62. (Previously presented) The method of claim 37, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation.

63. (Previously presented) The method of claim 62, wherein the backup operation is conducted at repeating time intervals.

64. (Previously presented) The method of claim 63, wherein the backup operation is initiated in response to a trigger event.

65. (Previously presented) The method of claim 37, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem.

66. (Previously presented) The method of claim 37, wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem.

67. (Previously presented) The method of claim 37, wherein one or more of the first, second or third clock frequencies is configurable by the memory system.

68. (Previously presented) The method of claim 37, wherein one or more of the first, second or third clock frequencies is configurable by a user.

69. (Previously presented) A memory system operatively coupled to a host system, the memory system comprising:

a volatile memory subsystem operable at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system; and

a non-volatile memory subsystem operable at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem,

the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency.

70. (Previously presented) The memory system of claim 69, further comprising:
a controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation.

71. (Previously presented) The memory system of claim 69, further comprising a plurality of power supplies and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation.

72. (Currently amended) The memory system of claim 69, wherein the third clock frequency is ~~approximately~~ substantially equal to the second clock frequency.

73. (Previously presented) The memory system of claim 69, wherein the memory system is not powered by a battery when it is in the second mode of operation.

74. (Previously presented) The memory system of claim 69, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.

75. (Previously presented) The memory system of claim 74, wherein the trigger condition comprises a power failure condition.

76. (Previously presented) The memory system of claim 69, wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.

77-82. (Canceled)

83. (Previously presented) The memory system of claim 69, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation.

84. (Previously presented) The memory system of claim 69, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation.

85. (Previously presented) The memory system of claim 84, wherein the backup operation is conducted at repeating time intervals.

86. (Previously presented) The memory system of claim 85, wherein the backup operation is initiated in response to a trigger event.

87. (Previously presented) The memory system of claim 69, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem.

88. (Previously presented) The memory system of claim 69, wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem.

89. (Previously presented) The memory system of claim 69, wherein one or more of the first, second or third clock frequencies is configurable by the memory system.

90. (Previously presented) The memory system of claim 69, wherein one or more of the first, second or third clock frequencies is configurable by a user.

REMARKS

The Office Action mailed April 3, 2012, has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Rejection Under 35 U.S.C. § 112, Second Paragraph

Claims ~~63~~ 38 and ~~85~~ 72 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. The term "approximately" was objected to and has been replaced with the term "substantially." This term is used to account for the fact that while in theory two clock frequencies can be identical, in practice there will always be a difference, even if it is infinitesimal. This is a common approach in patent practice and has been deemed acceptable in the case law. See for instance Andrew Corp. v. Gabriel Electronics, 847 F.2d 819, 6 USPQ2d 2010 (Fed. Cir. 1988), discussed in MPEP 2173.05(b), ("The court held that the limitation 'which produces substantially equal E and H plane illumination patterns' was definite because one of ordinary skill in the art would know what was meant by 'substantially equal.'")

Rejection(s) Under 35 U.S.C. § 103(a)

Claims 37-42, 61-62, 64-76, 83-84, and 89-90 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. pat. no. 6,336,174 to *Li et al*. (hereinafter, "*Li*") in view of U.S. pat. pub. no. 2008/0195806 to *Cope* (hereinafter, "*Cope*").

The independent claims—namely, claims 37 and 69—recite:

- operation of the volatile memory subsystem at *a first clock frequency in a first mode* (in which data is communicated between the volatile memory subsystem and the host system),
- operation of the non-volatile memory subsystem at *a second clock frequency in a second mode* (in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem), and
- operation of the volatile memory subsystem at *a third clock frequency in the second mode* (the third clock frequency is less than the first clock frequency).

According to the above, the volatile memory subsystem operates at a lower clock frequency in the second mode (data communicated between volatile and non-volatile memory subsystems) than in the first mode (data communicated between volatile memory subsystem and host).

The Office action acknowledges that *Li* "does not teach that in the first mode, the volatile memory operates at a first clock frequency while in the second mode, the non-volatile memory operates at a second clock frequency and the volatile memory operates at a third clock frequency that is less than the first clock frequency." The Office action cites *Cope* to cure this defect, stating:

> *Cope* discloses a memory [volatile memory device such a DRAM device, par. 0039] that is part of a memory system wherein after a pin grant transition 410, an adjust clock signal 412 transitions from a clock stable signal [which represents the claimed first mode of operation] to a clock adjustment signal 414 [representing the second mode of operation] which is generated by the first memory controller to signal the volatile memory to discontinue operation at a normal clock frequency [first clock frequency] and to begin operation at a new clock frequency [second or third clock frequencies, see par. 0039]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Li et al. with the changing clock frequencies of *Cope* since providing for memory operations at different clock frequencies depending on the memory being executed enables the memory system to operate at optimal power consumption depending on the operation [see par. 0046 of *Cope*].

A close examination of *Cope* reveals that during memory operation, **the two memories are synchronized with one another**. Depending on which of the two memories has access to the shared contact 262, the memories operate together at either a first clock frequency or a second clock frequency. **Importantly, they never operate at different clock frequencies**.

This is evident from paragraph [0021], which states:

> In a particular embodiment, the external clock circuit can generate a common clock signal at a first clock frequency **for both** of the first memory controller 204 and the second memory controller 238 when the first memory controller 204 performs memory operations and can generate a common clock signal at a second clock frequency **for both** of the first memory controller 204 and the second memory controller 238 when the second memory controller 238 performs memory operations. In a specific embodiment, by adjusting the common clock signal frequency **for both** the first memory controller 204 and the second memory controller 238, lower power consumption can be achieved than by operating both memory controllers 204 and 238 at a constant clock frequency. In a specific embodiment, the second clock frequency can be predetermined to reduce number of cycles performed by the second memory controller 238 over a time period to reduce power consumption.
>
> (Emphasis added)

It is also evident from paragraph [0026], which describes what happens after the hand off of control of the shared contact 262 from the default second memory (volatile memory 258) to the first memory (non-volatile memory 230). Paragraph [0026] details synchronization of the clock-frequencies so that they are both the same after the hand-off occurs, and states:

> In addition, the logic 206 can send a clock adjust signal to the second memory controller 238 indicating that the external clock circuit has changed the clock frequency. The second memory controller 238 can **synchronize** to the new clock frequency and return a clock adjust complete signal to the logic 206 **when the synchronization is complete**.

(Emphasis added)

In some instances, the shared frequency is lowered in order to reduce power consumption, but as in all cases, both memories are then run at the reduced frequency. This is evident from paragraph [0021], which further states:

> In a specific embodiment, by adjusting the common clock signal frequency for both the first memory controller 204 and the second memory controller 238, lower power consumption can be achieved than by operating both memory controllers 204 and 238 at a constant clock frequency. In a specific embodiment, the second clock frequency can be predetermined to reduce number of cycles performed by the second memory controller 238 over a time period to reduce power consumption.
>
> (Emphasis added)

The above clearly indicates that the frequencies of the ~~*Li*~~ *Cope* memories are tied together such that the two memories both operate at a first frequency **or** a second frequency. Therefore *Cope* cannot be combined with *Li* to achieve the different clock frequencies of operation for two modes.

FIG. 4 of *Cope* is reproduced below, with labels added for time segments A – F for ease of discussion. The clock frequencies for the first (non-volatile) and second (volatile) memories during these time segments are clearly described in paragraphs [0037] – [0042] in *Cope*. These clock frequencies are listed below, with "transition" indicating an indeterminate clock frequency as clearly described by *Cope* in paragraph [0041]: "[T]he adjust clock signal transition 420 can be generated by the first memory controller to signal to the second memory controller that a clock signal has stabilized after transitioning to a different or new clock frequency."

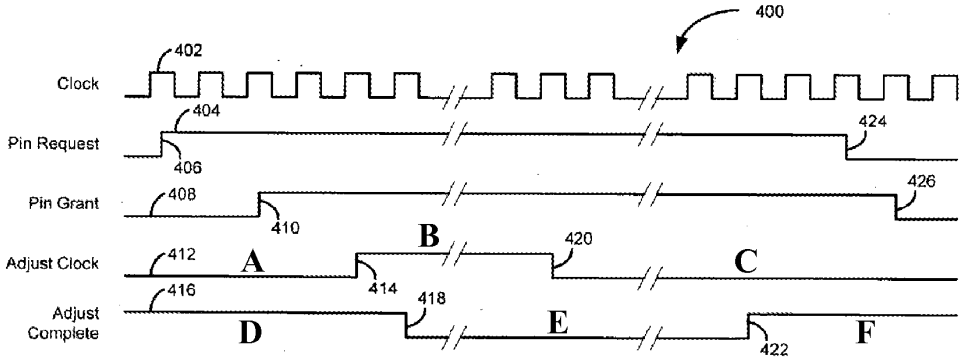

FIG. 4

Time Segment A: First memory (FLASH) at 1st frequency
Time Segment B: Transition
Time Segment C: First memory (FLASH) at 2nd frequency
Time Segment D: Second memory (DRAM) at 1st frequency
Time Segment E: Transition
Time Segment F: Second memory (DRAM) at 2nd frequency

Cope describes a 1st memory controller (FLASH controller) and a 2nd memory controller (DRAM controller) sharing a contact or data pin 262 (see [0012]-[0015] and that shared data pin (bus 106, 108, and 110 of Fig. 1 or bus 208, 210, and 212). *Cope* further describes that only ONE of the FLASH controller and DRAM controllers can use the shared data pin at a time, and that the DRAM controller is the default memory controller for controlling the shared contact (see paragraphs [0022], [0030], and [0045]).

In order for the FLASH controller to utilize the shared data bus in *Cope*, the FLASH controller must request the use of the shared data bus from the DRAM controller via a PIN REQUEST signal 404 at transition 406. The DRAM controller can release the shared data bus to the FLASH controller by asserting the PIN GRANT signal 408 at transition 410 (see [0037]-[0038]).

Cope describes changing the clock frequency for **both** the DRAM controller and FLASH controller (see [0021]). Once the DRAM controller releases the shared data bus to the FLASH controller, as indicated by the "pin grant transition 410" see [0038], the FLASH controller can

assert the ADJUST CLOCK signal 412 at transition 414 to "to signal [the] DRAM device, to discontinue operation at a normal clock frequency and to begin operation at a different or new clock frequency" (see [0039]). It should be noted that, according to *Cope*:

a. when the ADJUST SIGNAL 412 is LOW (not asserted or logic 0, see Fig. 4, Time Segment A and Time Segment C) then it is indicative of a clock signal that is stable, regardless of what the frequency of the clock signal is.

b. when the ADJUST SIGNAL 412 is HIGH (asserted or logic 1, see Fig. 4, Time Segment B) then it is indicative of:

i. a clock signal that is NOT stable and with indeterminate frequency, see [0041] and as noted above,

ii. at transition 414, the DRAM device has already released the shared bus and therefore cannot possibly be operable to communicate data and note that *Cope* further describes additional steps that must be performed before the DRAM device actually may starts operating using the new clock frequency, as clearly described in paragraph [0042] the ADJUST COMPLETE signal at "transition 422 is generated by the second memory controller to signal to the first memory controller that synchronization to the new clock frequency is complete", and

iii *Cope* further describes in paragraph [0040] that "In response to the adjust clock transition 414, an adjust complete signal 416 transitions to a low state at transition 418, indicating that synchronization to a clock signal is being performed." Or "…synchronization to a different or new clock frequency has not been completed."

c. It is very clear that *Cope* describes that:

i. during Time Segment A (see reproduced FIG. 4 above), the clock is stable at a first frequency,

ii. during Time Segment B, the clock is NOT stable, at an indeterminate frequency, and

iii. during Time Segment C, the clock is stable at a second frequency.

Therefore, it is not possible to have the ADJUST SIGNAL 412 while LOW to represent the claimed first mode of operation, because *Cope* uses the LOW level of ADJUST SIGNAL 412 to simply indicate that a "clock signal has stabilized after transitioning to a different or new clock frequency" **regardless of what that frequency is**. In fact, at ADJUST SIGNAL 412 LOW at Time Segment A, the clock is at a first frequency, while at ADJUST SIGNAL 412 LOW at Time Segment C, the clock is at a second frequency. In contrast, the claimed first mode of operation requires "operating the volatile memory subsystem at a first frequency." The DRAM device cannot be operating at two different frequencies, as alleged in the Office action, when the memory system is in a first mode.

Similarly, in the claimed second mode of operation, the "non-volatile memory subsystem operates at a second frequency" and "the volatile memory subsystem [operates] at a third frequency…" The Office action alleges that ADJUST CLOCK 412 transitioning at 414 to HIGH represents the claimed second mode of operation. It is very clear that *Cope* describes that:

a. during Time Segment B, when ADJUST CLOCK 412 transitions at 414 to HIGH, it is indicative of a clock that is NOT stable and thus the clock's frequency cannot be determined, see above, and

b. during Time Segment B, *Cope's* DRAM devices:

i. are inoperative to communicate data on the shared data bus since "after a pin grant transition 410" the DRAM controller has released the shared data bus to be used exclusively by the FLASH controller,

ii. cannot be operative since the clock frequency is unknown or indeterminate, and thus a catastrophic failure would occur if data access to the DRAM were to be gained somehow while the frequency "is not stable", and

iii. inoperable to communicate data since *Cope* clearly describes that the "adjust clock signal transition 414 can cause the volatile memory device to enter a self-refresh mode" and it is well known

> that if a DRAM device enters a self-refresh mode, which is akin to a power down mode, the DRAM uses an on-chip timer to generate internal refresh cycles as necessary, and the system clock may even be stopped during this time. Thus, no data read or write operation can be performed during DRAM self-refresh mode.

Cope cannot be used to describe two modes of operation, where a DRAM in a first mode operates at a first clock frequency and in a second mode operates at another frequency. This is because *Cope's* DRAM devices are operable only in a first Mode at a first frequency, and are inoperable to communicate data in a second mode where the clock is beginning to change or has changed to another frequency.

In *Cope*, after the FLASH controller asserts ADJUST SIGNAL 412 to a HIGH level, the DRAM controller asserts ADJUST COMPLETE signal 416 to LOW at transition 418 "to signal to the first (FLASH) memory controller that synchronization to a different or new clock frequency has not been completed" (see [0040]). Once the clock has stabilized, the FLASH controller returns ADJUST SIGNAL 412 to a LOW level, at 420, and after an unknown time period (indicated by the breaks in signals and clock in Fig. 4) the DRAM controller asserts ADJUST COMPLETE signal 416 to HIGH at transition 422 "to signal to the FLASH memory controller that synchronization to the new clock frequency is complete" (see [0042]).

Further, as noted above, when the ADJUST CLOCK pin is asserted at 414 (to begin the alleged second mode of operation), the volatile memory is in fact being taken offline, as indicated by the pin grant transition 410, because *Cope* describes that only one of the first and second memories is allowed access to the shared data pin 262 at a time. In this mode, therefore, the DRAM is non-operational. At best, it is directed to enter a self-refresh mode, but it is effectively disconnected from the system. The combination of *Cope* with *Li* therefore would not teach or suggest operating the volatile memory at a first clock frequency in a first mode and at a lower clock frequency in a second mode, wherein in the first mode the volatile memory is communicating with the host, and in the second mode it is communicating with the non-volatile memory.

It should also be noted that the transition 414 and the asserted ADJUST CLOCK during Time Segment B thereafter do not demarcate a stable second clock frequency—the new clock frequency is not stable for possible usage by the DRAM until transition 422, when the ADJUST COMPLETE pin is returned to high by the DRAM at transition 422 and during Time Segment F thereafter.

Conclusion

In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 50-3557.

Respectfully submitted,
NIXON PEABODY LLP

Dated: June 14, 2012

/Khaled Shami/
Khaled Shami
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Electronic Acknowledgement Receipt

EFS ID:	13013716
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-002
Receipt Date:	14-JUN-2012
Filing Date:	29-SEP-2008
Time Stamp:	13:32:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		062453_002_Supplemental_Amdt.pdf	237985 780a911a5630338b6ac2b958e08c8298341606af	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Supplemental Response or Supplemental Amendment	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	16
Warnings:			
Information:			
	Total Files Size (in bytes):	237985	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/240,916	09/29/2008	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	54 minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	7 minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 06/14/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 30	Minus	** 54	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	* 2	Minus	***7	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/JESSICA GAYNOR/

PTO/SB/36 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE

RESCISSION OF PREVIOUS NONPUBLICATION REQUEST
(35 U.S.C. 122(b)(2)(B)(ii))
AND, IF APPLICABLE,
NOTICE OF FOREIGN FILING
(35 U.S.C. 122(b)(2)(B)(iii))

Send completed form to:
Mail Stop PG Pub
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX: (571) 273-8300

Application Number	12240916
Filing Date	2008-09-29
First Named Inventor	Chi-She CHEN
Title	Non-Volatile Memory Module
Atty Docket Number	062453-002
Art Unit	2185
Examiner	Midys ROJAS

A request that the above-identified application not be published under 35 U.S.C. 122(b) (nonpublication request) was included with the above-identified application on filing pursuant to 35 U.S.C. 122(b)(2)(B)(i).
I hereby **rescind** the previous nonpublication request.

If a notice of foreign or international filing is or will be required by 35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c), I hereby provide such notice. This notice is being provided no later than forty-five (**45**) days after the date of such foreign or international filing.

*If a notice of subsequent foreign or international filing required by 35 U.S.C. 122(b)(2)(B)(iii) and 37 CFR 1.213(c) was not filed within forty-five (**45**) days after the date of filing of the foreign or international application, the application is ABANDONED, and a petition to revive under 37 CFR 1.137(b) is required. See 37 CFR 1.137(f).*

/Khaled Shami/ — Signature

August 22, 2012 — Date

Khaled Shami — Typed or printed name

38745 — Registration Number, if applicable

650-320-7700 — Telephone Number

This request must be signed in compliance with 37 CFR 1.33(b).

If information or assistance is needed in completing this form, please contact the Pre-Grant Publication Division at (703)605-4283 or by e-mail at PGPub@USPTO.gov.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop PG Pub, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature

Name (Print/Type) | Date

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	13558325
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-002
Receipt Date:	22-AUG-2012
Filing Date:	29-SEP-2008
Time Stamp:	12:29:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Rescind Nonpublication Request for Pre Grant Pub	062453_002_Recission.pdf	259216 3eba2863f7701ba99a9092d6fffe5637163cc7e0	no	2

Warnings:	
Information:	

Total Files Size (in bytes):	259216

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/240,916	09/29/2008	Chi-She Chen	062453-002

CONFIRMATION NO. 6240

46188
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

NEW OR REVISED PPD NOTICE

OC000000056273308

NOTICE OF NEW OR REVISED PROJECTED PUBLICATION DATE

The above-identified application has a new or revised projected publication date. The current projected publication date for this application is 12/06/2012. If this is a new projected publication date (there was no previous projected publication date), the application has been cleared by Licensing & Review or a secrecy order has been rescinded and the application is now in the publication queue.

If this is a revised projected publication date (one that is different from a previously communicated projected publication date), the publication date has been revised due to processing delays in the USPTO or the abandonment and subsequent revival of an application. The application is anticipated to be published on a date that is more than six weeks different from the originally-projected publication date.

More detailed publication information is available through the private side of Patent Application Information Retrieval (PAIR) System. The direct link to access PAIR is currently http://pair.uspto.gov. Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Questions relating to this Notice should be directed to the Office of Data Management, Application Assistance Unit at (571) 272-4000, or (571) 272-4200, or 1-888-786-0101.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/240,916	09/29/2008	Chi-She Chen	062453-002

CONFIRMATION NO. 6240

46188
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

NONPUBLICATION RESCISSION LETTER

OC000000056230596

Date Mailed: 08/31/2012

Communication Regarding Rescission Of Nonpublication Request and/or Notice of Foreign Filing

Applicant's rescission of the previously-filed nonpublication request and/or notice of foreign filing is acknowledged. The paper has been reflected in the Patent and Trademark Office's (USPTO's) computer records so that the earliest possible projected publication date can be assigned.

The projected publication date is 12/06/2012.

If applicant rescinded the nonpublication request before or on the date of "foreign filing,"[1] then no notice of foreign filing is required.

If applicant foreign filed the application after filing the above application and before filing the rescission, and the rescission did not also include a notice of foreign filing, then a notice of foreign filing (not merely a rescission) is required to be filed within 45 days of the date of foreign filing. See 35 U.S.C. § 122(b)(2)(B)(iii), and Clarification of the United States Patent and Trademark Office's Interpretation of the Provisions of 35 U.S.C. § 122(b)(2)(B)(ii)-(iv), 1272 Off. Gaz. Pat. Office 22 (July 1, 2003).

If a notice of foreign filing is required and is not filed within 45 days of the date of foreign filing, then the application becomes abandoned pursuant to 35 U.S.C. § 122(b)(2)(B)(iii). In this situation, applicant should either file a petition to revive or notify the Office that the application is abandoned. See 37 CFR 1.137(f). Any such petition to revive will be forwarded to the Office of Petitions for a decision. Note that the filing of the petition will not operate to stay any period of reply that may be running against the application.

Questions regarding petitions to revive should be directed to the Office of Petitions at (571) 272-3282.

[1] Note, for purpose of this notice, that "foreign filing" means "filing an application directed to the same invention in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing".

/hsarwari/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

46188 7590 09/17/2012

Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER
ROJAS, MIDYS

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 09/17/2012

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/240,916	09/29/2008	Chi-She Chen	062453-002	6240

TITLE OF INVENTION: NON-VOLATILE MEMORY MODULE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	12/17/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

46188 7590 09/17/2012

Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/240,916	09/29/2008	Chi-She Chen	062453-002	6240

TITLE OF INVENTION: NON-VOLATILE MEMORY MODULE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	12/17/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
ROJAS, MIDYS	2185	711-104000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/240,916	09/29/2008	Chi-She Chen	062453-002	6240

46188 7590 09/17/2012

Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER	
ROJAS, MIDYS	
ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 09/17/2012

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 466 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 466 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/240,916	CHEN ET AL.	
	Examiner	Art Unit	
	MIDYS ROJAS	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *6/14/2012*.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *37-42,61-76 and 83-90*.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Midys Rojas/
Primary Examiner, Art Unit 2185

REASONS FOR ALLOWANCE

Claims 37-42, 61-76, and 83-90 are allowed.

The following is an examiner's statement of reasons for allowance:

The Prior Art of Record fails to teach and/or suggest in the claimed combination controlling a memory system coupled to a host, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising: operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system; operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MIDYS ROJAS whose telephone number is (571)272-4207. The examiner can normally be reached on M-TH 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Midys Rojas/
Primary Examiner, Art Unit 2185

9/10/2012

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	("("20020083368" | "20040190210" | "4420821" | "4449205" | "5519663" | "6158015" | "6336174" | "6336176" | "6487623" | "6658507" | "6799244" | "7409590").PN.").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L2	12	("20020083368" | "20040190210" | "4420821" | "4449205" | "5519663" | "6158015" | "6336174" | "6336176" | "6487623" | "6658507" | "6799244" | "7409590").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L3	0	host same (volatile with non-volatile with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L4	1	(volatile with non-volatile with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L5	92	(memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L6	60	"711"/$.ccls. and (memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L7	1121	memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L8	151	"711"/$.ccls. and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L9	74	("4072852" | "4815074" | "4959774" | "5283792" | "5379431" | "5799200").PN. OR ("6336174").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L10	10	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) with (frequency or speed or clock)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L11	2	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28

L12	0	memory same (host near3 frequency) same (non-volatile near3 frequency) same mode	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L13	2	(memory with mode) same (host with frequency) same (non-volatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L14	6	(memory with mode) same (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L15	20	"711"/$.ccls. and (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L16	49	"711"/$.ccls. and (host with speed) same (nonvolatile with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L17	29	"711"/$.ccls. and (host with speed) same (backup with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L18	50	(backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L19	48	power and (backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L20	14	(power near3 (loss or fail$3)) and (backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L21	8	(power near3 (loss or fail$3)) and (copy$3 or tranfer$3) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L22	8	"711"/$.ccls. and (copy$3 or tranfer$3 or back-up or (back adj up)) with (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L23	94	"711"/$.ccls. and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L24	5081	((711/162) or (711/160) or (711/161) or (710/10)).CCLS.	USPAT; USOCR	OR	OFF	2012/09/10 13:28
L25	2	L24 and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L26	1	L24 and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L27	9	"711"/$.ccls. and ((non-volatile or nonvolatile) near3 memory) with ((vary$3 or alternat$3 or alter$3 or fluctuat$3 or chang$3) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L28	2	"711"/$.ccls. and ((non-volatile or nonvolatile) near3 memory) with (dynamic near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2012/09/10 13:28

			JPO			
L40	5839	((711/162) or (711/160) or (711/161) or (710/10) or (711/104)).CCLS.	USPAT; USOCR	OR	OFF	2012/09/10 13:40
L41	3	L40 and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:40
L42	5	L40 and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:41
L43	1	L40 and (host with speed) same (nonvolatile with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:41
L44	0	L40 and ((non-volatile or nonvolatile) near3 memory) with (dynamic near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:41
L45	2	L40 and (memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:41
L46	2	L40 and (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:42
L47	8	L40 and (host with speed) same (backup with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:42
L48	3	L40 and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:42

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L29	8101	((711/162) or (711/160) or (711/161) or (710/10)).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:28
L30	2	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:35
L31	524	(memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:36
L32	6	(memory with mode) same (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:36
L33	1029	memory with mode near3 frequency	US-PGPUB;	OR	OFF	2012/09/10 13:37

			USPAT; UPAD			
L34	0	L29 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:37
L35	2	L29 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency) (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:37
L36	524	L29 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency) (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:37
L37	2	L29 and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:39
L38	0	L29 and (memory with mode) same (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:39
L39	3	L29 and memory with mode near3 frequency	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:39
L49	9362	((711/162) or (711/160) or (711/161) or (710/10) or (711/104)).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:42
L50	0	L49 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:42
L51	2	L49 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency) (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:43
L52	524	L49 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency) (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:43
L53	7	L49 and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:43
L54	0	L49 and (memory with mode) same (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:43
L55	8	L49 and memory with mode near3 frequency	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:43
L56	0	netlist.as. with (memory same frequency)	US-PGPUB; USPAT;	OR	OFF	2012/09/10 14:10

			UPAD			
L57	42	netlist.as.	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 14:10
L58	134096	netlist.as. (frequency with mode)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 14:11
L59	1	netlist.as. and (frequency with mode)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 14:11

9/ 10/ 2012 2:12:25 PM
C:\ Users\ mrojas\ Documents\ EAST\ Workspaces\ 12240916.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12240916	CHEN ET AL.
	Examiner	Art Unit
	MIDYS ROJAS	2185

SEARCHED			
Class	Subclass	Date	Examiner
711	104, 160, 161, 162	9/10/2012	MR
710	10	9/10/2012	MR

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Updated search: limited search of 711/160, 161, 162; 710/10; and text searches	3/25/2012	MR
PALM inventor name search	3/25/2012	MR
EAST Updated search: limited search of 711/104, 160, 161, 162; 710/10; and text search	9/10/2012	MR
PALM Inventor Name search	9/10/2012	MR
EAST Interference search	9/10/2012	MR
EAST Assignee search	9/10/2012	MR

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
711	104, 160, 161, 162		
710	10		

	/MIDYS ROJAS/ Primary Examiner.Art Unit 2185

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Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 6240

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/240,916	09/29/2008	711	2185	062453-002

APPLICANTS

Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************

This application is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

10/08/2008

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /MIDYS ROJAS/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	12	54	7

ADDRESS

Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306
UNITED STATES

TITLE

NON-VOLATILE MEMORY MODULE

FILING FEE RECEIVED		
3570	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	("("20020083368" | "20040190210" | "4420821" | "4449205" | "5519663" | "6158015" | "6336174" | "6336176" | "6487623" | "6658507" | "6799244" | "7409590").PN.").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L2	12	("20020083368" | "20040190210" | "4420821" | "4449205" | "5519663" | "6158015" | "6336174" | "6336176" | "6487623" | "6658507" | "6799244" | "7409590").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L3	0	host same (volatile with non-volatile with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L4	1	(volatile with non-volatile with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L5	92	(memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L6	60	"711"/$.ccls. and (memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L7	1121	memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L8	151	"711"/$.ccls. and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L9	74	("4072852" | "4815074" | "4959774" | "5283792" | "5379431" | "5799200").PN. OR ("6336174").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L10	10	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) with (frequency or speed or clock)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L11	2	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28

L12	0	memory same (host near3 frequency) same (non-volatile near3 frequency) same mode	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L13	2	(memory with mode) same (host with frequency) same (non-volatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L14	6	(memory with mode) same (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L15	20	"711"/$.ccls. and (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L16	49	"711"/$.ccls. and (host with speed) same (nonvolatile with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L17	29	"711"/$.ccls. and (host with speed) same (backup with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L18	50	(backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L19	48	power and (backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L20	14	(power near3 (loss or fail$3)) and (backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L21	8	(power near3 (loss or fail$3)) and (copy$3 or tranfer$3) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L22	8	"711"/$.ccls. and (copy$3 or tranfer$3 or back-up or (back adj up)) with (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L23	94	"711"/$.ccls. and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L24	5081	((711/162) or (711/160) or (711/161) or (710/10)).CCLS.	USPAT; USOCR	OR	OFF	2012/09/10 13:28
L25	2	L24 and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L26	1	L24 and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:28
L27	9	"711"/$.ccls. and ((non-volatile or nonvolatile) near3 memory) with ((vary$3 or alternat$3 or alter$3 or fluctuat$3 or chang$3) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:28
L28	2	"711"/$.ccls. and ((non-volatile or nonvolatile) near3 memory) with (dynamic near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2012/09/10 13:28

			JPO			
L40	5839	((711/162) or (711/160) or (711/161) or (710/10) or (711/104)).CCLS.	USPAT; USOCR	OR	OFF	2012/09/10 13:40
L41	3	L40 and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:40
L42	5	L40 and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:41
L43	1	L40 and (host with speed) same (nonvolatile with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:41
L44	0	L40 and ((non-volatile or nonvolatile) near3 memory) with (dynamic near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:41
L45	2	L40 and (memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:41
L46	2	L40 and (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:42
L47	8	L40 and (host with speed) same (backup with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2012/09/10 13:42
L48	3	L40 and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/09/10 13:42
S1	0	("("20020083368" | "20040190210" | "4420821" | "4449205" | "5519663" | "6158015" | "6336174" | "6336176" | "6487623" | "6658507" | "6799244" | "7409590").PN.").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/27 15:21
S2	12	("20020083368" | "20040190210" | "4420821" | "4449205" | "5519663" | "6158015" | "6336174" | "6336176" | "6487623" | "6658507" | "6799244" | "7409590").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:21
S3	0	host same (volatile with non-volatile with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:34
S4	1	(volatile with non-volatile with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:34
S5	87	(memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2011/07/27 15:35

			JPO			
S6	56	"711"/$.ccls. and (memory with (back-up or copy) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:35
S7	1013	memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:44
S8	128	"711"/$.ccls. and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/27 15:44
S9	46	("4072852" | "4815074" | "4959774" | "5283792" | "5379431" | "5799200").PN. OR ("6336174").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/27 15:44
S10	8	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) with (frequency or speed or clock)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:08
S11	2	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:09
S12	0	memory same (host near3 frequency) same (non-volatile near3 frequency) same mode	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:11
S13	1	(memory with mode) same (host with frequency) same (non-volatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:12
S14	6	(memory with mode) same (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:12
S15	13	"711"/$.ccls. and (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:14
S16	40	"711"/$.ccls. and (host with speed) same (nonvolatile with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:22
S17	16	"711"/$.ccls. and (host with speed) same (backup with speed)	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:23
S18	50	(backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:29
S19	48	power and (backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:29
S20	14	(power near3 (loss or fail$3)) and (backup or back-up) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:30
S21	8	(power near3 (loss or fail$3)) and (copy$3 or tranfer$3) same (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:38
S22	8	"711"/$.ccls. and (copy$3 or tranfer$3 or	US-PGPUB;	OR	OFF	2011/07/28

		back-up or (back adj up)) with (high$3 near3 (speed or frequency) near3 (non-volatile or nonvolatile))	USPAT; USOCR			16:41
S23	88	"711"/$.ccls. and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 16:44
S24	4347	((711/162) or (711/160) or (711/161) or (710/10)).CCLS.	USPAT; USOCR	OR	OFF	2011/07/28 19:20
S25	0	S24 and memory with mode near3 frequency	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2011/07/28 19:21
S26	1	S24 and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; USOCR	OR	OFF	2011/07/28 19:21
S27	8	"711"/$.ccls. and ((non-volatile or nonvolatile) near3 memory) with ((vary$3 or alternat$3 or alter$3 or fluctuat$3 or chang$3) near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/03/08 13:52
S28	1	"711"/$.ccls. and ((non-volatile or nonvolatile) near3 memory) with (dynamic near3 frequency)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2012/03/08 13:56

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L29	8101	((711/162) or (711/160) or (711/161) or (710/10)).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:28
L30	2	(power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:35
L31	524	(memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:36
L32	6	(memory with mode) same (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:36
L33	1029	memory with mode near3 frequency	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:37
L34	0	L29 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:37
L35	2	L29 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency) (power near3 (loss or fail$3)) with (memory near3 (back-up or back	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:37

		adj up)) same (frequency)				
L36	524	L29 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency) (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:37
L37	2	L29 and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:39
L38	0	L29 and (memory with mode) same (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:39
L39	3	L29 and memory with mode near3 frequency	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:39
L49	9362	((711/162) or (711/160) or (711/161) or (710/10) or (711/104)).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:42
L50	0	L49 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:42
L51	2	L49 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency) (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:43
L52	524	L49 and (power near3 (loss or fail$3)) with (memory near3 (back-up or back adj up)) same (frequency) (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:43
L53	7	L49 and (memory near3 mode) with (operat$3 near3 (speed or frequency))	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:43
L54	0	L49 and (memory with mode) same (host with frequency) same (nonvolatile with frequency)	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:43
L55	8	L49 and memory with mode near3 frequency	US-PGPUB; USPAT; UPAD	OR	OFF	2012/09/10 13:43

9/ 10/ 2012 1:44:13 PM
C:\ Users\ mrojas\ Documents\ EAST\ Workspaces\ 12240916.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12240916	CHEN ET AL.
	Examiner	Art Unit
	MIDYS ROJAS	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/28/2011	09/10/2012							
	1	N	-							
	2	N	-							
	3	N	-							
	4	N	-							
	5	N	-							
	6	N	-							
	7	N	-							
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	31	N	-							
	32	N	-							
	33	N	-							
	34	N	-							
	35	N	-							
	36	N	-							

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12240916	CHEN ET AL.
	Examiner	Art Unit
	MIDYS ROJAS	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/28/2011	09/10/2012							
	37	✓	=							
	38	✓	=							
	39	✓	=							
	40	✓	=							
	41	✓	=							
	42	✓	=							
	43	N	-							
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	68		=							
	69		=							
	70		=							
	71		=							
	72		=							

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12240916	CHEN ET AL.
	Examiner	Art Unit
	MIDYS ROJAS	2185

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/28/2011	09/10/2012							
	73		=							
	74		=							
	75		=							
	76		=							
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	78		-							
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	84		=							
	85		=							
	86		=							
	87		=							
	88		=							
	89		=							
	90		=							

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12240916	CHEN ET AL.
	Examiner	Art Unit
	MIDYS ROJAS	2185

ORIGINAL		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
711	104	G	0	6	F	12 / 00 (2006.01.01)						

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
711	160	161	162		
710	10				

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17		33		49	11	65		81				
	2		18		34		50	12	66		82				
	3		19		35		51	13	67	23	83				
	4		20		36		52	14	68	24	84				
	5		21	1	37		53	15	69	25	85				
	6		22	2	38		54	16	70	26	86				
	7		23	3	39		55	17	71	27	87				
	8		24	4	40		56	18	72	28	88				
	9		25	5	41		57	19	73	29	89				
	10		26	6	42		58	20	74	30	90				
	11		27		43		59	21	75						
	12		28		44		60	22	76						
	13		29		45	7	61		77						
	14		30		46	8	62		78						
	15		31		47	9	63		79						
	16		32		48	10	64		80						

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/MIDYS ROJAS/ Primary Examiner.Art Unit 2185	09/10/2012	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	37	9

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

46188 7590 09/17/2012
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/240,916	09/29/2008	Chi-She Chen	062453-002	6240

TITLE OF INVENTION: NON-VOLATILE MEMORY MODULE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	12/17/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
ROJAS, MIDYS	2185	711-104000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 NIXON PEABODY LLP
2 Khaled Shami
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: NETLIST, INC.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): IRVINE, CALIFORNIA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 503557 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 9/26/2012

Typed or printed name Khaled Shami Registration No. 38745

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal

Application Number:	12240916
Filing Date:	29-Sep-2008
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Filer:	Khaled Shami/Pamela Wilson
Attorney Docket Number:	062453-002

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2040**

Electronic Acknowledgement Receipt

EFS ID:	13846688
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-002
Receipt Date:	26-SEP-2012
Filing Date:	29-SEP-2008
Time Stamp:	17:42:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2040
RAM confirmation Number	4774
Deposit Account	503557
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	062453_002_comm_on_allowance.pdf	23385 26dcff079c0b3cdd9dc0aaa217498b5a143381d2	no	2
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	062453_002_fee_transmittal.pdf	126328 dce87fca09fc35d3659dbfb8e36cd6062841077d	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	31956 174e29407854eb6593e2a97ff4674821131f20518	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	181669		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Chi-She Chen	
SERIAL NO.:	12/240,916	CONFIRMATION No.: 6240
FILING DATE:	September 29, 2008	
TITLE:	NON-VOLATILE MEMORY MODULE	
EXAMINER:	Rojas, Midys	
ART UNIT:	2185	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPLICANT'S COMMENTS ON REASONS FOR ALLOWANCE

These comments are responsive to the Notice of Allowance, mailed on September 17, 2012.

Applicant gratefully acknowledges the indication of allowance of Claims 37-42, 61-76 and 83-90. Applicant respectfully urges that additional and/or alternative reasons for allowance may exist apart from those advanced by the Examiner and the Applicant, and these reasons may each be independently sufficient to establish the patentability of each of the allowed claims.

Applicant respectfully reserves the right to introduce, articulate, or otherwise comment on any such additional reasons for allowance as may be appropriate in any future proceedings concerning the one or more claimed embodiments.

Please charge any additional required fee or credit any overpayment to our Deposit Account number 50-3557.

Respectfully submitted,

NIXON PEABODY LLP

Dated: 9/26/12

Khaled Shami
Reg. No. 38,745

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P.O. Box 60610
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PTO/SB/08a(07-05)
Approved for use through 7/31/2006. OMB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

	Complete if Known
Application Number	12/240,916
Filing Date	September 29, 2008
First Named Inventor	Chi-She Chen
Art Unit	2189
Examiner Name	Unknown

Sheet	1	of	1

Attorney Docket No: 987-04-CON-H

US PATENT DOCUMENTS

Examiner Initial *	Cite No	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate
/M.R./		4,420,821	12-13-1983	Hoffman	02-19-1982
		4,449,205	05-15-1984	Hoffman	02-19-1982
		5,519,663	05-21-1996	Harper, Jr. et al.	09-28-1994
		6,158,015	12-05-2000	Klein	03-30-1998
		6,336,176	01-01-2002	~~Li et al.~~ Leyda, et al.	08-09-1999
		6,487,623	11-26-2002	Emerson et al.	04-30-1999
		6,658,507	12-02-2003	Chan	08-31-1998
		6,799,244	09-28-2004	Tanaka et al.	12-06-2002
		2002/0083368	06-27-2002	Abe et al.	12-20-2001
		2004/0190210	09-30-2004	Leete	03-26-2003

Change(s) applied to document
/P.M./
9/24/2012

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]

EXAMINER	/Midys Rojas/	DATE CONSIDERED	07/27/2011

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.R./

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/240,916	10/30/2012	8301833	062453-002	6240

46188 7590 10/10/2012

Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 638 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

AO 120 (Rev. 2/99)

TO: **Mail Stop 8** **Director of the U.S. Patent & Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	**REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

In Compliance with 35 § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court NORTHERN CALIFORNIA on the following X Patents or ☐ Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
CV 13-03901 DMR	8/23/2013	Northern District of California, 1301 Clay St. #400-S, Oakland, CA 94612

PLAINTIFF	DEFENDANT
DIABLO TECHNOLOGIES INC	NETLIST INC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	8,001,434		***SEE ATTACHED COMPLAINT***
2	8,301,833		
3	8,359,501		
4	8,516,185		
5	8,516,187		

In the above—entitled case, the following patent(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
Richard W. Wieking	Clara Pierce	August 27, 2013

Copy 1—Upon initiation of action, mail this copy to Commissioner **Copy 3—Upon termination of action, mail this copy to Commissioner**
Copy 2—Upon filing document adding patent(s), mail this copy to Commissioner **Copy 4—Case file copy**

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Attorneys for Plaintiff
Diablo Technologies, Inc.

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

DMR

DIABLO TECHNOLOGIES, INC.,

Plaintiff,

v.

NETLIST, INC.,

Defendant.

Case No. CV 13 3901

COMPLAINT FOR DECLARATORY JUDGMENT

DEMAND FOR JURY TRIAL

For its Complaint against Defendant NETLIST, INC., ("NETLIST"), Plaintiff Diablo Technologies, Inc. ("DIABLO") alleges as follows:

FACTUAL BACKGROUND

DIABLO

1. DIABLO is a corporation incorporated under the laws of Canada, with its principal place of business at 80 Aberdeen Street, Suite 401, Ottawa, Ontario, K1S 5R5 Canada.

2. DIABLO, founded in 2003, delivers product solutions that enhance the performance and capability of memory system designs. DIABLO developed the Memory Channel Storage™ (MCS™) architecture for enterprise servers and storage systems.

3. DIABLO has been awarded "Most Innovative Flash Memory Enterprise Business Application" in the Flash Memory Summit Best of Show Awards for enabling a new class of ultra-low latency (ULL) SSDs and application accelerators. This innovative new architecture radically transforms memory and storage for enterprise rack, blade and storage servers.

NETLIST'S THREAT OF SUIT AGAINST DIABLO

4. NETLIST purports to be incorporated under the laws of Delaware, with its principal place of business at 51 Discovery, Suite 150, Irvine, California, 92618.

5. On August 22, 2013, NETLIST sent DIABLO a letter stating that "Netlist has concluded that Smart Modular Technologies, Inc., Smart Storage Systems, Inc., Smart Worldwide Holdings, Inc. and Diablo Technologies, Inc. (collectively "Defendants") are directly and /or indirectly infringing the following United States patents at least through the making, using, offering for sale and/or selling of the recently announced ULLtraDIMM product:

U.S. Patent No. 8,001,434, Memory Board With Self-Testing Capability

U.S. Patent No. 8,301,833, Non-Volatile Memory Module

U.S. Patent No. 8,359,501, Memory Board With Self-Testing Capability

U.S. Patent No. 8,516,185, System and Method Utilizing Distributed Byte-Wise Buffers on a Memory Module

U.S. Patent No. 8,516,187, Data Transfer Scheme for Non-Volatile Memory Module"

JURISDICTION AND VENUE

6. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331, 1338, 1367, 2201, and 2202.

7. This Court has personal jurisdiction over DIABLO. Among other things, DIABLO transacts business in this jurisdiction.

8. This Court has personal jurisdiction over NETLIST. Among other things, NETLIST transacts business in this jurisdiction and is a plaintiff in this District at least in the pending action *Netlist, Inc. v. Google Inc.* 4-09-cv-05718 SBA (CAND).

9. Venue is proper in this District pursuant to 28 U.S.C. § 1391.

INTRADISTRICT ASSIGNMENT

10. For purposes of intradistrict assignment pursuant to Local Rule 3-2(c), this Intellectual Property Action is to be assigned on a district-wide basis.

COUNT I

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 8,001,434)

11. DIABLO incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs of this Complaint.

12. Upon information and belief, NETLIST is the owner of the '434 patent.

13. NETLIST is asserting the '434 patent against "ULLtraDIMM."

14. DIABLO, contends that it has not infringed and does not infringe, any valid and enforceable claim of the '434 patent.

15. An actual and justiciable controversy has thus arisen between DIABLO and NETLIST concerning the alleged infringement of the '434 patent.

COUNT II

(Declaratory Judgment of Invalidity of U.S. Patent No. 8,001,434)

16. DIABLO incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs of this Complaint.

17. Upon information and belief, NETLIST contends that the '434 patent is valid.

18. DIABLO contends that the claims of the '434 patent are invalid under 35 U.S.C. §§ 101, 102, 103, and/or 112.

19. An actual and justiciable controversy has thus arisen between DIABLO and NETLIST concerning the validity of the '434 patent.

COUNT III

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 8,301,833)

20. DIABLO incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs of this Complaint.

21. Upon information and belief, NETLIST is the owner of the '833 patent.

22. NETLIST is asserting the ' 833 patent against "ULLtraDIMM".

23. DIABLO, contends that it has not infringed and does not infringe, any valid and enforceable claim of the ' 833 patent.

24. An actual and justiciable controversy has thus arisen between DIABLO and NETLIST concerning the alleged infringement of the ' 833 patent.

COUNT IV

(Declaratory Judgment of Invalidity of U.S. Patent No. 8,301,833)

25. DIABLO incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs of this Complaint.

26. Upon information and belief, NETLIST contends that the ' 833 patent is valid.

27. DIABLO contends that the claims of the '833 patent are invalid under 35 U.S.C. §§ 101, 102, 103, and/or 112.

28. An actual and justiciable controversy has thus arisen between DIABLO and NETLIST concerning the validity of the '833 patent.

COUNT V

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 8,359,501)

29. DIABLO incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs of this Complaint.

30. Upon information and belief, NETLIST is the owner of the '434 patent.

31. NETLIST is asserting the '501 patent against "ULLtraDIMM".

32. DIABLO contends that it has not infringed and does not infringe, any valid and enforceable claim of the '501 patent.

33. An actual and justiciable controversy has thus arisen between DIABLO and NETLIST concerning the alleged infringement of the '501 patent.

COUNT VI

(Declaratory Judgment of Invalidity of U.S. Patent No. 8,359,501)

34. DIABLO incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs of this Complaint.

35. Upon information and belief, NETLIST contends that the '501 patent is valid.

36. DIABLO contends that the claims of the '501 patent are invalid under 35 U.S.C. §§ 101, 102, 103, and/or 112.

37. An actual and justiciable controversy has thus arisen between DIABLO and NETLIST concerning the validity of the '501 patent.

COUNT VII

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 8,516,185)

38. DIABLO incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs of this Complaint.

39. Upon information and belief, NETLIST is the owner of the '185 patent.

40. NETLIST is asserting the '185 patent against "ULLtraDIMM".

41. DIABLO, contends that it has not infringed and does not infringe, any valid and enforceable claim of the '185 patent.

42. An actual and justiciable controversy has thus arisen between DIABLO and NETLIST concerning the alleged infringement of the '185 patent.

COUNT VIII

(Declaratory Judgment of Invalidity of U.S. Patent No. 8,516,185)

43. DIABLO incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs of this Complaint.

44. Upon information and belief, NETLIST contends that the '185 patent is valid.

45. DIABLO contends that the claims of the '185 patent are invalid under 35 U.S.C. §§ 101, 102, 103, and/or 112.

46. An actual and justiciable controversy has thus arisen between DIABLO and NETLIST concerning the validity of the '185 patent.

COUNT IX

(Declaratory Judgment of Non-Infringement of U.S. Patent No. 8,516,187)

47. DIABLO incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs of this Complaint.

48. Upon information and belief, NETLIST is the owner of the '187 patent.

49. NETLIST is asserting the '187 patent against "ULLtraDIMM".

50. DIABLO, contends that it has not infringed and does not infringe, any valid and enforceable claim of the '187 patent.

51. An actual and justiciable controversy has thus arisen between DIABLO and NETLIST concerning the alleged infringement of the '187 patent.

COUNT X

(Declaratory Judgment of Invalidity of U.S. Patent No. 8,516,187)

52. DIABLO incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs of this Complaint.

53. Upon information and belief, NETLIST contends that the '187 patent is valid.

54. DIABLO contends that the claims of the '187 patent are invalid under 35 U.S.C. §§ 101, 102, 103, and/or 112.

55. An actual and justiciable controversy has thus arisen between DIABLO and NETLIST concerning the validity of the '187 patent.

DEMAND FOR JURY TRIAL

DIABLO demands a trial by jury on all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, DIABLO respectfully requests that the Court enter judgment for DIABLO, and award it the following relief:

A. Declare that DIABLO has not infringed, and does not infringe, any valid and enforceable claim of the '434, '833, '501, '185, and '187 patents;

B. Declare that the claims of the '434, '833, '501, '185, and '187 patents are invalid;

C. Find this case an exceptional case and award DIABLO its attorneys' fees and costs under 35 U.S.C. § 285 and all other applicable statues, rules, and laws; and

D. Grant DIABLO such other and further relief as the Court deems appropriate and just under the circumstances.

Respectfully submitted this 23rd day of August 2013.

DIABLO TECHNOLOGIES, INC.,

By: Sanjeet Dutta

WILLIAM F. ABRAMS
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Attorneys for Plaintiff
DIABLO TECHNOLOGIES, INC.

TO: **Mail Stop 8** **Director of the U.S. Patent & Trademark Office** **P.O. Box 1450** **Alexandria, VA 22313-1450**	**REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK**

In Compliance with 35 § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Northern District of California on the following:
(X) Patents or ( ) Trademarks

DOCKET NO:	DATE FILED:	UNITED STATES DISCTRICT COURT
13-cv-05889-YGR	October 7, 2014	Ronald Dellums Federal Building 1301 Clay Street Oakland, CA 94612

PLAINTIFF:	DEFENDANT:
Netlist, Inc	Smart Modular Technologies, Inc

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1. 8,001,434		See attached **THIRD AMENDED COMPLAINT FOR PATENT INFRINGEMENT**
2. 8,301,833		
3. 8,359,501		
4. 8,516,185		
5. 8,516,187		

In the above-entitled case, the following patent(s) have been included.

DATE INCLUDED INCLUDED BY:
( ) Amendment ( ) Answer ( ) Cross Bill ( ) Other Pleading

PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1. 7,881,150		
2. 8,081,536		
3.		
4.		
5.		

In the above-entitled case, the following decision has been rendered or judgment issued:

DECISION/JUDGEMENT:

Richard W. Wieking, Clerk

Clara Pierce
(by) Deputy Clerk, Clara Pierce

Copy 1 – Upon initiation of action, mail this copy to Commissioner
Copy 2 – Upon filing document adding patent(s) mail this copy to Commissioner
Copy 3 – Upon termination of action, mail this copy to the Commissioner
Copy 4 – Case file copy

Trials@uspto.gov
571-272-7822

Paper 8
Date: December 16, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK CORPORATION,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-00994
Patent 8,301,833 B1

Before: LINDA M. GAUDETTE, BRYAN F. MOORE, and GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Sandisk Corporation, Inc. ("Petitioner") filed a Petition, on June 20, 2014, requesting an *inter partes* review of claims 1–30 of US Patent No. 8,301,833 B1 (Ex. 1001, "the '833 patent"). Paper 1 ("Pet."). Netlist, Inc.

("Patent Owner") filed a Preliminary Response on October 2, 2014. Paper 7 ("Prelim. Resp.").

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Pursuant to 35 U.S.C. § 314, the Board does not find a reasonable likelihood that Petitioner would prevail with respect to at least one claim of the '833 patent and, thus, does not authorize an *inter partes* review to be instituted as to those claims.

A. Related Proceedings

Petitioner indicates that the '833 patent is involved in the following co-pending actions: *Netlist, Inc. v. Smart Modular Technologies, Inc.*, U.S. District Court for the Northern District of California, Civil Action No. 3:13-CV-05889-YGR; *Diablo Technologies, Inc. v. Netlist, Inc.*, U.S. District Court for the Northern District of California, Civil Action No. 4:13-CV-03901-YGR; and *Smart Modular Technologies, Inc. v. Netlist, Inc.*, U.S. District Court for the Northern District of California, Civil Action No. 4:13-CV-03916-YGR.). Pet. 59.

B. The '833 Patent

The invention in the '833 patent relates to a specific configuration of hybrid memory systems that addresses non-volatile memory backup, while running the volatile memory subsystem at lower power, and therefore, at lower clock speeds. Ex. 1001, col. 16, ll. 29–34. Specifically, the alleged invention of the '833 patent includes circuitry for providing a regular high-

speed clock frequency (first clock frequency) during communications between the host and the volatile memory subsystem, and a slower clock frequency during communications between the volatile memory subsystem (using third clock frequency) and the non-volatile memory subsystem (using second clock frequency). *Id.* at col. 21, ll. 5–21. Further, the second and third clock frequencies may be substantially equal. *Id.* at col. 21, ll. 23–24.

C. Illustrative Claim

Of the challenged claims, 1 and 5 are independent claims. Claim 1 is illustrative of the claimed subject matter of the '833 patent, and is reproduced below:

> 1. A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:
>
> operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;
>
> operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem; and
>
> operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

1. Prior Art Relied Upon

Petitioner relies upon the following prior art references:

Fukuzo ("Fukuzo," Ex. 1013)	US 2006/0294295 A1	June 24, 2005
Panabaker ("Panabaker," Ex. 1014)	US 7,716,411 B2	June 7, 2006
Li ("Li," Ex. 1015)	US 6,336,174 B1	August 9, 1999
Spiers ("Spiers," Ex. 1016)	US 2006/0080515 A1	October 12, 2004
Hansen ("Hansen," Ex. 1017)	US 2005/0132250 A1	December 16, 2003
Sun ("Sun," Ex. 1018)	US 7,102,391 B1	July 29, 2004
Komatsuzaki ("Komatsuzaki," Ex. 1019)	US 6,944,042 B2	December 31, 2002

2. The Asserted Grounds

Petitioner asserts that the challenged claims are unpatentable based on the following grounds:

Reference[s]	Basis	Claims challenged
Fukuzo	§ 102	1, 2, 6, 8, 11, 12, 15, 18, 22, 24, 27, and 28
Panabaker	§ 102	1–6, 8, 11–13, 15, 17–22, 24, and 27–29
Fukuzo and Li	§ 103	3 and 19
Fukuzo, Li, and Spiers	§ 103	3 and 19
Fukuzo and Hansen	§ 103	7 and 23
Fukuzo, Li, and Hansen	§ 103	7, 9, 10, 23, 25, and 26
Fukuzo and Sun	§ 103	14 and 30
Fukuzo, Li,	§ 103	14 and 30

Reference[s]	Basis	Claims challenged
and Sun		
Fukuzo and Komatsuzaki	§ 103	16
Fukuzo, Li, and Komatsuzaki	§ 103	16
Panabaker and Li	§ 103	1–6, 8, 11, 12, 15, 17–22, 24, 27, and 28
Panabaker and Spiers	§ 103	3 and 19
Panabaker, Li, and Spiers	§ 103	3 and 19
Panabaker and Hansen	§ 103	7, 9, 23, and 25
Panabaker, Li, and Hansen	§ 103	7, 9, 10, 23, 25, and 26
Panabaker and Fukuzo	§ 103	13 and 29
Panabaker, Li, and Fukuzo	§ 103	13 and 29
Panabaker and Sun	§ 103	14 and 30
Panabaker, Li, and Sun	§ 103	14 and 30
Panabaker and Komatsuzaki	§ 103	16
Panabaker, Li, and Komatsuzaki	§ 103	16

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner does not present any claim constructions, rather, Petitioner states that "each claim should be construed in accordance with its plain and ordinary meaning under the required broadest reasonable interpretation." Pet. 9–10. Patent Owner provides a construction for one term only—"clock frequency." Patent Owner argues "the claimed 'clock frequency' should be construed literally as clock frequency." Prelim Resp. 18. Because the claims refer specifically to "clock" frequency, on this record, and for purposes of this Decision, we determine that the broadest reasonable interpretation of "clock frequency" requires identification of a clock running at a particular frequency.

B. Claims 1, 2, 6, 8, 11, 12, 15, 18, 22, 24, 27, and 28—Anticipated by Fukuzo (Ex. 1013)

Petitioner argues that claims 1, 2, 6, 8, 11, 12, 15, 18, 22, 24, 27, and 28 are anticipated by Fukuzo under 35 U.S.C. § 102(a) and (e). Pet. 9–17. Fukuzo discloses an SDRAM memory chip device that comprises a non-

volatile memory controller operating a nonvolatile memory and a FIFO memory. Ex. 1013, Abstract, ¶ 27. Fukuzo's SDRAM memory chip device is used to store data to its internal SDRAM memory array (volatile memory) and to external FLASH (nonvolatile memory) using at least two additional pins as compared with conventional SDRAM standard. *Id.* Two further pins reflecting the flash memory status provide appropriate issuance of load or store signals by the host. *Id.* Fukuzo teaches using foreground and background operations such that read/write operations to volatile memory can occur simultaneously with read/write operations to non-volatile memory. *Id*

Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend. Claim 1 recites "operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Claim 15 recites "the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency." Figure 3 of Fukuzo is

reproduced below.

FIG 3

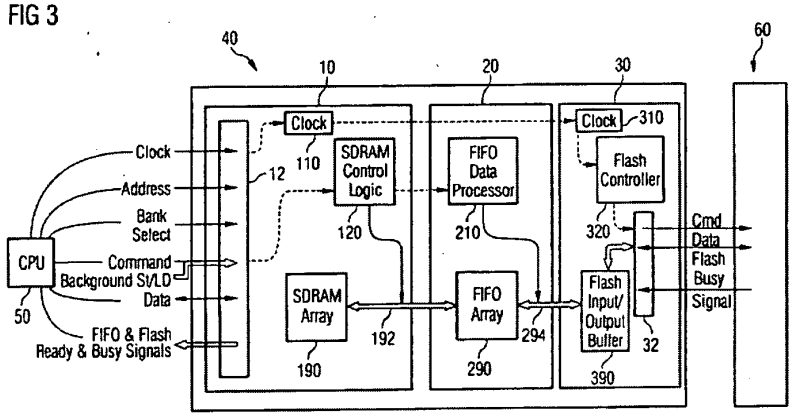

Figure 3, above, depicts a schematic block diagram of a memory chip device according to the invention of the Fukuzo device.

Petitioner asserts that Fukuzo's disclosure of SDRAM memory chip device 40 ("SDRAM Chip 40") is the claimed volatile memory subsystem and Fukuzo's disclosure of clock generator 110, which operates at 110 MHz and is valid for blocks 10 and 20 of the SDRAM chip 40, is the claimed first clock frequency. Pet. 14 (citing Ex. 1013 ¶¶ 84, 87–8). Further, Petitioner asserts that Fukuzo's disclosure of flash clock 310 which drives flash controller 320 and flash input/output buffer 390, which is described as operating at 20 MHz and is valid for block 30 of SDRAM chip 40, meets the limitation to a third clock frequency. Pet. 14 (citing Ex. 1013 ¶¶ 84, 87–88). We are not persuaded by Petitioner's argument or cited disclosure.

Petitioner reads the entire SDRAM chip 40 on the volatile memory subsystem. However, SDRAM chip 40 has at least two clocks running at different frequencies. Petitioner does not sufficiently explain how the chip reads on operating at a first frequency in one mode and a second frequency

in a second mode when the chip appears to be running both frequencies all the time or at least at the first frequency all the time. *See* Prelim. Resp. 21. It appears what Petitioner is actually doing is using blocks 10 and 20 to be the volatile memory subsystem at one time and block 30 to be the volatile memory subsystem at other times.

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984). Nonetheless, Petitioner reads inconsistently the claim limitation on two distinct structures, SDRAM core section 10 and flash controller section 30 of the SDRAM chip 40, described in the reference as being driven by two different clocks.

Petitioner presents no persuasive or credible explanation or disclosure to support this way of reading Fukuzo on the claim language. Alternately, if the Petitioner reads the volatile memory subsystem to be chip 40 as a whole, then it does not appear the chip "operates" at the frequency of flash clock 310, but rather at the frequency of the system clock 110. *See* Prelim. Resp. 21. Nonetheless, Petitioner does not explain its reading of two different clocks which drive different sets of components as corresponding to the clock for the single volatile memory subsystem of the claim.

The claim language must be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Sneed*, 710 F.2d 1544, 1548, (Fed. Cir. 1983). While it would be unreasonable to ignore any interpretive guidance afforded by the specification, *see In re Morris*, 127 F.3d 1048, 1054–55, (Fed. Cir. 1997), it is improper to read limitations from the specification into the claims. *Id.* For example, the specification of the

'833 patent discloses only one bank of volatile memory devices 32. Ex. 1001, Fig. 1. The Specification of the '833 patent discloses only one clock input into the volatile memory subsystem and does not suggest that there are subsections of the volatile memory subsystem that are operating at different clock frequencies. *Id.* at col. 15, l. 41–col. 17, l. 38.

Additionally, the specification suggests "[r]unning the volatile memory subsystem 30 at the reduced frequency during a backup and/or restore operation may advantageously reduce overall power consumption of the memory system 10." *Id.* at col. 16, ll. 34–37. Petitioner's reading of two separate sections of memory on the volatile memory subsystem is not consistent with the goal of reducing overall power consumption because the memory that Petitioner points to as running at a reduced frequency (flash/input output buffer 390) is not the same memory that is accessed by the host system (SDRAM array 190). Thus, on the record before us, Petitioner has not shown sufficiently that Fukuzo discloses the limitations to "operating the volatile memory subsystem at a third clock frequency . . . the third clock frequency being less than the first clock frequency" and "the volatile memory subsystem further being operable at a third clock frequency . . . the third clock frequency being less than the clock first frequency," as recited in independent claims 1 and 15.

Thus, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it would prevail with respect to claims 1 and 15, or claims 2, 6, 8, 11, 12, 18, 22, 24, 27, and 28 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Fukuzo.

C. Claims 1–6, 8, 11–13, 15, 17–22, 24, and 27–29 — Anticipated by Panabaker (Ex. 1014)

Petitioner argues that claims 1–6, 8, 11–13, 15, 17–22, 24, and 27–29 are anticipated by Panabaker under 35 U.S.C. § 102(e). Pet. 9–17. Panabaker discloses a hybrid memory device comprising a memory controller, a volatile memory (e.g. SDRAM) and nonvolatile memory (e.g. flash memory). *See e.g.*, Ex. 1014, Abstract, Fig. 3A, col. 7, ll. 8–11. Panabaker's memory controller operates such that the memory device has only a single memory interface with respect to voltage and access protocols defined for one type of memory. *Id.* Panabaker teaches that the memory controller allows access to both SDRAM (volatile memory) and non-volatile memory, with the non-volatile memory overlaid in one or more designated blocks of the volatile memory address space (or vice-versa). *Id.* In Panabaker, a host is coupled to the controller of the hybrid memory device, where the controller either allows a direct access to the volatile memory or uses a buffer for speed matching between the host and the nonvolatile memory. *Id.*

Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend. Claim 1 recites "operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Claim 15 recites "the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency."

Petitioner asserts that Panabaker's disclosure of SDRAM buffer set 210 as the volatile memory subsystem "is at least as fast as a given SDRAM

chip and its protocol requires . . . " meets the limitation to a first clock frequency. Pet. 19 (citing Ex. 1014, col. 4, ll. 33–47). Further, Petitioner asserts that Panabaker's disclosure of speed matching buffer set as volatile memory subsystem meets the limitation to a first clock frequency. Pet. 20 (citing Ex. 1013 ¶¶ 84, 87–88). We are not persuaded by this cited disclosure.

Petitioner apparently reads the controller 308A and the buffer 310 and the SDRAM 304 on the volatile memory subsystem in the first mode. However, in the second mode, Petitioner is unclear whether it reads the volatile memory subsystem on the controller 308A or the speed matching buffer 310. Reading the controller as the volatile memory subsystem is inconsistent with specification which discloses a controller 62 that is separate from the volatile and non-volatile memory subsystems. Ex. 1001, Fig. 1. The controller 62 provides the clock signal to the volatile and nonvolatile memory subsystems. Ex. 1001, Fig. 6. As Patent Owner points out, Petitioner does not sufficiently explain what it considers the volatile memory subsystem and does not point to any clock which provides a first or third frequency to that subsystem. *See* Prelim. Resp. 28–29.

Petitioner does not specify that Panabaker teaches that the speed matching buffer operates at a third clock frequency. For example, Panabaker teaches that a firmware protocol is used for speed matching. *See e.g.,* Ex. 1014, 6:32–36 ("As can be readily appreciated, because SDRAM is presently one or more orders of magnitude faster than flash, the protocol includes a way for the controller 308A to signal to the firmware 330 when a flash read or write request is busy and when the request is ready."). Petitioner does not explain how this scheme amounts to operating the speed

matching buffer at a third clock frequency. We find that one of ordinary skill at the time of the invention reasonably would not consider Panabaker as disclosing a volatile memory subsystem that operates at the first and third clock frequencies. Thus, on the record before us, Petitioner has not shown sufficiently that Panabaker discloses these limitations.

Therefore, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it would prevail with respect to claims 1 and 15, and claims 2–6, 8, 11–13, 17–22, 24, and 27–29 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Panabaker.

D. Obviousness Grounds

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Based on the arguments and evidence presented by Petitioner, we are unpersuaded that it has established a reasonable likelihood that it would prevail in showing the unpatentability of any of the challenged claim under

35 U.S.C. § 103 as obvious over a combination relying on either Fukuzo or Panabaker.

As discussed above in the context of the anticipation analysis with regard to Fukuzo and Panabaker, Petitioner has not shown sufficiently that Fukuzo or Panabaker discloses a volatile memory subsystem that operates at a third frequency, as is required by each of independent claims 1 and 15. Additionally, Petitioner does not provide any further explanation why Fukuzo or Panabaker disclose a volatile memory subsystem that operates at a third frequency under an obviousness analysis. Each of Petitioner's obviousness grounds assumes that either Fukuzo or Panabaker discloses that limitation. Pet. 7–9. Petitioner bears the burden of proof of showing that limitation for each independent claim. Nonetheless, as shown above, none of the challenges relied on to meet claims 1 and 15 has shown sufficiently the required "third frequency."

Thus, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it would prevail with respect to: the ground that claims 3 and 19 are unpatentable over Fukuzo and Li; the ground that claims 3 and 19 are unpatentable over Fukuzo, Li, and Spiers; the ground that claims 7 and 23 are unpatentable over Fukuzo and Hansen; the ground that claims 7, 9, 10, 23, 25, and 26 are unpatentable over Fukuzo, Li, and Hansen; the ground that claims 14 and 30 are unpatentable over Fukuzo and Sun; the ground that claims 14 and 30 are unpatentable over Fukuzo, Li, and Sun; the ground that claim 16 is unpatentable over Fukuzo and Komatsuzaki; the ground that claim 16 is unpatentable over Fukuzo, Li, and Komatsuzaki; the ground that claims 1–6, 8, 11, 12, 15, 17–22, 24, 27, and 28 are unpatentable over

Panabaker and Li; the ground that claims 3 and 19 are unpatentable over Panabaker and Spiers; the ground that claims 3 and 19 are unpatentable over Panabaker, Li, and Spiers; the ground that claims 7, 9, 23, and 25 are unpatentable over Panabaker and Hansen; the ground that claims 7, 9, 10, 23, 25, and 26 are unpatentable over Panabaker, Li, and Hansen; the ground that claims 13 and 29 are unpatentable over Panabaker and Fukuzo; the ground that claims 13 and 29 are unpatentable over Panabaker, Li, and Fukuzo; the ground that claims 14 and 30 are unpatentable over Panabaker and Sun; the ground that claims 14 and 30 are unpatentable over Panabaker, Li, and Sun; the ground that claim 16 is unpatentable over Panabaker and Komatsuzaki; the ground that claim 16 is unpatentable over Panabaker, Li, and Komatsuzaki.

III. CONCLUSION

The information presented does not show that there is a reasonable likelihood that Petitioner would prevail at trial with respect to at least one claim of the '833 patent, based on any ground presented in the petition. On this record, we deny the petition for *inter partes* review of claims 1–30.

IV. ORDER

Accordingly, it is

ORDERED that that the petition is *denied* as to all challenged claims, and no trial is instituted.

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Paper 13
Entered: March 13, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMART MODULAR TECHNOLOGIES INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-01370
Patent 8,301,833 B1

Before: LINDA M. GAUDETTE, BRYAN F. MOORE, and GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Smart Modular Technologies Inc. ("Petitioner") filed a Corrected Petition requesting an *inter partes* review of claims 1–30 of US Patent No. 8,301,833 B1 (Ex. 1009, "the '833 patent"). Paper 8 ("Pet."). Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 11 ("Prelim. Resp.").

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). Pursuant to 35 U.S.C. § 314, the Board does not find a reasonable likelihood that Petitioner would prevail with respect to at least one claim of the '833 patent and, thus, does not authorize an *inter partes* review to be instituted as to those claims.

A. Related Proceedings

Petitioner recites the District Court proceedings related to this *inter partes* review. Pet. 2–3. This *inter partes* review challenges the same patent at issue in the decision entered in IPR2014-00994 in which we denied institution. IPR2014-00994 (Paper 8).

B. The '833 Patent

The invention in the '833 patent relates to a specific configuration of hybrid memory systems that addresses non-volatile memory backup while running the volatile memory subsystem at lower power, and, therefore, at lower clock speeds. Ex. 1001, col. 16, ll. 29–34. Specifically, the alleged invention of the '833 patent includes circuitry for providing a regular high-speed clock frequency (first clock frequency) during communications between the host and the volatile memory subsystem, and a slower clock frequency during communications between the volatile memory subsystem (using a third clock frequency) and the non-volatile memory subsystem (using a second clock frequency). *Id.* at col. 21, ll. 5–21. Further, the second and third clock frequencies may be substantially equal. *Id.* at col. 21,

ll. 23–24.

C. Illustrative Claim

Of the challenged claims, 1 and 5 are independent claims. Claim 1 is illustrative of the claimed subject matter of the '833 patent, and is reproduced below:

> 1. A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:
>
> operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;
>
> operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem; and
>
> operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

D. Prior Art Relied Upon

Petitioner relies upon the following prior art references:

Reference	Patent Number	Exhibit Number
Fukuzo '295Pub	US 2006/0294295 A1	Ex. 1012
Leete '210Pub	US 2004/0190210 A1	Ex. 1013
Ichikawa '142	US 7,600,142 B2	Ex. 1014
Long '552	US 7,421,552 B2	Ex. 1015
Tsunoda '618	US 7,062,618 B2	Ex. 1016

E. The Asserted Grounds

Petitioner asserts that the challenged claims are unpatentable based on the following grounds:

Reference[s]	Basis	Claims Challenged
Fukuzo '295Pub	§ 102	1, 2, 4, 6–13, 15, 16, 18, 20, and 22–29[1]
Fukuzo '295Pub and Leete '210Pub	§ 103	3, 5, 14, 17, 19, 21 and 30
Ichikawa '142	§ 102	1, 2, 7, 8, 11–13, 15, 18, 23, 24 and 27–29
Ichikawa '142 and Leete '210Pub	§ 103	3–6, 9, 10, 14, 16, 17, 19–22, 25, 26, and 30
Long '552	§ 102	1, 2, 4, 5, 7, 12, 13, 15, 18, 20, 21, 23, 28, and 29[2]

[1] We note the challenged claims are listed at page 6 of the Petition. Also, analysis is provided starting at page 26 of the Petition. Although Claim 16 is not listed, analysis provided at page 29 of the Petition.

[2] We note the Petition isn't consistent. The challenged claims are listed as 1, 2, 4, 5, 12, 13, 15, 18, 20, 21, 28, and 29. Pet. 7. Nonetheless, analysis

Reference[s]	Basis	Claims Challenged
Long '552 and Leete '210Pub	§ 103	3, 6–11, 14, 16, 17, 19, 22–27, and 30
Tsunoda '618	§ 102	1, 2, 4, 5, 12, 13, 15, 16, 18, 20, 21, 28, and 29
Tsunoda '618 and Leete '210Pub	§ 103	3, 6–11, 14, 16, 17, 19, 22–27, and 30

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner and Patent Owner propose constructions for several terms. Pet. 19–24; Prelim Resp. 15–21. We determine that none of the terms cited by the parties require explicit construction for the purpose of this Decision.

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provided for claims 1, 2, 4, 5, 7, 12, 13, 15, 18, 20, 21, 23, 28, and 29. *See* Pet. 43–44.

B. Claims 1, 2, 4, 6–13, 15, 16, 18, 20, and 22–29—Anticipation by Fukuzo '295Pub (Ex. 1013)

Petitioner argues that claims 1, 2, 4, 6–13, 15, 16, 18, 20, and 22–29 are anticipated by Fukuzo '295Pub under 35 U.S.C. § 102(b). Pet. 24–30. Fukuzo '295Pub discloses an SDRAM memory chip device that comprises a non-volatile memory controller operating a nonvolatile memory and a FIFO memory. Ex. 1013, Abstract, ¶ 27. Fukuzo '295Pub's SDRAM memory chip device is used to store data to its internal SDRAM memory array (volatile memory) and to external FLASH (nonvolatile memory) using at least two additional pins as compared with conventional SDRAM standard. *Id.* Two further pins reflecting the flash memory status provide appropriate issuance of load or store signals by the host. *Id.* Fukuzo '295Pub teaches using foreground and background operations such that read/write operations to volatile memory can occur simultaneously with read/write operations to non-volatile memory. *Id.*

Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend. Claim 1 recites "operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Claim 15 recites "the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency." Figure 3 of Fukuzo

'295Pub is reproduced below.

FIG 3

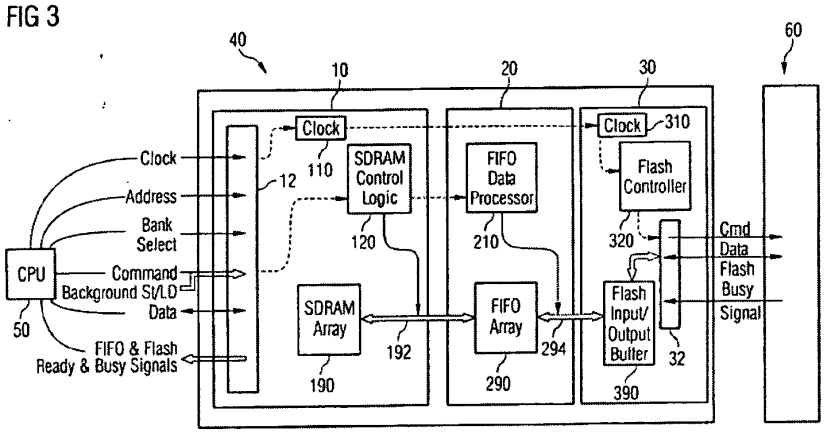

Figure 3, above, depicts a schematic block diagram of a memory chip device according to the invention of the Fukuzo '295Pub device.

Petitioner asserts that Fukuzo '295Pub's disclosure of FIFO Buffer 20 is the claimed volatile memory subsystem and Fukuzo '295Pub's disclosure that FIFO Buffer 20 operates at 130 MHz is the claimed first clock frequency. Pet. 25 (citing Ex. 1013 ¶¶ 84, 127). Further, Petitioner asserts that one of ordinary skill in the art would understand that FIFO Buffer 20 receives the same clock as the flash memory system (clocked at 20Mz) though FIFO timing generator 211, thus FIFO Buffer 20 meets the limitation to a third clock frequency. Pet. 14 (citing Ex. 1013 ¶¶ 84, 87–88). Petitioner's expert repeats this assertion without further explanation. Ex. 1010 ¶ 40. We are not persuaded by Petitioner's argument or cited disclosure.

Petitioner states, without explanation, that "the FIFO SDRAM buffer receives the same clock of the flash memory system, via the FIFO timing generator." Pet. 25. However, the cited disclosure, other than for a line in

Figure 3 between FIFO Buffer 20 and FIFO timing generator 211, does not disclose explicitly that the FIFO timing generator 211 provides the flash clock signal to FIFO Buffer 20. At best, the cited disclosure states that there is "data transfer between the SDRAM FIFO memory array 290 and the flash memory input/output buffer 390 (second data transfer bus 294)." Ex. 1001 ¶ 103. Petitioner's declarant, Dr. Nader Baghezadeh, does not provide any further explanation. Ex. 1010 ¶ 40. Petitioner does not explain sufficiently how or why FIFO timing generator 211 provides a clock signal that runs FIFO Buffer 20 at 20 MHz. *See* Prelim. Resp. 27.

Anticipation requires the disclosure in a single prior art reference of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984). We are not persuaded Petitioner has shown sufficiently that Fukuzo '295Pub discloses the limitations to "operating the volatile memory subsystem at a third clock frequency . . . the third clock frequency being less than the first clock frequency" and "the volatile memory subsystem further being operable at a third clock frequency . . . the third clock frequency being less than the clock first frequency," as recited in independent claims 1 and 15.

Thus, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood it would prevail with respect to claims 1 and 15, or claims 2, 4, 6–13, 16, 18, 20, and 22–29 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Fukuzo '295Pub.

C. Claims 3, 5, 14, 17, 19, 21 and 30—Obviousness over Fukuzo '295Pub and Leete '210Pub (Ex.1013)

Petitioner argues that claims 3, 5, 14, 17, 19, 21 and 30 would have been obvious over Fukuzo '295Pub and Leete '210Pub under 35 U.S.C. § 103(a). Pet. 30–32. Claims 3, 5, 14, 17, 19, 21 and 30 depend from independent claims 1 and 15. As discussed above, Fukuzo '295Pub fails to teach or suggest all of the elements of independent claims 1 and 15. Petitioner does not assert that Leete '210Pub overcomes the aforementioned deficiency in Fukuzo '295Pub. Thus, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood it would prevail with respect to claims 3, 5, 14, 17, 19, 21 and 30, on the ground that these claims would have been obvious over Fukuzo '295Pub and Leete '210Pub.

D. Claims 1, 2, 7, 8, 11–13, 15, 18, 23, 24 and 27–29— Anticipated by Ichikawa '142 (Ex. 1014)

Petitioner argues that claims 1, 2, 7, 8, 11–13, 15, 18, 23, 24 and 27–29 are anticipated by Ichikawa '142 under 35 U.S.C. § 102(b). Pet. 32–35. Ichikawa '142 discloses a system including volatile memory RAM 13 and nonvolatile memory system combining serial input-output (SIO) 14 with external flash memory 30. Ex. 1014, 1:12–16, 1:23–25, 1:27–28, Fig 2. Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend.

Claim 1 recites "operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Claim 15 recites "the volatile memory subsystem further being

operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency."

Petitioner asserts that Ichikawa '142's disclosure of RAM 13 as the volatile memory subsystem discloses a first clock frequency because Ichikawa '142 "discloses that RAM 13 is clocked at 5 MHz during read and write operations with the CPU 11" and Ishikawa's disclosure of RAM 13 as the volatile memory subsystem discloses a second clock frequency because Ichikawa '142 "discloses that RAM [13] functions at the 1 MHz clock during operations with SIO and external flash memory." Pet. 33 (citing Ex. 1014, 4:29–41, 55–61, 2:38–40, 3:50–56). The cited portions of Ichikawa '142 recite: "the 5-MHZ clock signal CKH is supplied to the CPU 11" (Ex. 1014, 4:37–38); "[t]he CPU 11 carries out prescribed computation and control processing . . . in synchronization with a clock signal CLK" (*id.* at 3:50–53); "[n]ormally, the central processing unit operates on a first clock signal" (*id.* at 2:38–39); and

> Operating on the l-MHZ clock signal, the CPU 11 reads one byte of the data stored in the RAM 13 (step 44), supplies the data to the serial input-output interface 14 (step 45), and gives a serial transfer command (step 46). Also operating on the l-MHZ clock signal, the serial input-output interface 14 converts the data received from the CPU 11 to serial data and transfers the data to the external memory device 30 (step 47).

id. at 4:55–61. We are not persuaded by this cited disclosure.

The cited disclosure states that CPU 11 is operating on either a 5 MHZ clock signal or a 1 MHz clock signal. There is an underlying assumption in Petitioner's argument that RAM 13 is clocked at the same speed as the CPU. Petitioner does not provide sufficient support for this

assumption. *See* Prelim. Resp. 44–45. Petitioner relies on its declarant, Dr. Bagherzadeh, for the proposition that "a POSITA would understand that the external flash memory and the RAM are communicating at the same frequency of 1 MHz to be able to transfer data between the components," (Pet. 33–34 (citing Ex. 1010 (Bagherzadeh Decl.) ¶¶ 86, 87)), but Dr. Bagherzadeh provides no evidentiary support for this conclusory statement. We note that the '833 patent shows explicitly that controller 62 provides a specific clock signal to the volatile and nonvolatile memory subsystems. Ex. 1001, 17:1–14, Fig. 7, 8. We are not persuaded Petitioner has shown sufficiently that Ichikawa '142 discloses these limitations.

Therefore, upon review of Petitioner's analysis and supporting evidence, we determine Petitioner has not demonstrated that there is a reasonable likelihood it would prevail with respect to claims 1 and 15, and claims 2, 7, 8, 11–13, 18, 23, 24 and 27–29 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Ichikawa '142.

E. Claims 3–6, 9, 10, 14, 16, 17, 19–22, 25, 26, and 30—Obviousness over Ichikawa '142 and Leete '210Pub

Petitioner argues that claims 3–6, 9, 10, 14, 16, 17, 19–22, 25, 26, and 30 would have been obvious over Ichikawa '142 and Leete '210Pub under 35 U.S.C. § 103(a). Pet. 35–41. Claims 3–6, 9, 10, 14, 16, 17, 19–22, 25, 26, and 30 depend from independent claims 1 and 15. As discussed above, Ichikawa '142 fails to teach or suggest all of the elements of independent claims 1 and 15. Petitioner does not assert that Leete '210Pub overcomes the aforementioned deficiency in Ichikawa '142. Thus, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated there is a reasonable likelihood it would prevail with

respect to claims 3–6, 9, 10, 14, 16, 17, 19–22, 25, 26, and 30, on the ground that these claims would have been obvious over Ichikawa '142 and Leete '210Pub.

F. Claims 1, 2, 4, 5, 7, 12, 13, 15, 18, 20, 21, 23, 28, and 29— Anticipation by Long '552 (Ex. 1015)

Petitioner argues that claims 1, 2, 4, 5, 7, 12, 13, 15, 18, 20, 21, 23, 28, and 29 are anticipated by Long '552 under 35 U.S.C. § 102(b). Pet. 41–44. Long '552 discloses a system including volatile memory cache 42 and nonvolatile memory vault 44. Ex. 1015, 3:47–50. Further, Long '552 discloses that the device is configured to operate at a fast clock speed, supplied with 50 to 100 watts of power when communicating normally with the host. *Id.*, 4:46–53 and 3:50–59). Long '552 discloses that the device is configured to operate at a significantly slower clock speed, supplied with 30 watts of power when communicating with the non-volatile memory 44. *Id.* 4:54–61.

Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend. Claim 1 recites "operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Claim 15 recites "the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency."

Petitioner asserts that Long '552's disclosure of controller 40[3] as the volatile memory subsystem meets the limitation to a first clock frequency

[3] We note that the Petition says "RAM 13," but that's apparently a

because Long '552 discloses that the processing circuitry of controller 40 is clocked at a relatively fast clock signal supported by 50-100 watts of power during read and write operations with the host. Pet. 42. (citing Ex. 1015, 4:46–53; 3:50–59). The cited portion of Long '552 recites:

> The clock generator circuit 46 is configured to provide a relatively-fast clock signal (or multiple clock signals) to the processing circuitry of the controller 40 during normal operation when the controller 40 is performing data storage operations on behalf of the set of hosts 22.

Ex. 1014, 4:46–51.

Petitioner asserts that Long '552 teaches a third clock frequency because "the flash memory vault is clocked at a significantly slower clock supported by less than 30 watts of power, which is applicable during read and write operations with the storage cache 42" and "one of ordinary skill would understand that since the available power is significantly less than during the host communication processes, the speed is significantly less for all the components in operation." Pet. 42. (citing Ex. 1015, 4:54–61; Ex. 1010 ¶¶ 134–135). We are not persuaded by this cited disclosure.

The citation provided does not state that storage cache 42 or flash-based memory vault 44 is clocked at a relatively fast clock signal. Rather, the cited disclosure notes that the processing circuitry of the controller is running at a relatively high clock speed and then is run on a significantly slower clock speed at a later time. This disclosure is silent as to whether

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typographical error because Long doesn't teach a RAM 13, and the cited section is about clock generator circuit 46 driving circuitry of controller 40 at "a relatively-fast clock signal (or multiple clock signals)."

storage cache 42 or flash-based memory vault 44 is running at the relatively high clock speed along with the controller. *See* Prelim. Resp. 48–49. Thus, it cannot be determined whether storage cache 42 or flash-based memory vault 44 is forced to run at a significantly lower clock speed when the available power is reduced. Petitioner does not provide objective evidence sufficient to support a finding that storage cache 42 must be necessarily clocked at the same speed as the controller. Additionally, the conclusory statements of Petitioner's declarant that a "person of ordinary skill in the art would know from education and experience that the speed is proportional to the maximum power available to the components" and "since the available power is significantly less than during the host communication processes, the speed is significantly less for all the components in operation," do not explain adequately how the this claim limitation is met. Ex. 1010 ¶ 134; *see also, e.g., In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations." (citations omitted)); *Velander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) ("In giving more weight to prior publications than to subsequent conclusory statements by experts, the Board acted well within [its] discretion."). For example, these statements in the Petition and Bagherzadeh declaration do not make clear whether clock speed being proportional to available power is always the case or whether anything in the Long reference teaches these alleged facts. Thus, we are not persuaded Petitioner has shown sufficiently that Long '552 discloses these limitations.

Therefore, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a

reasonable likelihood that it would prevail with respect to claims 1 and 15, and claims 2, 4, 5, 7, 12, 13, 18, 20, 21, 23, 28, and 29 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Long '552.

G. Claims 3, 6–11, 14, 16, 17, 19, 22–27, and 30—Obviousness over Long '552 and Leete '210Pub

Petitioner argues that claims 3, 6–11, 14, 16, 17, 19, 22–27, and 30 would have been obvious over Long '552 and Leete '210Pub under 35 U.S.C. § 103(a). Pet. 44–50. Claims 3, 6–11, 14, 16, 17, 19, 22–27, and 30 depend from independent claims 1 and 15. As discussed above, Long '552 fails to teach or suggest all of the elements of independent claims 1 and 15. Petitioner does not assert that Leete '210Pub overcomes the aforementioned deficiency in Long '552. Thus, upon review of Petitioner's analysis and supporting evidence, we determine Petitioner has not demonstrated that there is a reasonable likelihood it would prevail with respect to claims 3, 6–11, 14, 16, 17, 19, 22–27, and 30, on the ground that these claims would have been obvious over Long '552 and Leete '210Pub.

H. Claims 1, 2, 4, 5, 12, 13, 15, 16, 18, 20, 21, 28, and 29— Anticipation by Tsunoda '618 (Ex. 1016)

Petitioner argues that claims 1, 2, 4, 5, 12, 13, 15, 16, 18, 20, 21, 28, and 29 are anticipated by Tsunoda '618 under 35 U.S.C. § 102(b). Pet. 50–54. Tsunoda '618 discloses a system including SDRAM volatile memory cache 4010 and flash non-volatile memory 4020. Ex. 1016, 4:2-6. Further, Tsunoda '618 discloses that the device is configured to operate the volatile memory 42 at a high SDRAM speed, when communicating normally with the host (*id.*, 13:51–53, 11:51–54, and 12:27–31). Tsunoda '618 discloses that the device is configured to operate at a speed different from the high

speed, when communicating with the non-volatile memory 44. *Id.* 12:21–25, 13:55–58, and 11:51–54.

Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend. Claim 1 recites "operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Claim 15 recites "the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency."

Petitioner asserts that Tsunoda '618's disclosure of speed matching buffer 108 within the SDRAM discloses a first clock frequency. Pet. 51–52 (citing Ex. 1016, 11:51–54). We are not persuaded by this cited disclosure.

Petitioner apparently reads buffer 108 and SDRAM 103 on the volatile memory subsystem. However, speed matching buffer 108 is a part of memory control unit 104. Ex. 1016, Fig. 1. Reading the controller as the volatile memory subsystem is inconsistent with Tsunoda '618's disclosure that controller 62 is *separate from* the volatile and non-volatile memory subsystems. Ex. 1001, Fig. 1. Controller 62 provides the clock signal to the volatile and nonvolatile memory subsystems. Ex. 1001, Fig. 6. As Patent Owner points out, Petitioner does not explain sufficiently why the controller is a part of the volatile memory subsystem. *See* Prelim. Resp. 56–58. We find that one of ordinary skill at the time of the invention would not have considered reasonably Tsunoda '618 as disclosing a volatile memory subsystem that operates at the first and third clock frequencies. Thus, , we

are not persuaded Petitioner has shown sufficiently that Tsunoda '618 discloses these limitations.

Therefore, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it would prevail with respect to claims 1 and 15, and claims 2, 4, 5, 12, 13, 16, 18, 20, 21, 28, and 29 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Tsunoda '618.

I. Claims 3, 6–11, 14, 17, 19, 22–27, and 30—Obviousness over Tsunoda '618 and Leete '210Pub

Petitioner argues that claims 3, 6–11, 14, 17, 19, 22–27, and 30 would have been obvious over Tsunoda '618 and Leete '210Pub under 35 U.S.C. § 103(a). Pet. 54–59. Claims 3, 6–11, 14, 17, 19, 22–27, and 30 depend from independent claims 1 and 15. As discussed above, Tsunoda '618 fails to teach or suggest all of the elements of independent claims 1 and 15. Petitioner does not assert that Leete '210Pub overcomes the aforementioned deficiency in Tsunoda '618. Thus, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it would prevail with respect to claims 3, 6–11, 14, 17, 19, 22–27, and 30, on the ground that these claims would have been obvious over Tsunoda '618 and Leete '210Pub.

III. CONCLUSION

The information presented does not show that there is a reasonable likelihood that Petitioner would prevail at trial with respect to at least one claim of the '833 patent, based on any ground presented in the Petition. We deny the Petition for *inter partes* review of claims 1–30.

IV. ORDER

Accordingly, it is

ORDERED that that the Petition is *denied* as to all challenged claims, and no trial is instituted.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00649
Patent 8,301,833 B1

Before BRYAN F. MOORE, GEORGIANNA W. BRADEN, and SHEILA F. McSHANE, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc. ("Petitioner") requests *inter partes* review of claims 1–30 of

U.S. Patent No. 8,301,833 B2 ("the '833 Patent," Ex. 1001) pursuant to 35 U.S.C. §§ 311 *et seq*. Paper 1 ("Pet."). Netlist, Inc. ("Patent Owner") filed a preliminary response. Paper 6 ("Prelim. Resp."). Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.108. Upon consideration of the Petition and Preliminary Response, we conclude the information presented shows there is not a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 1–30 of the '833 Patent.

A. Related Matters

Petitioner recites the District Court proceedings related to this *inter partes* review. Pet. 2. The Board has twice declined to institute an *inter partes* review of claims 1–30 of the '883 Patent. *Sandisk Corporation v. Netlist, Inc.*, Case IPR2014-00994 (PTAB December 16, 2014) (Paper 8) (rehearing denied, Paper 10); *Smart Modular Technologies Inc. v. Netlist, Inc.*, Case IPR2014-01370 (PTAB March 13, 2015) (Paper 13)).

Considering the particular circumstances of this case, we address the merits of the Petition and do not exercise our discretion under 35 U.S.C. § 325(d) (indicating "if another proceeding or matter involving the patent is before the Office, the Director may determine the manner in which the post-grant review or other processing or matter may proceed . . . and may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office") and/or 35 U.S.C. § 314(a) (authorizing institution of an *inter*

partes review under particular circumstances, but not requiring institution under any circumstances). *See* 37 C.F.R. § 42.108(a) ("the Board may authorize the review to proceed") (emphasis added); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (explaining that under § 314(a), "the PTO is permitted, but never compelled, to institute an IPR proceeding"). Petitioner was not a party to any of the prior proceedings. In addition, this Petition raises new issues, including asserting obviousness in view of references not at issue in the previous proceedings. Pet. 3.

B. The '833 Patent

The invention in the '833 patent relates to a specific configuration of hybrid memory systems that addresses non-volatile memory backup while running the volatile memory subsystem at lower power, and, therefore, at lower clock speeds. Ex. 1001, 16:29–34. Specifically, the alleged invention of the '833 patent includes circuitry for providing a regular high-speed clock frequency (first clock frequency) during communications between the host and the volatile memory subsystem, and a slower clock frequency during communications between the volatile memory subsystem (using a third clock frequency) and the non-volatile memory subsystem (using a second clock frequency). *Id.* at 21:5–21. Furthermore, the second and third clock frequencies may be substantially equal. *Id.* at 21:23–24.

C. Illustrative Claim

Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

> operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;
>
> operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem; and
>
> operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

Ex. 1001, 21:6–22.

D. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–30 are unpatentable based on the following grounds:

References	**Basis**	**Claim(s) challenged**
Bonella[1] and Mills[2]	§ 103	1–30
Bonella, Mills, and Ashmore[3]	§ 103	1–30
Bonella, Mills, Ashmore and Larson[4]	§ 103	7 and 23
Bonella, Mills, Ashmore and Windows 2000[5]	§ 103	8–10, 24–26

[1] US Publication No. 2007/0136523 A1, filed December 8, 2006 ("Bonella," Ex. 1005). Claims priority to US Provisional No. 11/635,926 filed December 8, 2005.
[2] US Patent No. 6,026,465, issued February 15, 2000 ("Mills," Ex. 1007).
[3] US Publication No. 2006/0212651 A1, published September 21, 2006 ("Ashmore," Ex. 1008).
[4] US Patent No. 6,571,244 B1, issued May 27, 2003 ("Larson," Ex. 1019).
[5] MICROSOFT WINDOWS 2000 PROFESSIONAL RESOURCE KIT, lists Feb. 2, 2000 date of publication ("Windows 2000," Ex. 1021).

Bonella, Mills, Ashmore and Klein[6]	§ 103	16
Bonella, Mills, Ashmore and Maeda[7]	§ 103	17

Pet. 3, 14–59.

II. DISCUSSION

A. Claim Construction

In an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Consistent with the broadest reasonable construction, claim terms are presumed to have their ordinary and customary meaning as understood by a person of ordinary skill in the art in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

At this juncture of the proceeding, we determine that it is not necessary to provide an express interpretation of any term of the claims.

B. Asserted Obviousness over Bonella and Mills

Petitioner contends claims 1–30 are unpatentable under 35 U.S.C. § 103(a) as obvious over Bonella and Mills. Pet. 14–48. Relying on the testimony of Ron Maltiel, Petitioner explains how Bonella and Mills allegedly describe all of the claim limitations. *Id.* (citing Ex. 1003).

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[6] US Patent No. 6,721,860 B2, issued April 3, 2004 ("Klein," Ex. 1009).
[7] US Publication No. 2005/0249011 A1, published November 10, 2005 ("Maeda," Ex. 1013).

1. Bonella (Ex. 1005)

Bonella is directed to a plug-and-play end-user add-in memory module for computers and consumer electronic devices. Ex. 1005 ¶ 2. Bonella discloses a memory module including a volatile memory, a non-volatile memory, and a controller that provides address, data, and control interfaces to the memories and to a host system. *Id.* ¶ 6.

Bonella teaches a "Power Level 5" state that allows for full function, full performance operation. *Id.* ¶ 47. Bonella also teaches a "Power Level 4" state that reduces the power consumption of the memory module by limiting the DRAM performance. *Id.* ¶ 48.

Bonella also teaches that the DRAM write buffer is occasionally backed up to the internal FLASH memory so as to ensure data integrity in case of a power loss. *Id.* ¶ 96. This write buffer flushing can be triggered by a power loss event, which then causes Bonella's "Power loss algorithm" to be executed:

> When the memory module controller detects a power loss event, the data that is flagged as critical is flushed to the FLASH, a flag is set and the memory module then shuts down. At new power on the normal power on sequence is followed and data restored to the DRAM.

Id. ¶ 101.

During the execution of the power loss algorithm, Bonella's memory relies on backup power such as, for example, Uninterruptible Power Supply (UPS) capacitors. *Id.* ¶ 29.

2. Mills (Ex. 1007)

Mills describes several interfaces for a FLASH memory device, one of which is a synchronous FLASH interface, i.e. "a synchronous flash

interface (SFI) flash memory integrated circuit 600 that incorporates a complete synchronous flash interface in a single flash memory chip." Ex. 1007, 16:60–63. The synchronous FLASH interface includes a clock input such that all the external operations of the device are synchronized to the rising edge of the clock. *Id.* at 17:10–25.

Mills teaches that this synchronous operation is used for both read operations and write operations: "When SFI is enabled, interlace control 670 and [bank] select logic 674 operate to interlace read (and write) operations between flash bank A 610 and a flash bank B 620 . . . ." *Id.* at 17:33–39. Because "the device is interleaved internally," it "creates an average access time for sequential read accesses that is significantly less than the access time of an asynchronous flash device." *Id.* at 17:1–9.

3. Analysis

Claims 1 and 15 recite generally three limitations (excluding the preamble). We determine that Petitioner has not shown a reasonable likelihood that Bonella teaches the third limitation of claims 1 and 15, i.e. "operating the volatile memory subsystem [operable] at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Below, we summarize Petitioner's position as to the other two limitations of claims 1 and 15 to provide context for the discussion of the third limitation.

In a first limitation, claims 1 and 15 recite "operating the volatile memory subsystem [operable] at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system." Petitioner argues that Bonella discloses this feature. Pet. 15–19. Petitioner contends

"[o]ne of ordinary skill in the art would understand that Bonella's DRAM [volatile memory subsystem] is operating at the particular frequency of the clock signal ("CLK")." *Id.* at 16 (citing Ex. 1005 ¶ 52; Ex. 1003 ¶ 92).

Petitioner also contends, Bonella teaches its memory module has multiple power states, including Power Level 5 [first mode] which "allows for full function, full performance operation" with "no preset restrictions placed on the DRAM" and when "a skilled artisan would understand . . . 'data is communicated between the volatile memory subsystem and the host system' during a read from and write to the DRAM write buffer." Pet. 17–18 (quoting Ex. 1005 ¶ 6, 8–9, 47, Abstract; Ex. 1003 ¶ 98).

In a second limitation, claims 1 and 15 recite "operating the non-volatile memory subsystem [operable] at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem." Petitioner argues that the combination of Bonella and Mills teach this feature. Pet. 19–24.

Petitioner admits "Bonella does not explicitly disclose "*operating the non-volatile memory subsystem*" (the FLASH memory) "*at a second clock frequency*" during this second mode . . . ." Pet. 21. According to Petitioner, Mills discloses a synchronous Flash interface where read and write operations are synchronized to the rising edge of a clock signal provided to the device and operating at a particular frequency (i.e., "*operating [a] non-volatile memory subsystem at a second clock frequency*")." Pet. 21–22 (citing Ex. 1007, 16:60–63, 17:10–25; Ex. 1003 ¶ 106–107). As explained below, we determine Bonella does not teach operating the volatile memory subsystem [operable] at a third clock frequency when the memory system is

in the second mode of operation, the third clock frequency being less than the first clock frequency, as recited in claims 1 and 15, therefore, we do not decide whether Petitioner has combined Bonella and Mills properly. Below we discuss Petitioner's contentions regarding Bonella that are relevant to the discussion of the third claim limitation.

Petitioner contends Bonella teaches a FLASH memory and associated controller and in the alleged "first mode of operation" Bonella used the DRAM buffer as a write buffer and periodically flushes the write data to the FLASH memory. *Id.* at 20 (citing 1005 ¶ 96; Fig. 1, Ex 1003 ¶¶ 94–97). On the other hand, Petitioner further contends that during a power loss event, the memory module flushes critical data to the FLASH memory–this is Petitioner's alleged "second mode of operation." *Id.* (citing 1005 ¶ 101, Ex 1003 ¶¶ 103).

In a third limitation, claims 1 and 15 recite "operating the volatile memory subsystem [operable] at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Petitioner argues that Bonella discloses this feature. Pet. 23–30. Petitioner contends Bonella discloses modes of operation supported by the system, including a power saving mode [Power Level 4] which saves power in part by reducing the frequency at which the DRAM is operating. Pet. 24–25 (citing Ex 1003 ¶ 116). Table 1, showing the power modes according to Bonella, is reproduced below.

TABLE 1

Partial List of ACPI Power States

ACPI Power State	Power Source	Power Level (0–5)	Memory Module operational Condition
D0	Line/ Battery	5	No operational restrictions, full power
D0	Battery	4	PCIe/DRAM performance reduction, no FLASH restrictions
D0	Battery	3	PCIe/DRAM DRAM wr buffer only, FLASH restrictions
D1	Line/ Battery	2	DRAM in standby, FLASH idle
D1	Battery	1	DRAM in standby, FLASH standby
D1	Battery	0	DRAM off, FLASH standby

Table 1 (Ex. 1005, Table 1), above, shows Power Level 4 which operates at a reduced frequency that Petitioner contends is the claimed "third frequency." Pet. 24–25. According to Petitioner, "A skilled artisan would understand a DRAM operating at a 'reduced' frequency in such a power saving mode [Power Level 4] to be operating at a clock frequency lower than the clock frequency at which the DRAM would operate in a normal operating mode, such as Power Level 5 of Bonella." *Id.* at 25 (citing Ex. 1003 ¶ 118).

Specifically, Petitioner asserts

> Bonella's power flush algorithm (i.e., the "second mode") would still be triggered during Bonella's "power saving" mode of operation (i.e., when the DRAM was operating at a "third clock frequency") if a power loss event occurred. Bonella teaches that the memory module's backup power source is located within the memory module, Ex. 1005, ¶29, and that the external power source can be a "Line" or "Battery," even under less than "full power" operation, *id.*, ¶46. One of ordinary skill in the art would understand that Bonella's memory module, when operating under a "power saving" mode that reduced the DRAM operating frequency (i.e., a "third clock frequency"), could still lose its external power source and be forced to switch to the power loss

> algorithm (i.e., the "second mode"). Ex. 1003, ¶119. Bonella thus teaches to one of ordinary skill in the art at least one situation where the '*volatile memory subsystem*' operates '*at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency.*'

Pet. 25–26.

Patent Owner asserts that "Bonella does not teach that the alleged VMS [volatile memory system] operates at the alleged 'third clock frequency' during the alleged 'second mode of operation.'" Prelim. Resp. 26. Petitioner asserts the "second mode of operation" is the power loss operation described in paragraph 101 of Bonella (Pet. 20), however, Patent Owner disagrees. *Id.* at 25. Contrary to Petitioner's position, Patent Owner correctly explains, as a complement to that assertion, that the power source during that alleged "second mode of operation" is the battery uninterruptible power supply ("UPS") and/or the capacitor ("CAP") UPS because line and battery power from the alleged "host system" has been lost. *Id.* (citing Ex. 1005 ¶ 33).

Petitioner asserts that the DRAM (the alleged volatile memory system) operates at the alleged "*third clock frequency*" during Power Level 4. Pet. 20. As quoted above, Petitioner asserts "when operating under a 'power saving' mode that reduced the DRAM operating frequency (*i.e.*, a "*third clock frequency*"), could still lose its external power source and be forced to switch to the power loss algorithm (*i.e.*, the "*second mode*")." *Id.* Petitioner does not point to any disclosure in Bonella, however, that indicates what frequency the DRAM is operating at during a power loss. Rather, as Patent Owner explains, the battery associated with Power Level 5 (alleged "first mode of operation") and Power Level 4 (alleged "second

frequency") is a not the UPS battery so there is no suggestion in Bonella about what frequency the DRAM runs at when powered by the UPS battery. Prelim Resp. 25–26. Thus, we agree with Patent Owner's assertions that "the Petition fails to show evidence that operating in a 'power saving' mode prior to Bonella's 'power loss algorithm' has any effect on the operating frequencies during the 'power loss algorithm.'" Prelim. Resp. 29–30.

Petitioner does not provide sufficient objective evidence sufficient to support a finding that the DRAM operates at the frequency of Power Level 4 when a power failure occurs during Power Level 4. Additionally, the conclusory statements of Petitioner's declarant, which are essentially identical to the statements in the Petition, do not explain adequately how the limitation to a "third frequency" is met. Ex. 1003 ¶ 116–120; *see also, e.g., In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations." (citations omitted)); *Velander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) ("In giving more weight to prior publications than to subsequent conclusory statements by experts, the Board acted well within [its] discretion."). For example, statements in the Petition and Maltiel's declaration do not make clear where Bonella states that during a power loss the DRAM runs at the frequency of the power lever state immediately preceding the power loss, or whether anything in the Bonella reference teaches that alleged fact.

Petitioner also asserts that

> [u]sing Bonella's power reduction technique during the power loss algorithm would also have been the arrangement of old elements (Bonella's power reduction mode and Bonella's power

> loss algorithm), each performing the same function it had been known to perform, in a way that yields no more than one of ordinary skill in the art would expect from such an arrangement (reducing power consumption during a power loss event, as suggested by Long and Ashmore).

Pet. 29 (citing Ex. 1003 ¶ 126). Petitioner further asserts "[o]ne of ordinary skill in the art would know that Bonella's backup power supply is not unlimited and therefore would have been motivated to conserve power during such emergency backup operations in order to ensure backup of all unsaved data, or at least as much as possible." *Id.* at 27 (citing Ex. 1003 ¶ 122). Petitioner has not shown, however, how or why Bonella's power reduction modes are applicable during a power loss event, given that during a power loss event power is supplied by the UPS, and not the external Line/battery that supplies power under normal operations.

Petitioner asserts that Ashmore supports that contention that running at the frequency associated with Power Level 4 during a power loss would have been obvious because Ashmore "provides a method for reducing battery power consumption during a main power loss to reduce the likelihood of loss of user write-cached data in a write-caching mass storage controller." Pet. 28 (quoting Ex. 1008 ¶ 9) (emphasis added). Specifically, Petitioner asserts Ashmore "only provide[s] battery power to the critical memory banks, but not to the non-critical memory banks, in order to reduce the amount of battery power consumed during the main power outage." *Id.* (quoting Ex. 1008 ¶ 9). We are not persuaded by this cited disclosure.

The Ashmore citation relied upon does not state that the operating frequency of the memory bank is adjusted. Petitioner does not point to a motivation to adjust the frequency of the memory banks specifically, simply a general motivation to reduce battery power during power loss. Thus, we

are not persuaded Ashmore supports that contention that running at the frequency associated with Power Level 4 during a power loss would have been obvious.

Petitioner also asserts that Long supports that contention that running at the frequency associated with Power Level 4 during a power loss would have been obvious because Long "'provide[s] a significantly slower clock signal to the processing circuitry' *of a memory* 'while the controller 40 moves data from the volatile-memory storage cache 42 to the flash-based memory vault 44.'" Pet. 28 (quoting Ex. 1011, 4:54–64) (emphasis added). We are not persuaded by this cited disclosure.

The Long citation relied upon does not state that storage cache 42 or FLASH-based memory vault 44 is clocked at a relatively fast clock signal. Petitioner leaves out the part of the quote that states that it is specifically the "processing circuitry *of the controller 40*" is run at a lower clock speed. That is, the cited disclosure notes that the processing circuitry of the controller is running at a relatively high clock speed and then is run on a significantly slower clock speed at a later time. This disclosure is silent as to whether storage cache 42 or FLASH-based memory vault 44 is running at the relatively high clock speed along with the controller. Thus, it cannot be determined whether storage cache 42 or FLASH-based memory vault 44 is forced to run at a significantly lower clock speed when the available power is reduced. Thus, we are not persuaded Long supports that contention that running at the frequency associated with Power Level 4 during a power loss would have been obvious.

Accordingly, for the reasons stated above, Petitioner has not shown there is a reasonable likelihood of prevailing in establishing that claims 1

and 15, and claims 2–14 and 16–30 that depend therefrom, would have been obvious over Bonella and Mills.

C. Asserted Obviousness over Bonella, Mills, and Ashmore

Petitioner contends claims 1–30 are unpatentable under 35 U.S.C. § 103(a) as obvious over Bonella, Mills, and Ashmore. Pet. 48–49. As explained above, we determine that Petitioner has not shown a reasonable likelihood that Bonella and Mills renders obvious the "third frequency" limitation of claims 1 and 15, even considering the disclosure of Ashmore. Thus, Petitioner has not shown there is a reasonable likelihood of prevailing in establishing the unpatentability of claims 1–30 of the '833 Patent as obvious over Bonella, Mills, and Ashmore.

D. Remaining Asserted Obviousness Grounds

As discussed above in the context of the obviousness analysis with regard to Bonella, Mills, and Ashmore, Petitioner has not shown sufficiently that Bonella, Mills, and/or Ashmore teaches "a volatile memory subsystem" that operates at a "third frequency," as is required by each of independent claims 1 and 15. Each of Petitioner's remaining obviousness grounds assumes that either Bonella or Ashmore discloses that limitation. Pet. 50–59. Petitioner bears the burden of proof of showing that limitation for each independent claim. Nonetheless, as shown above, none of the challenges Petitioner relied on to meet claims 1 and 15 shows sufficiently the required "third frequency."

Thus, upon review of Petitioner's analysis and supporting evidence and Patent Owner's response and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it

would prevail with respect to: (1) the ground that claims 7 and 23 are unpatentable over Bonella, Mills, with or without Ashmore, and Larson; (2) the ground that claims 8–10 and 24–26 are unpatentable over Bonella, Mills, with or without Ashmore, and Windows 2000; (3) the ground that claim 16 is unpatentable over Bonella, Mills, with or without Ashmore, and Klein; and (4) the ground that claim 17 is unpatentable over Bonella, Mills, with or without Ashmore, and Maeda.

III. CONCLUSION

The information presented does not show that there is a reasonable likelihood that Petitioner would prevail at trial with respect to at least one claim of the '833 patent, based on any ground presented in the Petition. On this record, we deny the Petition for *inter partes* review of claims 1–30.

IV. ORDER

Accordingly, it is

ORDERED that that the Petition is *denied* as to all challenged claims, and no trial is instituted.

IPR2017-00649
Patent 8,301,833 B1

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PTO/SB/96 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Chi-She Chen et al.

Application No./Patent No.: 8,301,833 Filed/Issue Date: 10-30-2012

Titled: NON-VOLATILE MEMORY MODULE

Netlist, Inc. , a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is _____ %); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 028504, Frame 0323, or for which a copy therefore is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Khaled Shami/ July 10, 2018

Signature Date

Khaled Shami, Reg. No. 38,745 Attorney for Assignee

Printed or Typed Name Title

PTO/SB/80 (11-08)
Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☑ Practitioners associated with the Customer Number: 151145

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☑ The address associated with Customer Number: 151145

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

Netlist, Inc.
175 Technology Drive, Suite 150
Irvine, CA 92618

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	[signature]	Date	12/5/17
Name	Noel B. Whitley	Telephone	949-639-0115
Title	VP, IP & Licensing		

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	33131184
Application Number:	12240916
International Application Number:	
Confirmation Number:	6240
Title of Invention:	NON-VOLATILE MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	46188
Filer:	Khaled Shami/Casey Berger
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-002
Receipt Date:	10-JUL-2018
Filing Date:	29-SEP-2008
Time Stamp:	12:11:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	00160010002_POA.pdf	941908 938e52ddd4bb70fc441d95d4ead37c66e97f12c2	no	2

Warnings:

The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing	
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Total Files Size (in bytes):	941908

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/240,916	09/29/2008	Chi-She Chen	

CONFIRMATION NO. 6240

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

POA ACCEPTANCE LETTER

OC000000101000648

Date Mailed: 07/17/2018

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/10/2018.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/nrhayden/

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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/240,916	09/29/2008	Chi-She Chen	062453-002

CONFIRMATION NO. 6240

46188
Nixon Peabody LLP
P.O. Box 26769
San Francisco, CA 94126

POWER OF ATTORNEY NOTICE

OC000000101000575

Date Mailed: 07/17/2018

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/10/2018.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/nrhayden/

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. ƒ 290 and/or 15 U.S.C. ƒ 1116 you are hereby advised that a court action has been filed in the U.S. District Court **Western District of Texas** on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. ƒ 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:21-cv-00430	4/28/2021	Western District of Texas

PLAINTIFF	DEFENDANT
Netlist, Inc.	Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	8,301,833	10/30/2012	Netlist, Inc.
2			
3			
4			
5			

In the above´ entitled case, the following patent(s)/trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above´ entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1´ Upon initiation of action, mail this copy to Director Copy 3´ Upon termination of action, mail this copy to Director
Copy 2´ Upon filing document adding patent(s), mail this copy to Director Copy 4´ Case file copy