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	First Named Inventor: to be determined
	Title: NON-VOLATILE MEMORY MODULE

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Commissioner for Patents
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The following enclosures are transmitted herewith to be filed in the patent application of:

      Inventor(s):
      1.   to be determined

APPLICATION:

    (X) Specification in 40 pages.

    (X) Drawings in 12 sheets.

CONTINUITY INFORMATION:

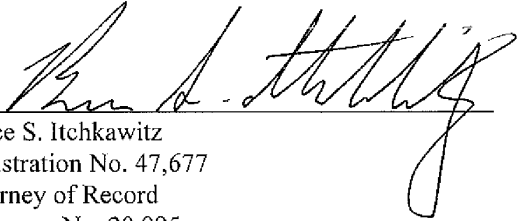| Application	Relationship	Parent App. No.	Filing Date	Status
This Application	Non-Provisional of	60/941,586	6/01/2007	closed

Reference to prior domestic applications is made in the:

    (X) Specification.

OTHER APPLICATION PARTS:

FILING FEES:

    (X) The total fees will be paid at a later date.

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NON-VOLATILE MEMORY MODULE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001]   The present application claims the benefit of priority from U.S. Provisional Application No. 60/941,586, filed June 1, 2007, which is incorporated in its entirety by reference herein.

BACKGROUND

[0002]   Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the computer system to provide volatile memory to the computer system.

[0003]   Volatile memory generally maintains stored information only when it is powered. Batteries have been used to provide power to volatile memory during power failures or interruptions. However, batteries may require maintenance, may need to be replaced, are not environmentally friendly, and the status of batteries can be difficult to monitor.

[0004]   Non-volatile memory can generally maintain stored information while power is not applied to the non-volatile memory. In certain circumstances, it can therefore be useful to backup volatile memory using non-volatile memory.

SUMMARY

[0005]   In certain embodiments, a memory system coupled to a computer system is provided which includes a volatile memory subsystem, a non-volatile memory subsystem, and a controller operatively coupled to the non-volatile memory subsystem. The memory system can also include at least one circuit configured to selectively operatively decouple the controller from the volatile memory subsystem.

[0006]   In some embodiments, a power module for providing a plurality of voltages to a memory system is described. The power module includes non-volatile and volatile memory, and the plurality of voltages include at least a first voltage and a second voltage. The power module of certain embodiments includes an input providing a third

voltage to the power module and a voltage conversion element configured to provide the second voltage to the memory system. The power module also includes a first power element configured to selectively provide a fourth voltage to the conversion element. The power module further includes a second power element configured to selectively provide a fifth voltage to the conversion element. The power module can be configured to selectively provide the first voltage to the memory system either from the conversion element or from the input.

[0007]   The power module can be configured to be operated in at least three states in certain embodiments. In a first state, the first voltage is provided to the memory system from the input and the fourth voltage is provided to the conversion element from the first power element. In a second, state the fourth voltage is provided to the conversion element from the first power element and the first voltage is provided to the memory system from the conversion element. In a third state, the fifth voltage is provided to the conversion element from the second power element and the first voltage is provided to the memory system from the conversion element.

[0008]   A method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems is provided in certain embodiments. The method includes, during a first condition, providing the first voltage to the memory system from an input power supply and providing the second voltage to the memory system from a first power subsystem. The method further includes detecting a second condition and, during the second condition, providing the first voltage and the second voltage to the memory system from the first power subsystem. The method also includes charging a second power subsystem and detecting a third condition. During the third condition, the method includes providing the first voltage and the second voltage to the memory system from the second power subsystem.

[0009]   In certain embodiments, a method is provided for controlling a memory system operatively coupled to a host system and which includes a volatile memory subsystem and a non-volatile memory subsystem. The method can include operating the volatile memory subsystem at a first frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the

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host system. In certain embodiments, the method further includes operating the non-volatile memory subsystem at a second frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem. The method can also include operating the volatile memory subsystem at a third frequency when the memory system is in the second mode of operation, the third frequency less than the first frequency.

[0010]   In certain embodiments, a method is provided for controlling a memory system operatively coupled to a host system. The memory system includes a volatile memory subsystem and a non-volatile memory subsystem. In certain embodiments, the method includes communicating data words between the volatile memory subsystem and the host system when the memory system is in a first mode of operation. The method can further include transferring data words from the volatile memory subsystem to the non-volatile memory subsystem when the memory system is in a second mode of operation. Transferring each data word can include storing a first portion of the data word in a buffer, storing a second portion of the data word in the buffer, and writing the entire data word from the buffer to the non-volatile memory subsystem.

[0011]   A memory system operatively coupled to a host system is provided in certain embodiments. The memory system can include a volatile memory subsystem and a non-volatile memory subsystem comprising at least 100 percent more storage capacity than does the volatile memory subsystem. The memory system includes a controller operatively coupled to the volatile memory subsystem and operatively coupled to the non-volatile memory subsystem, the controller configured to allow data to be communicated between the volatile memory subsystem and the host system when the memory system is operating in a first state and to allow data to be communicated between the volatile memory subsystem and the non-volatile memory subsystem when the memory system is operating in a second state.

[0012]   A method of controlling a memory system operatively coupled to a host system is provided in certain embodiments. The memory system includes a volatile memory subsystem and a non-volatile memory subsystem. The method can include communicating data between the volatile memory subsystem and the host system when the memory system is in a first mode of operation. The method of certain embodiments further includes storing a

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first copy of data from the volatile memory subsystem to the non-volatile memory subsystem at a first time when the memory system is in a second mode of operation. The method may further include restoring the first copy of data from the non-volatile memory subsystem to the volatile memory subsystem and erasing the first copy of data from the non-volatile memory subsystem. In certain embodiments, the method also includes storing a second copy of data from the volatile memory subsystem to the non-volatile memory subsystem at a second time when the memory system is in the second mode of operation, wherein storing the second copy begins before the first copy is completely erased from the non-volatile memory subsystem.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013]   Figure 1 is a block diagram of an example memory system compatible with certain embodiments described herein.

[0014]   Figure 2 is a block diagram of an example memory module with ECC (error-correcting code) having a volatile memory subsystem with nine volatile memory elements and a non-volatile memory subsystem with five non-volatile memory elements in accordance with certain embodiments described herein.

[0015]   Figure 3 is a block diagram of an example memory module having a microcontroller unit and logic element integrated into a single device in accordance with certain embodiments described herein.

[0016]   Figures 4A-4C schematically illustrate example embodiments of memory systems having volatile memory subsystems comprising registered dual in-line memory modules in accordance with certain embodiments described herein.

[0017]   Figure 5 schematically illustrates an example power module of a memory system in accordance with certain embodiments described herein.

[0018]   Figure 6 is a flowchart of an example method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems.

[0019]   Figure 7 is a flowchart of an example method of controlling a memory system operatively coupled to a host system and which includes at least 100 percent more storage capacity in non-volatile memory than in volatile memory.

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