NON-VOLATILE MEMORY MODULE

BACKGROUND OF THE INVENTION

[0001] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (*e.g.*, a server system or a personal computer) and are accessed by the processor of the computer system to provide volatile memory to the computer system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Figure 1 is a block diagram of an example 512MB DDR2 (PC2-3200) memory module in accordance with certain embodiments described herein.

[0003] Figure 2 is a block diagram of an example memory module with ECC (error-correcting code) having a first memory bank with nine volatile memory elements and a second memory bank with five non-volatile memory elements in accordance with certain embodiments described herein.

[0004] Figure 3 is a block diagram of an example memory module with ECC and having a logic element and microcontroller unit integrated into a single device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0005] Figure 1 is a block diagram of an example memory module 10 compatible with certain embodiments described herein. The memory module 10 comprises a printed-circuit card (PCB) 20, a first memory bank 30 on the PCB 20, and a second memory bank 40 on the PCB 20. The first memory bank 30 comprises a first plurality of volatile memory elements 32 and the second memory bank 40 comprises a second plurality of non-volatile memory elements 42. Certain embodiments described herein advantageously provide non-volatile storage via the second memory bank 40 in addition to high-performance (*e.g.*, high speed) storage via the first memory bank 30. Certain embodiments described herein utilize the second memory bank 40 as a flash "mirror" to provide back-up of the volatile first memory bank 30 in the event of power interruptions.

[0006] In certain embodiments, the memory module 10 is configured to be in electrical communication with a host system. Examples of host systems include, but are not

limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited.

[0007] In certain embodiments, the memory module 10 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, or 8-GB. Other memory capacities are also compatible with certain embodiments described herein. In addition, memory modules 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein.

[0008] In certain embodiments, the PCB 20 has an industry-standard form factor. For example, the PCB 10 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 10 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), mini-DIMM, VLP mini-DIMM, and micro-DIMM are also compatible with certain embodiments described herein.

[0009] The PCB 20 comprises an interface 22 that is configured to be in electrical communication with the host system (not shown). For example, the interface 22 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 22 provides a conduit for power voltage as well as data and address signals between the memory module 10 and the host system. For example, the interface 22 can comprise a standard 240-pin DDR2 edge connector.

[0010] In certain embodiments, the first plurality of volatile memory elements 32 comprises two or more dynamic random-access memory (DRAM) elements. Types of DRAM elements 32 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and synchronous DRAM (SDRAM). For example, in the block diagram of Figure 1, the first memory bank 30 comprises eight 64Mx8 DDR2 SDRAM elements 32. In addition, volatile memory elements 32 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Volatile memory elements 32 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-

grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[0011] In certain embodiments, the second pluarlity of non-volatile memory elements 42 comprises two or more flash memory elements. Types of flash memory elements 42 compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, and multi-level cell (MLC). For example, in the block diagram of Figure 1, the second memory bank 40 comprises 512 MB of flash memory organized as four 128Mbx8 NAND flash memory elements 42. In addition, non-volatile memory elements 42 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Non-volatile memory elements 42 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[0012] Figure 2 is a block diagram of an example memory module 10 with ECC (error-correcting code) having a first memory bank 30 with nine volatile memory elements 32 and a second memory bank 40 with five non-volatile memory elements 42 in accordance with certain embodiments described herein. The additional memory element 32 of the first memory bank 30 and the additional memory element 42 of the second memory bank 40 provide the ECC capability.

[0013] As schematically illustrated by Figure 1, in certain embodiments, the memory module 10 further comprises a voltage monitor circuit 50, a microcontroller unit (MCU) 60, a logic element 70, and a capacitor module 80. In certain embodiments, the MCU 60 provides memory management for the second memory bank 40 and controls data transfer between the first memory bank 30 and the second memory bank 40. The MCU 60 of certain embodiments comprises a 16-bit microcontroller, although other types of microcontrollers are also compatible with certain embodiments described herein. In certain embodiments, the capacitor module 80 comprises a step-up transformer 82, a step-down transformer 84, and a capacitor bank 86.

[0014] In certain embodiments, the logic element 70 comprises a field-programmable gate array (FPGA). Other types of logic elements 70 compatible with certain

embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element 70 is a custom device. In certain embodiments, the logic element 70 comprises various discrete electrical elements, while in certain other embodiments, the logic element 70 comprises one or more integrated circuits. Figure 3 is a block diagram of an example memory module 10 having a microcontroller unit 60 and logic element 70 integrated into a single device.

[0015] Under normal operation in certain embodiments, the host system accesses the first memory bank 30, rather than the second memory bank 40, because the volatile memory elements 32 have superior read/write characteristics. The voltage monitor circuit 50 monitors the power supplied by the host system via the interface 22. Upon detecting a low power (*e.g.*, indicative of a powering down of the host system), the voltage monitor circuit 50 sends a signal to the MCU 60 which responds by executing a write cycle on the second memory bank 40. During this write cycle, data is read from the first memory bank 30 and is transferred to the second memory bank 40 via the MCU 60.

[0016] As schematically illustrated by Figure 1, the logic element 70 of certain embodiments is in electrical communication with the second memory bank 40 and the MCU 60. The logic element 70 can provide signal level translation between the volatile memory elements 32 (*e.g.*, 1.8V SSTL-2 for DDR2 SDRAM elements) and the non-volatile memory elements 42 (*e.g.*, 3V TTL for NAND flash memory elements). In certain embodiments, the logic element 70 is also programmed to perform address decoding for the first memory bank 30 and the second memory bank 40.

[0017] During normal operation in certain embodiments, the step-up transformer 82 keeps the capacitor bank 86 charged at a peak value. In certain embodiments, the step-down transformer 84 acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (*e.g.*, 1.8V to the volatile DRAM elements 32 and 3.0V to the non-volatile flash memory elements 42) during power down. In certain embodiments, the memory module 10 further comprises switch 90 (*e.g.*, FET switch) that switches between the charged capacitor bank 86 and system power received via the interface 22. The switch 90 of

certain embodiments advantageously ensures that the volatile memory elements 32 are powered long enough for the data to be stored in the non-volatile memory elements 42, and then switches over to the system power.

[0018] When normal operation resumes, data is transferred from the non-volatile memory bank 40 to the volatile memory bank 30 via the MCU 60. The host system can then resume accessing the volatile memory bank 30 of the memory module 10. In certain embodiments, the transfer of data from the volatile memory bank 30 to the non-volatile memory bank 40, or from the non-volatile memory bank 40 to the volatile memory bank 30, takes less than one minute per GB.

[0019] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

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