SDR SDRAM

MT48LC16M4A2 – 4 Meg x 4 x 4 Banks
MT48LC8M8A2 – 2 Meg x 8 x 4 Banks
MT48LC4M16A2 – 1 Meg x 16 x 4 Banks

Features

- PC100- and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full-page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh modes: standard and low-power (not available on AT devices)
- Auto refresh
  - 64ms, 4096-cycle refresh (commercial and industrial)
  - 16ms, 4096-cycle refresh (automotive)
- LVTTL-compatible inputs and outputs
- Single 3.3V ±0.3V power supply

Options — Marking

- Configuration
  - 16 Meg x 4 (4 Meg x 4 x 4 banks) — 16M4[3]
  - 8 Meg x 8 (2 Meg x 8 x 4 banks) — 8M8
  - 4 Meg x 16 (1 Meg x 16 x 4 banks) — 4M16
- Write recovery (^{t}WR)
  - ^{t}WR = 2 CLK — A2
- Plastic package – OCPL[1]
  - 54-pin TSOP II (400 mil) — TG
  - 54-pin TSOP II (400 mil) Pb-free — P
  - 54-ball VFBGA (x16 only) (8mm x 8mm) — F4
  - 54-ball VFBGA (x16 only) (8mm x 8mm) — B4[2]
- Timing – cycle time
  - 6ns @ CL = 3 — -6[3]
  - 6ns @ CL = 3 — -6A
  - 7.5ns @ CL = 3 (PC133) — -75[3]
  - 7.5ns @ CL = 2 (PC133) — -7E
- Self refresh
  - Standard — None
  - Low-power — L[3]
- Operating temperature range
  - Commercial (0°C to +70°C) — None
  - Industrial (–40°C to +85°C) — IT
  - Automotive (–40°C to +105°C) — AT[2]
- Revision — :G, :J

Notes:
1. Off-center parting line.
2. Contact Micron for availability.
3. Available only on Revision G.

Table 1: Key Timing Parameters

CL = CAS (READ) latency

Speed Grade	Clock Frequency (MHz)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-6	167	3-3-3	18	18	18
-6A	167	3-3-3	18	18	18
-75	133	3-3-3	20	20	20
-7E	133	2-2-2	15	15	15

Table 2: Address Table

Parameter	16 Meg x 4	8 Meg x 8	4 Meg x 16
Configuration	4 Meg x 4 x 4 banks	2 Meg x 8 x 4 banks	1 Meg x 16 x 4 banks
Refresh count	4K	4K	4K
Row addressing	4K A[11:0]	4K A[11:0]	4K A[11:0]
Bank addressing	4 BA[1:0]	4 BA[1:0]	4 BA[1:0]
Column addressing	1K A[9:0]	512 A[8:0]	256 A[7:0]

Table 3: 64Mb SDR Part Numbering

Part Numbers	Architecture	Package
MT48LC16M4A2TG	16 Meg x 4	54-pin TSOP II
MT48LC16M4A2P	16 Meg x 4	54-pin TSOP II
MT48LC8M8A2TG	8 Meg x 8	54-pin TSOP II
MT48LC8M8A2P	8 Meg x 8	54-pin TSOP II
MT48LC4M16A2TG	4 Meg x 16	54-pin TSOP II
MT48LC4M16A2P	4 Meg x 16	54-pin TSOP II
MT48LC4M16A2B4[1]	4 Meg x 16	54-ball VFBGA
MT48LC4M16A2F4[1]	4 Meg x 16	54-ball VFBGA

Note: 1. FBGA Device Decoder: www.micron.com/decoder.

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