

# SDR SDRAM

**MT48LC64M4A2 – 16 Meg x 4 x 4 banks**

**MT48LC32M8A2 – 8 Meg x 8 x 4 banks**

**MT48LC16M16A2 – 4 Meg x 16 x 4 banks**

## Features

- PC100- and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh mode (not available on AT devices)
- Auto refresh
  - 64ms, 8192-cycle refresh (commercial and industrial)
  - 16ms, 8192-cycle refresh (automotive)
- LVTTL-compatible inputs and outputs
- **Single 3.3V ±0.3V power supply**

## Options

- Configurations
  - 64 Meg x 4 (16 Meg x 4 x 4 banks)
  - 32 Meg x 8 (8 Meg x 8 x 4 banks)
  - 16 Meg x 16 (4 Meg x 16 x 4 banks)
- Write recovery (<sup>t</sup>WR)
  - <sup>t</sup>WR = 2 CLK
- Plastic package – OCPL<sup>1</sup>
  - 54-pin TSOP II OCPL<sup>1</sup> (400 mil) (standard)
  - 54-pin TSOP II OCPL<sup>1</sup> (400 mil) Pb-free
  - 60-ball TFBGA (x4, x8) (8mm x 16mm)
  - 60-ball TFBGA (x4, x8) (8mm x 16mm) Pb-free
  - 54-ball VFBGA (x16) (8mm x 14 mm)
  - 54-ball VFBGA (x16) (8mm x 14 mm) Pb-free
  - 54-ball VFBGA (x16) (8mm x 8 mm)
  - 54-ball VFBGA (x16) (8mm x 8 mm) Pb-free
- Timing – cycle time
  - 6ns @ CL = 3 (x8, x16 only)
  - 7.5ns @ CL = 3 (PC133)
  - 7.5ns @ CL = 2 (PC133)
- Self refresh
  - Standard
  - Low power
- Operating temperature range
  - Commercial (0°C to +70°C)
  - Industrial (–40°C to +85°C)
  - Automotive (–40°C to +105°C)
- Revision

## Marking

64M4
32M8
16M16
A2
TG
P
FB
BB
FG <sup>2</sup>
BG <sup>2</sup>
F4 <sup>3</sup>
B4 <sup>3</sup>
-6A
-75 <sup>2</sup>
-7E
None
L <sup>2</sup> , <sup>4</sup>
None
IT
AT <sup>4</sup>
:D/:G

- Notes:
1. Off-center parting line.
  2. Only available on Revision D.
  3. Only available on Revision G.
  4. Contact Micron for availability.

**Table 1: Key Timing Parameters**

CL = CAS (READ) latency

Speed Grade	Clock Frequency (MHz)	Target <sup>t</sup> RCD- <sup>t</sup> RP-CL	<sup>t</sup> RCD (ns)	<sup>t</sup> RP (ns)	CL (ns)
-6A	167	3-3-3	18	18	18
-75	133	3-3-3	20	20	20
-7E	133	2-2-2	15	15	15

**Table 2: Address Table**

Parameter	64 Meg x 4	32 Meg x 8	16 Meg x 16
Configuration	16 Meg x 4 x 4 banks	8 Meg x 8 x 4 banks	4 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row addressing	8K A[12:0]	8K A[12:0]	8K A[12:0]
Bank addressing	4 BA[1:0]	4 BA[1:0]	4 BA[1:0]
Column addressing	2K A[9:0], A11	1K A[9:0]	512 A[8:0]

**Table 3: 256Mb SDR Part Numbering**

Part Numbers	Architecture	Package
MT48LC64M4A2TG	64 Meg x 4	54-pin TSOP II
MT48LC64M4A2P	64 Meg x 4	54-pin TSOP II
MT48LC64M4A2FB <sup>1</sup>	64 Meg x 4	60-ball FBGA
MT48LC64M4A2BB <sup>1</sup>	64 Meg x 4	60-ball FBGA
MT48LC32M8A2TG	32 Meg x 8	54-pin TSOP II
MT48LC32M8A2P	32 Meg x 8	54-pin TSOP II
MT48LC32M8A2FB <sup>1</sup>	32 Meg x 8	60-ball FBGA
MT48LC32M8A2BB <sup>1</sup>	32 Meg x 8	60-ball FBGA
MT48LC16M16A2TG	16 Meg x 16	54-pin TSOP II
MT48LC16M16A2P	16 Meg x 16	54-pin TSOP II
MT48LC16M16A2FG	16 Meg x 16	54-ball FBGA
MT48LC16M16A2BG	16 Meg x 16	54-ball FBGA

 Note: 1. FBGA Device Decoder: [www.micron.com/decoder](http://www.micron.com/decoder).

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