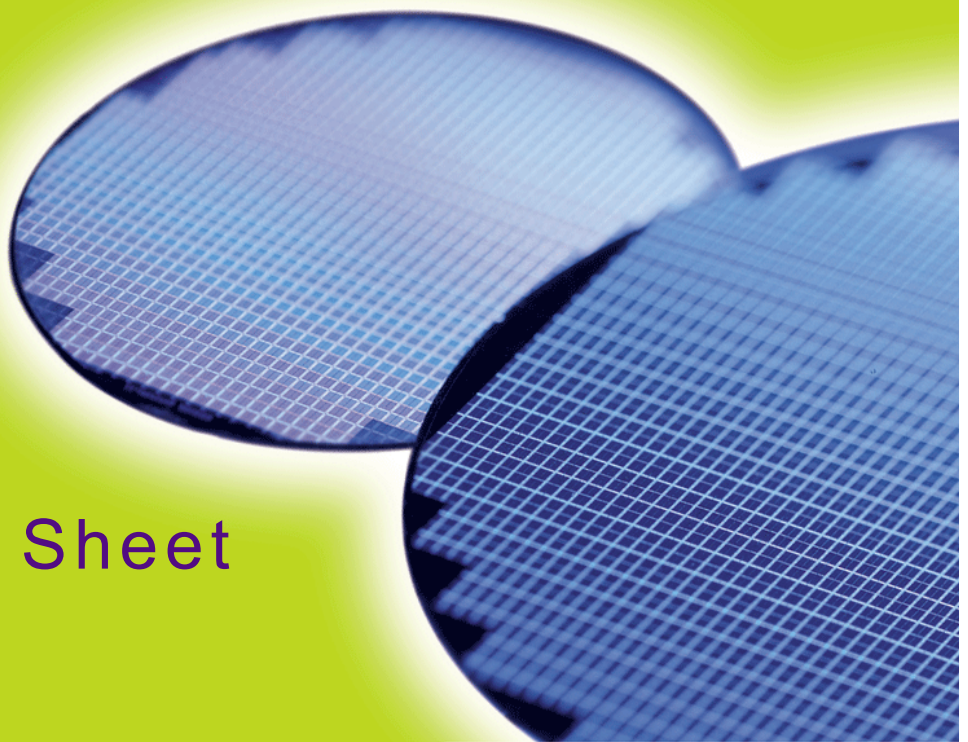


HY[B/I]39S256[40/80/16]0FT(L)
HY[B/I]39S256[40/80/16]0FE(L)
HYB39S256[40/80/16]0FF(L)
HYB39S256407FE

*256-MBit Synchronous DRAM
SDRAM*



Internet Data Sheet

Rev. 1.42

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HY[B/I]39S256[40/80/16]0FT(L), HY[B/I]39S256[40/80/16]0FE(L), HYB39S256[40/80/16]0FF(L), HYB39S256407FE

Revision History: 2007-09, Rev. 1.42

Page	Subjects (major changes since last revision)
All	Adapted internet edition
7	Corrected SDRAM organization for x4 in Table 4

Previous Revision: 2007-09, Rev. 1.41

All	Editorial Change
4	Corrected HYB39S256407FF-7 to HYP39S256407FE-7

Previous Revision: 2007-04, Rev. 1.40

4	Corrected HYB39S256400FE-7 to HYB39S256400FF-7
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Previous Revision: 2007-03, Rev. 1.30

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1 Overview

This chapter lists all main features of the product family HYB39S256[400/800/160]F[E/T/F](L) and the ordering information.

1.1 Features

- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C Standard Operating Temperature
- -40 to 85 °C Industrial Operating Temperature
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{\text{CAS}}$ Latency: 2 & 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8 and full page
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x4, x8)
- Data Mask for Byte Control (x16)
- Auto Refresh (CBR) and Self Refresh
- Power Down and Clock Suspend Mode
- 8192 refresh cycles / 64 ms (7.8 μs)
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V \pm 0.3 V Power Supply
- LVTTTL Interface versions
- Packages:
 - P(G)–TSOPII–54 (400mil width)
 - PG–TFBGA–54

TABLE 1
Performance

Product Type Speed Code			-6	-7	Unit
Speed Grade			PC166–333	PC133–222	—
Max. Clock Frequency	@CL3	f_{CK3}	166	143	MHz
		t_{CK3}	6	7	ns
		t_{AC3}	5.4	5.4	ns
	@CL2	t_{CK2}	7.5	7.5	ns
		t_{AC2}	5.4	5.4	ns

1.2 Description

The HYB39S256[400/800/160]F[E/T/F](L) are four bank Synchronous DRAMs organized as 4 banks x 16 MBit x4, 4 banks x 8 MBit x8 and 4 banks x 4 Mbit x16 respectively. These synchronous devices achieve high speed data transfer rates for $\overline{\text{CAS}}$ latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with Qimonda's advanced 0.11- μm 256-MBit DRAM process technology.



The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, $\overline{\text{CAS}}$ latency and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V \pm 0.3 V power supply. All 256-Mbit components are available in P(G)-TSOPII-54 and PG-TFBGA-54 packages.

TABLE 2

Ordering Information for RoHS Compliant Products

Product Type	Speed Grade	Description	Package	Note
Standard Operating Temperature				
HYB39S256407FE-7	PC133-222	143MHz 64M x 4 SDRAM	PG-TFBGA-54	¹⁾ 
HYB39S256400FF-7			PG-TFBGA-54	
HYB39S256400FE-7			PG-TSOPII-54	
HYB39S256400FFL-7			PG-TFBGA-54	
HYB39S256400FEL-7			PG-TSOPII-54	
HYB39S256800FF-7		143MHz 32M x 8 SDRAM	PG-TFBGA-54	
HYB39S256800FE-7			PG-TSOPII-54	
HYB39S256800FFL-7			PG-TFBGA-54	
HYB39S256800FEL-7			PG-TSOPII-54	
HYB39S256160FF-7		143MHz 16M x 16 SDRAM	PG-TFBGA-54	
HYB39S256160FE-7			PG-TSOPII-54	
HYB39S256160FFL-7			PG-TFBGA-54	
HYB39S256160FEL-7			PG-TSOPII-54	
HYB39S256160FF-6		166MHz 16M x 16 SDRAM	PG-TFBGA-54	
HYB39S256160FE-6			PG-TSOPII-54	
HYB39S256160FFL-6			PG-TFBGA-54	
HYB39S256160FEL-6	PG-TSOPII-54			
Industrial Operating Temperature				
HYI39S256800FE-7	PC166-333	143MHz 32M x 8 SDRAM	PG-TSOPII-54	¹⁾ 
HYI39S256160FE-7		143MHz 16M x 16 SDRAM		

¹⁾ RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

TABLE 3

Ordering Information for Lead-Containing Products

Product Type	Speed Grade	Description	Package
Standard Operating Temperature			
HYB39S256400FT-7	PC133-222	143MHz 64M x 4 SDRAM	P-TSOPII-54
HYB39S256400FTL-7			
HYB39S256800FT-7		143MHz 32M x 8 SDRAM	
HYB39S256800FTL-7			
HYB39S256160FT-7		143MHz 16M x 16 SDRAM	
HYB39S256160FTL-7			
HYB39S256160FT-6		166MHz 16M x 16 SDRAM	
Industrial Operating Temperature			
HYI39S256800FT-7	PC133-222	143MHz 32M x 8 SDRAM	P-TSOPII-54
HYI39S256160FT-7		143MHz 16M x 16 SDRAM	

Note: For product nomenclature see **Chapter 6** of this data sheet

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