Technology Note

PCI Bus Variation

Netlist Ex 2016
Samsung v Netlist
IPR2022-00996

www.euresys.com

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PCI

The PCI bus specification is handled by the PCI-SIG (PCI Special Interest Group), which is an association of numerous industrial actors in the field.
Euresys s.a. is a member of the PCI-SIG (vendor ID h1805).
The web site address of PCI-SIG is http://www.pcisig.com

Purpose of this Application Note

The purpose of this document is to provide Euresys' customers with some background information on PCI bus variants. This will help them to understand how to match frame grabbers and PC motherboards in order to achieve the expected system performance.

PCI Variants

Conventional PCI

The original PCI Revision 1.0 local bus specification was introduced in June 1992. The industrial inception of this technology started with PCI Revision 2.0 in April 1993, which included expansion slots and 66 MHz clock rate support. PCI Revision 2.1 in June 1995 introduced significant improvements related to 66 MHz operation and bandwidth efficiency. In December 1998, the Revision 2.2 clarified some detail issues. The next revision to be issued is Revision 2.3. In this document, the specification for 5 Volt add-in cards is removed, although the specification for 5 Volt system connectors is retained. The final revision of the Conventional PCI bus will be Revision 3.0. The specification for 5 Volt system connectors is removed, which definitely precludes the use of 5 Volt add-in cards. Conventional PCI is characterized by a bus width of 32 or 64 bits, and a clock speed of 33 or 66 MHz. Any combination of width and speed can be found. The vast majority of existing desktop PCs are equipped with Conventional PCI technology.

PCI-X

PCI-X is a high performance evolution of Conventional PCI. It uses the same hardware structure, which makes it possible to operate a PCI-X add-in card in a Conventional PCI slot, and vice-versa. PCI-X allows for a considerably higher bandwidth than Conventional PCI. It is characterized by a higher clock speed up to 133 MHz, and is usually found in the 64-bit bus width, although the 32-bit width can exist. Revision 1.0 initially issued in July 2000 presently specifies PCI-X as an addendum to Conventional PCI. An improvement to PCI-X is under preparation, and will be specified by PCI-X Revision 2.0. It is intended to extend the clocking capability to 266 and 533 MHz. The PCI-X technology is dedicated to server applications, and is therefore found in many high-end PC motherboards.

PCI Express

PCI Express availability is expected in 2004. PCI Express will be a replacement for Conventional PCI offering much more flexibility and performance while maintaining software compatibility. The hardware bus structure is substantially different, but the card form factor of the existing desktop enclosures will remain. The connector will change. PCI Express uses a serialized point-to-point technology instead of massive parallel data transportation. The initial standard Revision 1.0 has been released in 2002.

PCI Performance

Characterizing Parameters

There are two essential parameters characterizing a PCI bus: the bus width and the clock speed. Both of them directly influence the bus performance.

Bus Width

The transmission medium used by the PCI bus is a set of 32 or 64 parallel electrical lines. This figure is called the bus width. An elementary block of 32- or 64-bit data is transferred from a source agent (initiator) to a destination agent (target) within one clock cycle. 32-bit data can be considered as a set of 4 bytes, and 64-bit data can be considered as a set of 8 bytes.

Clock Speed

The PCI bus is a synchronous system. This means that each agent connected to a bus is actuated by a clock signal exhibiting the same frequency and phase. For Conventional PCI, the clock speed is 33 or 66 MHz. For PCI-X, the clock speed is 66 MHz or 133 MHz. The data transfer principle used by PCI involves bursts of data transmitted at the clock speed. The pair of agents exchanging data are called "good citizens" when they cooperate to realize long data bursts. The clock speed is an indication of the data throughput capability of the bus, but high performance transfer is subordinated to the good citizenship of all intervening agents, including the motherboard itself.

Data Rate

At a given time, an initiator agent is transferring data with a target agent. This transaction cannot last more than a few microseconds, as another agent may request its own transfer resources. An arbitration process successively assigns the bus ownership to all requesting agents in such a way that all pending transactions are satisfied. The practical data rate over the bus is the effective transfer rate for all transactions averaged over a substantial period of time. The data rate is expressed in Megabytes per second (MB/s). The peak data rate is a theoretical figure which is only reached during a very short amount of time inside a data burst. The practical data rate is always lower than the peak data rate. Achieving sustained full speed bursts is a way for the practical data rate to approach the peak data rate. However, other considerations, such as transaction arbitration latencies, limit the usability of the peak data rate. Dictated from experience, a practical data rate in excess of some 70% of the peak data rate should not be expected. The terms “bandwidth” and “throughput” are used as equivalent to “data rate”.

PCI Bandwidth Summary

PCI variant	Clock speed	Bus width		Peak data rate	Practical data rate
Conventional PCI only	33 MHz	32 bits	4 bytes	132 MB/s	90 MB/s
		64 bits	8 bytes	264 MB/s	180 MB/s
Conventional PCI or PCI-X	66 MHz	32 bits	4 bytes	264 MB/s	180 MB/s
		64 bits	8 bytes	528 MB/s	360 MB/s
PCI-X only	133 MHz	32 bits	4 bytes	532 MB/s	360 MB/s
		64 bits	8 bytes	1064 MB/s	720 MB/s

The peak data rate is obtained by arithmetically multiplying the clock speed and the number of bytes making up the data width. The practical figures supplied in this table should be considered as a “rule of the thumb” when evaluating system performance. The real performance essentially depends on systems characteristics, and should be validated on a real system.

Number of Slots

The PCI Bus as a Set of Slots

All desktop and server PC motherboards can accommodate additional internal hardware to fulfill special peripheral functions, such as frame grabbers. The prevalent way to achieve this is the peripheral bus, namely the PCI bus. The PCI bus exposes several so-called slots connected in parallel, enabling the insertion of add-in cards on a one-per-slot basis to implement the additional peripheral functions. For electrical reasons, any PCI bus has a limited number of slots. The standard defines how many slots a given PCI bus is allowed to expose. Modern motherboards may exhibit more than one bus, possibly with different attributes. The following applies to each individual bus provided by the motherboard.

Maximum Slot Summary

PCI variant	Clock speed	Practical data rate
Conventional PCI only	33 MHz	Four
	66 MHz	Two
PCI-X	66 MHz	Four
	133 MHz	Two

For operation at 66 MHz, PCI-X is preferred to Conventional PCI, as the number of available slots is double. This is a key technical feature conveying a strong justification for PCI-X.

Signaling Voltage

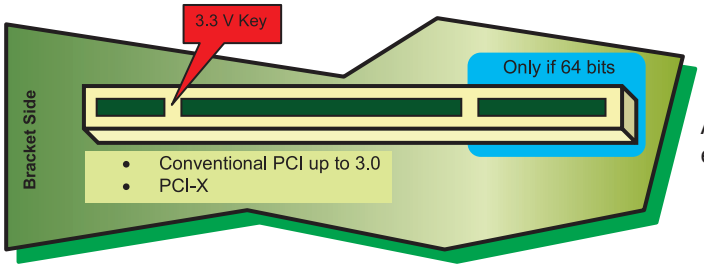
Definition

The digital data transmission through the PCI bus operates under certain voltage levels defining the low and high logic states. For technological reasons, it has been adequate to consider two systems in this respect. These are the 5 Volt signaling environment and the 3.3 Volt signaling environment. The signaling environments cannot be mixed. This means that all add-in cards linked to a PCI bus must adopt the signaling voltage imposed by the motherboard.
The 5 Volt system is older, and tends to be replaced by the 3.3 Volt system. This signaling voltage migration is the main motivation for the latest revisions of Conventional PCI from 2.2 to 3.0.

Slot Variants

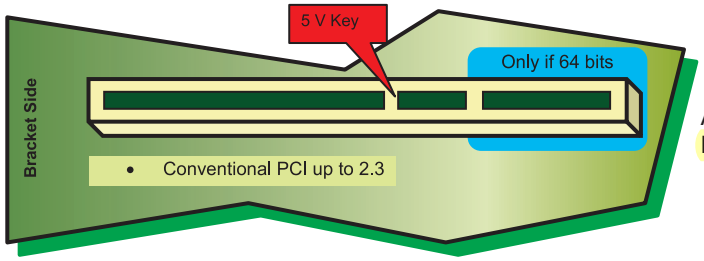
The system connectors (or slots) can be of the 3.3 Volt or 5 Volt type. All slots of a particular PCI bus are identical, reflecting the signaling voltage (3.3 Volt or 5 Volt) imposed by the motherboard.

3.3 Volt Connector



A bus complying with any PCI variant can exhibit the 3.3 Volt connector.

5 Volt Connector

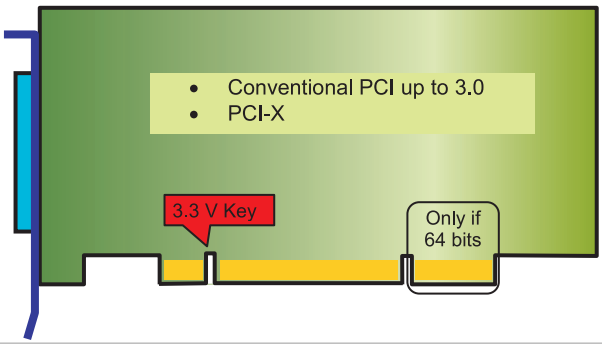


A bus complying with Conventional PCI 3.0 or PCI-X cannot exhibit the 5 Volt connector.

Add-in Card Variants

A PCI board can be designed to be operated in the 3.3 Volt or 5 Volt environment, or both. In the latter case, it is often called a “universal” card. There are three types of add-in cards featuring an edge connector shape that adequately fits into an allowable system connector.

3.3 Volt Add-in Card



An add-in card complying with any PCI variant can be a 3.3 Volt card.

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