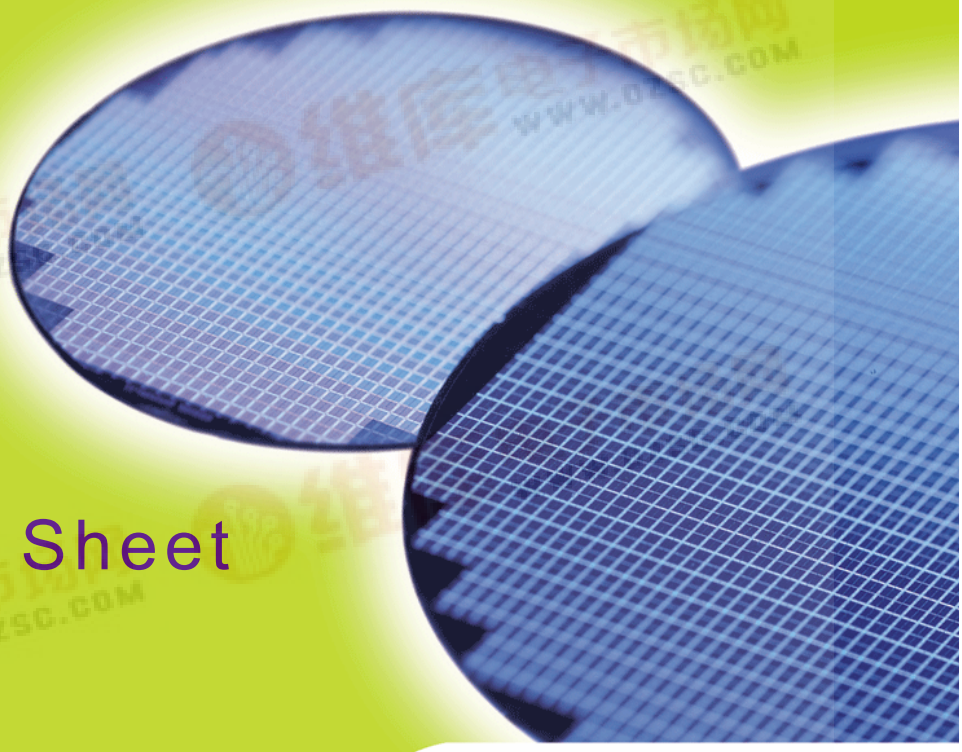
June 2007

HYB39SC256[80/16]0FE
HYI39SC256[80/16]0FF

256-MBit Synchronous DRAM
Green Product
SDRAM



Internet Data Sheet

Rev. 1.25

HYB39SC256[80/16]0FE, HYI39SC256[80/16]0FF Revision History: 2007-06, Rev. 1.25	
Page	**Subjects (major changes since last revision)**
All	Adapted internet edition
41	Corrected in figure 28 (auto refresh) tRC to tRFC
Previous Revision: 2007-06, Rev. 1.24	
8	Corrected figure 1
11,12	Corrected block diagram
Previous Revision: 2007-06, Rev. 1.23	
18	Added text for Auto Refresh Command (CBR)
Previous Revision: 2007-06, Rev. 1.22	
6	Corrected ball DQ0 to 2,8A for data signals x16 organization
6	Corrected data Data Signal Bus [7:0] for data signals x8 organization
Previous Revision: 2007-06, Rev. 1.21	
13	Corrected operation command "Power Down / Clock suspend ...” in truth table
Previous Revision: 2007-05, Rev. 1.2	
13	Corrected operation command "Power Down Exit" to X (WE#)
15	Corrected text to "After the mode register is set a NOP command is required" , chapter 3.2
19	Corrected text to "One clock delay is required for mode entry and exit", chapter 3.4
21	Corrected the line "Input Capacitances: CK" in table 10, chapter 4
21	Corrected to A0-A12 in table 10, chapter 4
22	Corrected tCK MIN in table 13
22	Corrected CLE setup time in table 13
Previous Revision: 2007-05, Rev. 1.11	
6	Corrected A6 position from H to 3H in table 3
Previous Revision: 2006-09, Rev. 1.1	

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all?
Your feedback will help us to continuously improve the quality of this document.
Please send your proposal (including a reference to this document) to:
techdoc@qimonda.com

1 Overview

This chapter lists all main features of the product family HY[B/I]39SC256[80/16]0F[E/F] and the ordering information.

1.1 Features

- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C Operating Temperature for HYB...
- -40 to 85 °C Operating Temperature for HYI...
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 2 & 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8 and full page
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x8, x16)
- Data Mask for Byte Control (x16)
- Auto Refresh (CBR) and Self Refresh
- Power Down and Clock Suspend Mode
- 8192 refresh cycles / 64 ms (7.8 µs)
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V ± 0.3 V Power Supply
- LVTTL Interface
- Plastic Packages
  - PG-TSOPII-54 (400mil width)
  - PG-TFBGA-54 (12 mm x 8 mm)
- RoHS compliant product

TABLE 1
Performance

Product Type Speed Code			–6	–7	Unit
Speed Grade			PC166–333	PC143–333 PC133–222[1)]	—
Max. Clock Frequency	@CL3	f_{CK3}	166	143	MHz
		t_{CK3}	6	7	ns
		t_{AC3}	5.4	5.4	ns
	@CL2	t_{CK2}	7.5	7.5	ns
		t_{AC2}	5.4	5.4	ns

1) Max. Frequency CL/t_{RCD} / t_{RP}

1.2 Description

The HY[B/I]39SC256[80/16]0F[E/F] are four bank Synchronous DRAM's organized as 16 MBit ×8 and 8 Mbit x16 respectively. These synchronous devices achieve high speed data transfer rates for CAS latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with Qimonda advanced 0.11 µm 256-MBit DRAM process technology.

The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V ± 0.3 V power supply. All 256-Mbit components are available in PG–TSOPII–54 and PG-TFBGA-54 packages.

TABLE 2

Ordering Information for RoHS Compliant Products

Product Type[1)]	Speed Grade	Description	Package	Note
Standard Operating Temperature (0 to 70 °C)				
HYB39SC256800FE-6	PC166–333	166MHz 16M ×8 SDRAM	PG-TSOPII-54	2)
HYB39SC256160FE-6		166MHz 8M ×16 SDRAM	green Product	
HYB39SC256800FE-7	PC133–222	143MHz 16M ×8 SDRAM		
HYB39SC256800FEH-7				
HYB39SC256160FE-7		143MHz 8M ×16 SDRAM		
HYB39SC256160FEH-7				
HYB39SC256160FF-6	PC166–333	166MHz 8M ×16 SDRAM	PG-TFBGA-54	2)
HYB39SC256160FF-7	PC133–222	143MHz 8M ×16 SDRAM	green Product	
HYB39SC256800FF-7		143MHz 8M ×8SDRAM		
Industrial Operating Temperature (-40 to 85 °C)				
HYI39SC256800FE-6	PC166–333	166MHz 16M ×8 SDRAM	PG-TSOPII-54	2)
HYI39SC256160FE-6		166MHz 8M ×16 SDRAM	green Product	
HYI39SC256800FE-7	PC133–222	143MHz 16M ×8 SDRAM		
HYI39SC256160FE-7		143MHz 8M ×16 SDRAM		

1) Please check with your Qimonda representative that leadtime and availability of your preferred device and version meet your project requirements.

2) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

*Note: For product nomenclature see **Chapter 6** of this data sheet*

2 Configuration

This chapter contains the pin configuration table, the TSOP and FBGA package drawing, and the block diagrams for the ×8, ×16 organization of the SDRAM.

2.1 Pin Configuration

Listed below are the pin configurations sections for the various signals of the SDRAM

TABLE 3
Pin Configuration of the SDRAM

Pin No.	Name	Pin Type	Buffer Type	Function
Clock Signals x8/x16 Organization				
38,2F	CLK	I	LVTTL	**Clock Signal CK**
37,3F	CKE	I	LVTTL	**Clock Enable**
Control Signals x8/x16 Organization				
18, 8F	$\overline{RAS}$	I	LVTTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
17, 7F	$\overline{CAS}$	I	LVTTL	
16, 9F	$\overline{WE}$	I	LVTTL	
19, 9G	$\overline{CS}$	I	LVTTL	**Chip Select**
Address Signals x8/x16 Organization				
20, 7G	BA0	I	LVTTL	**Bank Address Signals 1:0**
21, 8G	BA1	I	LVTTL	
23, 7H	A0	I	LVTTL	**Address Signal, Address Signal 10/Auto precharge**
24, 8H	A1	I	LVTTL	
25, 8J	A2	I	LVTTL	
26, 7J	A3	I	LVTTL	
29, 3J	A4	I	LVTTL	
30, 2J	A5	I	LVTTL	
31, 3H	A6	I	LVTTL	
32, 2H	A7	I	LVTTL	
33, 1H	A8	I	LVTTL	
34, 3G	A9	I	LVTTL	
22, 9H	A10	I	LVTTL	
35, 2G	A11	I	LVTTL	
36, 1G	A12	I	LVTTL	

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.