4.20.3 – 144 Pin, PC133 SDRAM Unbuffered SO–DIMM, Reference Design Specification

PC133 SDRAM Unbuffered SO-DIMM

Reference Design Specification

Revision 1.02

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1. Product Description

This reference specification defines the electrical and mechanical requirements for 144-pin, 3.3 Volt, 133 MHz, 64-bit wide, Unbuffered Synchronous DRAM Small Outline Dual In-Line Memory Modules (SDRAM SO-DIMMs).These SDRAM SO-DIMMs are intended for use as main memory when installed in systems such as mobile personal computers.

Reference design examples are included which provide an initial basis for Unbuffered SO-DIMM designs. Modifications to these reference designs are required to meet all system timing, signal integrity and thermal requirements for 133 MHz support. Other designs are acceptable, and all Unbuffered SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the JEDEC defined 144-pin 8-Byte Unbuffered SDRAM SO-DIMM product. (Refer to JEDEC standard 21-C, Section 4.5.6, at www.jedec.org).

Product Family Attributes

SO-DIMM Organization	x 64
SO-DIMM Dimensions (nominal)	67.6 mm (2.66”) x 25.40 mm (1.0”) to x 31.75 mm (1.25”)
Pin Count	144
SDRAMs Supported	64 Mb, 128 Mb, 256 Mb
Capacity	32 MB, 64 MB, 128 MB, 256 MB
Serial PD	Consistent with JEDEC Rev. 2.0
Voltage Options	3.3 volt (V_{DD}/V_{DDQ})
Interface	LVTTL

2. Environmental Requirements

PC133 SDRAM Unbuffered SO-DIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +65	∝C	1
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature	-50 to +100	∝C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

3. Architecture

Pin Description

CK(0:1)	Clock Inputs	2	DQ(0:63)	Data Input/Output	64
CKE(0:1)	Clock Enables	2	DQMB(0:7)	Data Mask	8
RAS	Row Address Strobe	1	V_{DD}	Power (3.3 V)	18
CAS	Column Address Strobe	1	V_{SS}	Ground	18
WE	Write Enable	1	SCL	Serial Presence Detect Clock Input	1
$\overline{S}$(0:1)	Chip Selects	2	SDA	Serial Presence Detect Data Input/Output	1
A(0:9,11:13)	Address Inputs	13	NC	No Connect	8
A10/AP	Address Input/Autoprecharge	1	DU	Don't Use - leave as NC	1
BA0-BA1	SDRAM Bank Address	2		**Total:**	144

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0 - CK1	Input	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0,1	Input	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S}0$ - $\overline{S}1$	Input	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by $\overline{S}0$; Bank 1 is selected by $\overline{S}1$.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0, BA1	Input	—	Selects which SDRAM bank of four is activated.
A0 - A9, A11-A13 A10/AP	Input	—	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A11 defines the column address (CA0-CA11) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63	Input Output	—	Data Bit Input/Output pins.
DQMB0 - DQMB7	Input	Active High	The Data Input/Output masks, associated with one data byte, place the DQ buffers in a high impedance state when sampled high. In Read mode, DQMB controls the output buffers like an output enable. In Write mode, DQMB operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high.
V_{DD}, V_{SS}	Supply		Power and ground for the module.
SDA	Input Output	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V_{DD} to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V_{DD} to act as a pull up.

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