National Semiconductor

December 12, 2007

LP2998
DDR-II and DDR-I Termination Regulator

General Description

The LP2998 linear regulator is designed to meet JEDEC SSTL-2 and JEDEC SSTL-18 specifications for termination of DDR-SDRAM and DDR-II memory. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5A continuous current as required for DDR-SDRAM termination. The LP2998 also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output as a reference for the chipset and DIMMs.

An additional feature found on the LP2998 is an active low shutdown ($\overline{SD}$) pin that provides Suspend To RAM (STR) functionality. When $\overline{SD}$ is pulled low the V_{TT} output will tri-state providing a high impedance output; while, V_{REF} remains active. A power savings advantage can be obtained in this mode through lower quiescent current.

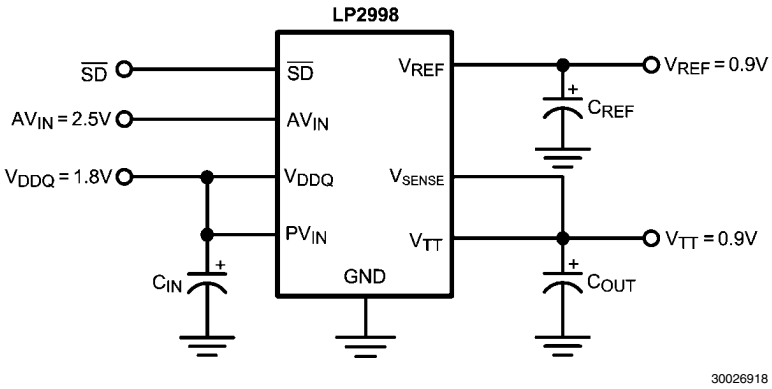
Features

- Source and sink current
- Low output voltage offset
- No external resistors required
- Linear topology
- Suspend to Ram (STR) functionality
- Low external component count
- Thermal Shutdown
- Available in SO-8, PSOP-8 packages

Applications

- DDR-I and DDR-II Termination Voltage
- SSTL-18 Termination
- SSTL-2 and SSTL-3 Termination
- HSTL Termination

Typical Application Circuit



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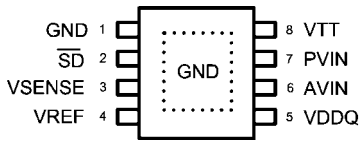
Connection Diagrams



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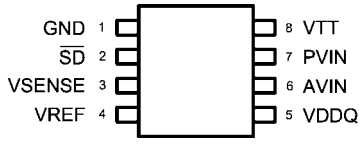
PSOP-8 Layout



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SO-8 Layout

Pin Descriptions

SO-8 Pin or PSOP-8 Pin	Name	Function
1	GND	Ground.
2	$\overline{SD}$	Shutdown.
3	VSENSE	Feedback pin for regulating V_{TT}.
4	VREF	Buffered internal reference voltage of V_{DDQ} /2.
5	VDDQ	Input for internal reference equal to V_{DDQ}/2.
6	AVIN	Analog input pin.
7	PVIN	Power input pin.
8	VTT	Output voltage for connection to termination resistors.
	EP	Exposed pad thermal connection. Connect to soft Ground.

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LP2998MA	SO-8	M08A	95 Units per Rail
LP2998MAX	SO-8	M08A	2500 Units Tape and Reel
LP2998MR	PSOP-8	MRA08A	95 Units Tape and Reel
LP2998MRX	PSOP-8	MRA08A	2500 Units Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

PVIN, AVIN, VDDQ to GND No pin should exceed AVIN	−0.3V to +6V
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C
SO-8 Thermal Resistance (θ_{JA})	151°C/W
PSOP-8 Thermal Resistance (θ_{JA})	43°C/W
Minimum ESD Rating (Note 2)	1kV

Operating Range

Junction Temp. Range (Note 3)	-40°C to +125°C
AVIN to GND	2.2V to 5.5V

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C and limits in **boldface type** apply over the full **Operating Temperature Range** (T_J = -40°C to +125°C) (Note 4). Unless otherwise specified, VIN = AVIN = PVIN = 2.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REF}	V_{REF} Voltage (DDR I)	VIN = VDDQ = 2.3V	**1.135**	1.150	**1.185**	V
		VIN = VDDQ = 2.5V	**1.235**	1.250	**1.285**	V
		VIN = VDDQ = 2.7V	**1.335**	1.350	**1.385**	V
	V_{REF} Voltage (DDR II)	PVIN = VDDQ = 1.7V	**0.837**	0.850	**0.887**	V
		PVIN = VDDQ = 1.8V	**0.887**	0.910	**0.937**	V
		PVIN = VDDQ = 1.9V	**0.936**	0.950	**0.986**	V
Z_{VREF}	V_{REF} Output Impedance	I_{REF} = -30 to +30 µA		2.5		kΩ
V_{TT}	V_{TT} Output Voltage (DDR I) (Note 7)	I_{OUT} = 0A				
		VIN = VDDQ = 2.3V	**1.120**	1.150	**1.190**	V
		VIN = VDDQ = 2.5V	**1.210**	1.250	**1.290**	V
		VIN = VDDQ = 2.7V	**1.320**	1.350	**1.390**	V
		I_{OUT} = +/- 1.5A				
		VIN = VDDQ = 2.3V	**1.125**	1.150	**1.190**	V
		VIN = VDDQ = 2.5V	**1.225**	1.250	**1.290**	V
		VIN = VDDQ = 2.7V	**1.325**	1.350	**1.390**	V
	V_{TT} Output Voltage (DDR II) (Note 7)	I_{OUT} = 0A, AVIN = 2.5V				
		PVIN = VDDQ = 1.7V	**0.822**	0.850	**0.887**	V
		PVIN = VDDQ = 1.8V	**0.874**	0.900	**0.939**	V
		PVIN = VDDQ = 1.9V	**0.923**	0.950	**0.988**	V
		I_{OUT} = +/- 0.5A, AVIN = 2.5V				
		PVIN = VDDQ = 1.7V	**0.820**	0.850	**0.890**	V
		PVIN = VDDQ = 1.8V	**0.870**	0.900	**0.940**	V
		PVIN = VDDQ = 1.9V	**0.920**	0.950	**0.990**	V
VOS_{Vtt}	V_{TT} Output Voltage Offset (V_{REF} – V_{TT}) for DDR I (Note 7)	I_{OUT} = 0A	**-30**	0	**30**	mV
		I_{OUT} = -1.5A	**-30**	0	**30**	mV
		I_{OUT} = +1.5A	**-30**	0	**30**	mV
	V_{TT} Output Voltage Offset (V_{REF} – V_{TT}) for DDR II (Note 7)					
		I_{OUT} = 0A	**-30**	0	**30**	mV
		I_{OUT} = -0.5A	**-30**	0	**30**	mV
		I_{OUT} = +0.5A	**-30**	0	**30**	mV
I_Q	Quiescent Current (Note 5)	I_{OUT} = 0A		320	**500**	µA
Z_{VDDQ}	VDDQ Input Impedance			100		kΩ
I_{SD}	Quiescent current in shutdown (Note 6)	SD = 0V		115	**150**	µA
I_{Q_SD}	Shutdown leakage current	SD = 0V		2	**5**	µA
V_{IH}	Minimum Shutdown High Level		**1.9**			V
V_{IL}	Maximum Shutdown Low Level				**0.8**	V
Iv	V_{TT} leakage current in shutdown	SD = 0V V_{TT} = 1.25V		1	**10**	µA
I_{SENSE}	V_{SENSE} Input current			13		nA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SD}	Thermal Shutdown (Note 6)			165		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			10		°C

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions see Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Note 3: At elevated temperatures, devices must be derated based on thermal resistance. The device in the SO-8 package must be derated at θ_{JA} = 151.2° C/W junction to ambient with no heat sink.

Note 4: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

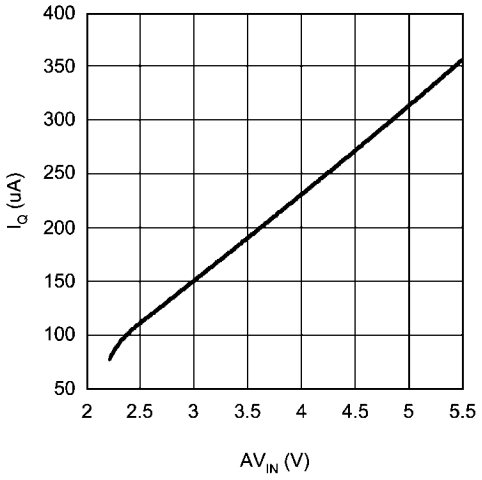
Note 5: Quiescent current defined as the current flow into AVIN.

Note 6: The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction to ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown.

Note 7: V_{TT} load regulation is tested by using a 10 ms current pulse and measuring V_{TT}.

Typical Performance Characteristics

Iq vs AV_{IN} in SD



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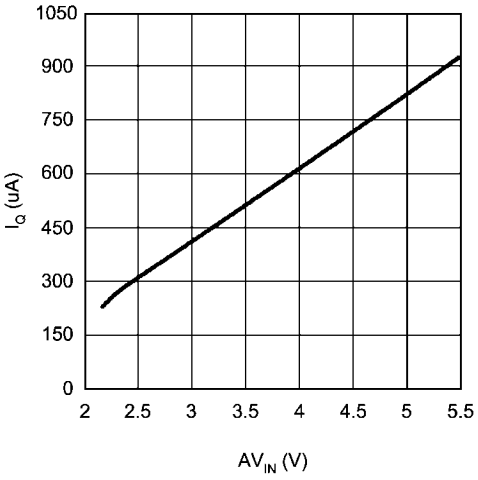
Iq vs AV_{IN}



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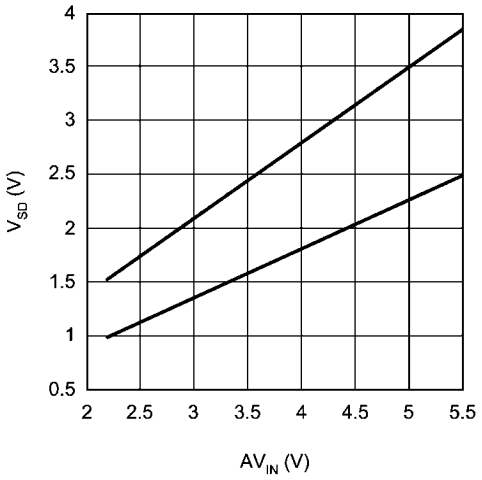
V_{IH} and V_{IL}



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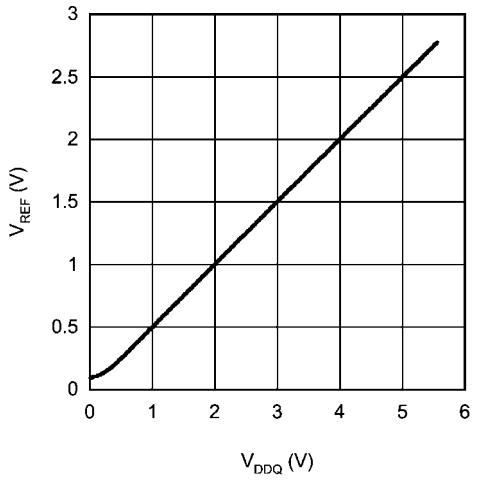
V_{REF} vs V_{DDQ}



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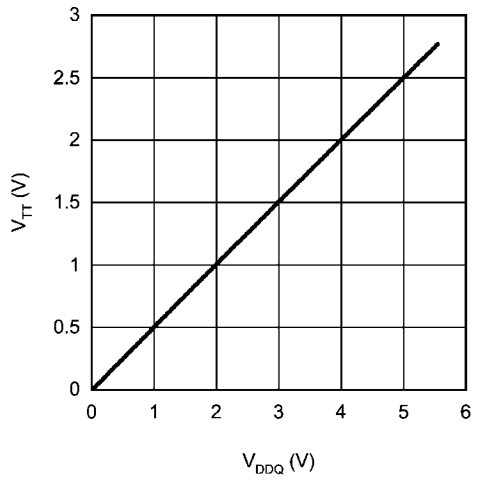
V_{TT} vs V_{DDQ}



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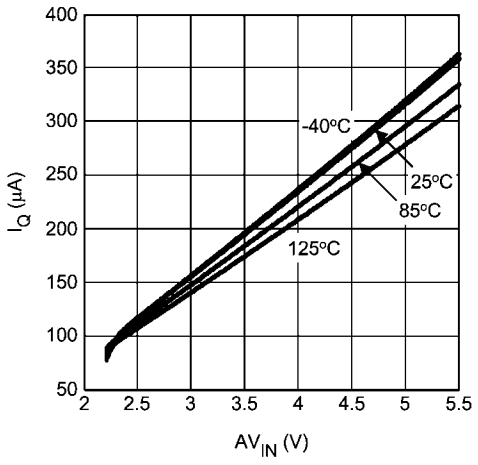
Iq vs AV_{IN} in SD Temperature



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